

关键参数

Key Parameters

V_{CES}		750	V
$V_{CE(sat)}$	Typ.	1.55	V
I_{CN}	Max.	315	A
Die Size		10.00×11.10	mm ²

特点

Features

- 沟槽栅，场截止 Trench Gate, Field Stop
- 低通态损耗 Low On-state Loss
- 低开关损耗 Low Switching Loss
- 软关断 Soft Turn Off
- 易并联使用 Easy Paralleling

电路结构

Circuit Configuration

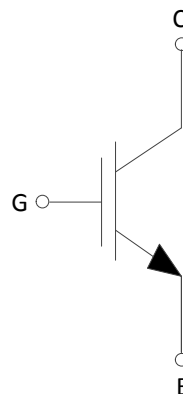


图 1. 电路结构

Fig. 1 Circuit configuration

最大额定值

Maximum Ratings

符号 Symbol	参数名称 Parameter	数值 Value	单位 Unit
V_{CE}	集电极-发射极电压, $T_{vj}=25\text{ }^{\circ}\text{C}$ Collector-emitter voltage, $T_{vj}=25\text{ }^{\circ}\text{C}$	750	V
V_{GE}	栅极-发射极电压 Gate-emitter voltage	±20	V
I_C	集电极电流, 由 $T_{vj\text{ max}}$ 限制 Collector-emitter current, limited by $T_{vj\text{ max}}$	315	A
I_{CM}	集电极峰值电流, 由 $T_{vj\text{ max}}$ 限制 Peak collector current, limited by $T_{vj\text{ max}}$	630	A
$T_{vj\text{ max}}$	最大允许结温 Max. Junction temperature	175	°C
$T_{vj(op)}$	工作结温 Operation Junction temperature	-40...+175	°C
t_{SC}	短路脉宽, $V_{GE}=15\text{V}$, $V_{CC}=400\text{V}$, $T_{vj}=150\text{ }^{\circ}\text{C}$ Short circuit pulse, $V_{GE}=15\text{V}$, $V_{CC}=400\text{V}$, $T_{vj}=150\text{ }^{\circ}\text{C}$	6	μs

静态特性值
Static Characteristics

晶圆测试, $T_{vj}=25\text{ }^{\circ}\text{C}$

Tested on wafer, $T_{vj}=25\text{ }^{\circ}\text{C}$

符号 Symbol	参数名称 Parameter	条件 Test Conditions	最小值 Min.	典型值 Typ.	最大值 Max.	单位 Unit
V_{CES}	集电极-发射极击穿电压 Collector-Emitter breakdown voltage	$V_{GE}=0V, I_C=1mA$	750			V
$V_{CE(sat)}$	集电极-发射极饱和电压 Collector-emitter saturation voltage	$V_{GE}=15V, I_C=60A$	0.70	0.95	1.20	V
$V_{GE(th)}$	栅极-发射极阈值电压 Gate threshold voltage	$I_C=5mA, V_{GE}=V_{CE}$	5.4	6.0	6.6	V
I_{CES}	集电极截止漏电流 Zero gate voltage collector current	$V_{CE}=750V, V_{GE}=0V$			10	μA
I_{GES}	栅极漏电流 Gate leakage current	$V_{GE}=\pm 20V, V_{CE}=0V$			500	nA

电特性值
Electrical Characteristics

除非特别声明, 否则 $T_{vj}=25\text{ }^{\circ}\text{C}$
 $T_{vj}=25\text{ }^{\circ}\text{C}$ unless otherwise stated

符号 Symbol	参数名称 Parameter	条件 Test Conditions	最小值 Min.	典型值 Typ.	最大值 Max.	单位 Unit
$V_{CE(sat)}$	集电极-发射极饱和电压 Collector-emitter saturation voltage	$V_{GE}=15V, I_C=315A$		1.55		V
		$V_{GE}=15V, I_C=315A, T_{vj}=150\text{ }^{\circ}\text{C}$		1.80		V
C_{ies}	输入电容 Input capacitance	$V_{CE}=25V, V_{GE}=0V, f=100kHz$		21.6		nF
C_{oes}	输出电容 Output capacitance			0.84		nF
C_{res}	反向传输电容 Reverse transfer capacitance			0.11		nF
R_g	内部栅极电阻 Integrated gate resistor			6		Ω

工艺参数值**Mechanical Parameters**

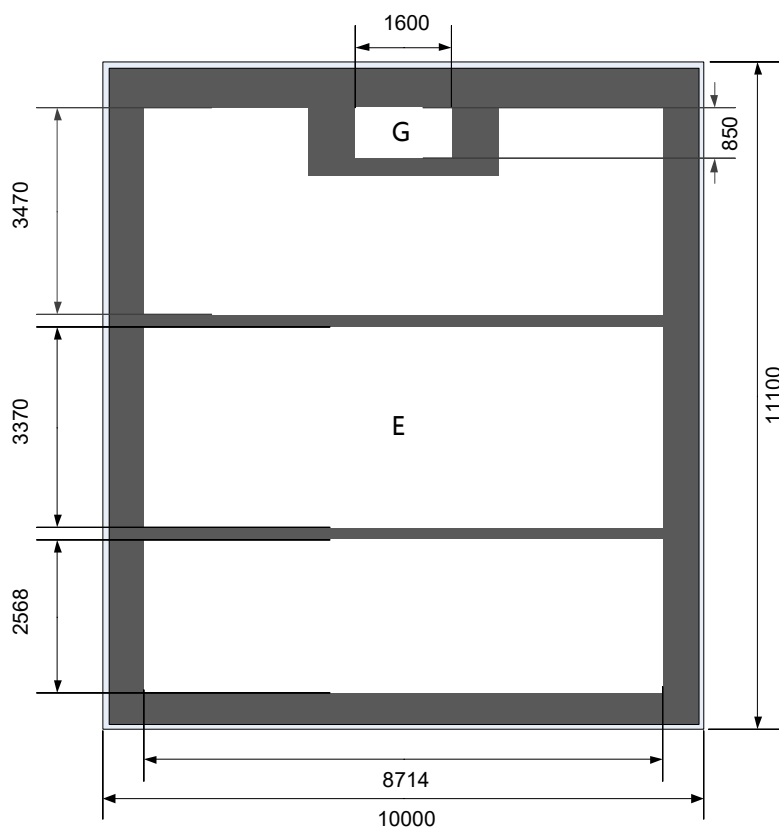
芯片尺寸 Chip size	10.00×11.10	mm ²
发射极键合区尺寸(包含栅极) Emitter pad size (incl. gate pad)	8.71×(2.57+3.37+3.47)	mm ²
栅极键合区尺寸 Gate pad size	1.60×0.85	mm ²
总面积 Area total	111.00	mm ²
厚度 Thickness	74	μm
晶圆尺寸 Wafer size	200	mm
每片晶圆上最大芯片数 Max. possible chips per wafer	230	
正面金属 Pad metal	Al/Si	
背面金属 Backside metal	Al-Ti-Ni-Ag	
正面钝化 Passivation frontside	Polyimide	
建议存储环境 Recommended storage environment	存储在原始容器中, 23°C 干燥氮气柜小于 6 个月 Store in original container, in dry nitrogen, <6 months at an ambient temperature of 23°C	

其他电特性**Further Electrical Characteristics**

开关和热学特性请参考相关模块数据手册

For switching characteristic and thermal properties, please refer to the device datasheet

This chip datasheet refers to the device datasheet	TG950FF08S3-S4A11	Ver 21.09
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E=发射极 G=栅极 单位：微米 E=Emitter G=Gate Unit: μm

图 2. 芯片外观尺寸

Fig. 2 Chip drawing

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