MITSUBISHI ELECTRIC

<HVIC>

M81748FP

1200V HIGH VOLTAGE HALF BRIDGE DRIVER

DESCRIPTION

M81748FP is high voltage Power MOSFET and IGBT gate driver for half bridge applications.

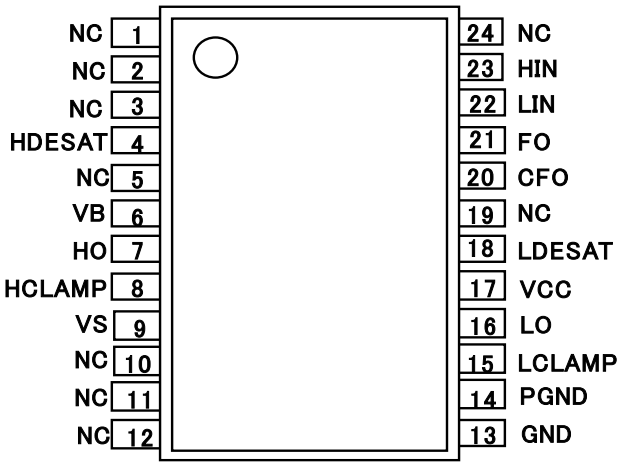
FEATURES

- ●Floating supply voltage up to 1200V
- ●Low quiescent power supply current
- ●Separate sink and source current output up to ±2A (typ)
- ●Active Miller clamp NMOS with sink current up to 2A (typ)
- ●Input noise filters (HIN,LIN,FO)
- ●Desat detection and protection with output soft shutdown
- ●Under voltage lockout
- ●Synchronization signal to synchronize shutdown with other phases
- ●24-Lead SSOP PACKAGE

APPLICATIONS

Power MOSFET and IGBT gate driver for Medium and Micro inverter or general purpose.

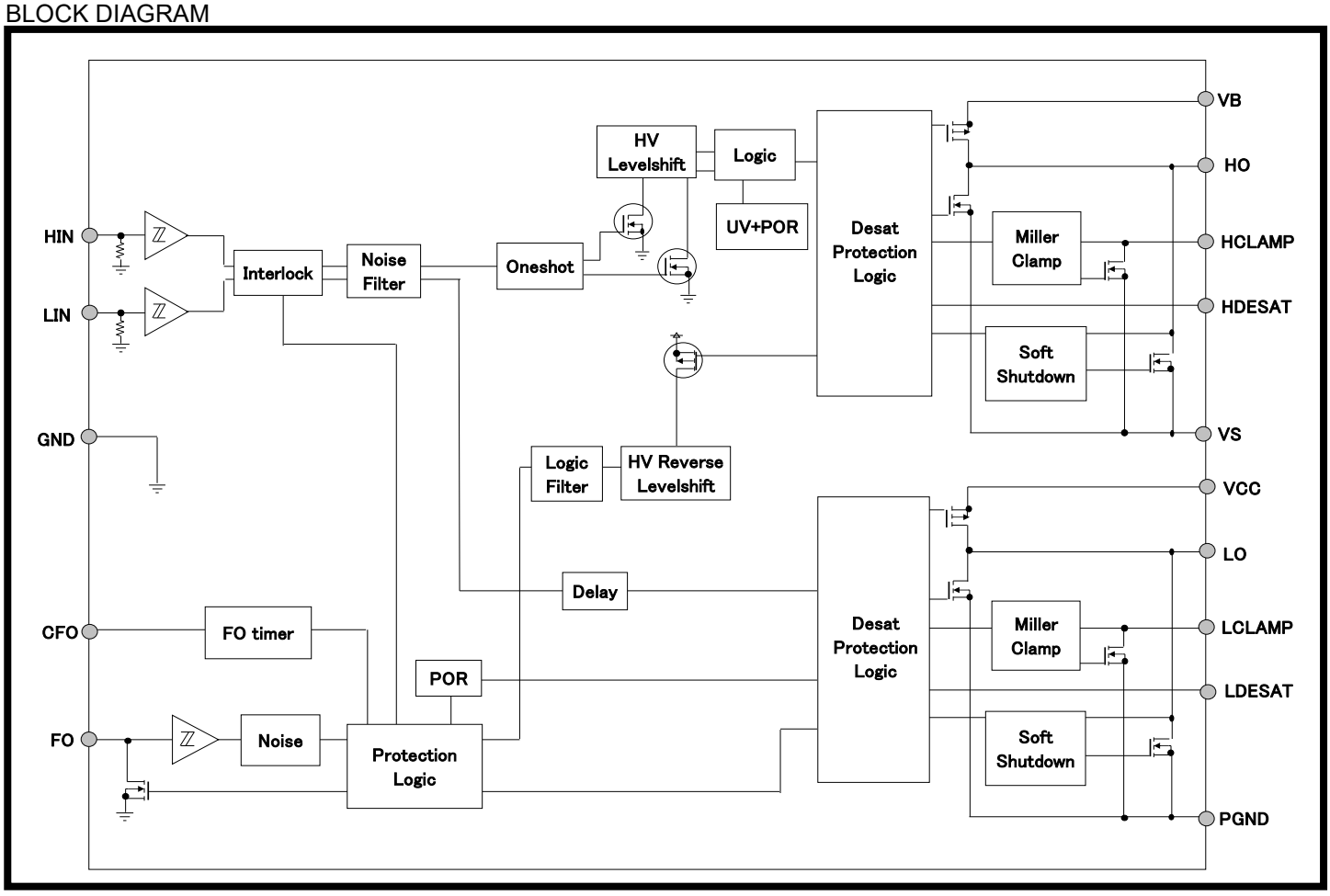
PIN CONFIGURATION (TOP VIEW)



Outline:SSOP24

NC:NO CONNECTION

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings indicate limitation beyond which destruction of device may occur. All voltage parameters are absolute voltage reference to GND unless otherwise specified.

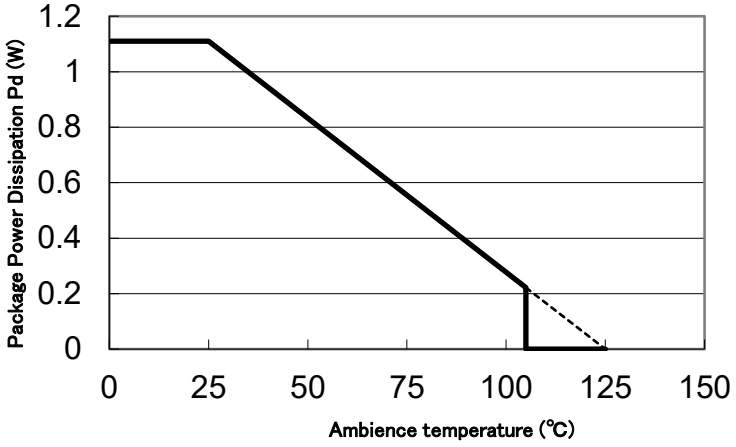
Symbol	Parameter	Test conditions	Raitings	Unit
V_B	High side floating supply absolute voltage		-0.5～1224	V
V_S	High side floating supply offset voltage		V_B -24～V_B +0.5	V
V_{BS}	High side floating supply voltage	$V_{BS}=V_B-V_S$	-0.5～24	V
V_{HO}	High side output voltage		V_S -0.5～V_B +0.5	V
V_{HCLAMP}	High side CLAMP input/output voltage		V_S -0.5～V_B +0.5	V
V_{HDESAT}	High side DESAT input/otuput voltage		V_S -0.5～V_B +0.5	V
V_{CC}	Low side fixed supply voltage		-0.5～24	V
V_{LO}	Low side output voltage		-0.5～V_{CC} +0.5	V
V_{LCLAMP}	Low side CLAMP input/output voltage		-0.5～V_{CC} +0.5	V
V_{LDESAT}	Low side DESAT input/output voltage		-0.5～V_{CC} +0.5	V
V_{IN}	Logic input voltage	HIN, LIN	-0.5～V_{CC} +0.5	V
V_{FO}	FO input/output voltage		-0.5～V_{CC} +0.5	V
dV_S/dt	Allowable offset voltage slew rate	V_S –GND and PGND	±50	V/ns
Pd	Package power dissipation	Ta= 25°C ,On our standard PCB	～1.11	W
Kq	Linear derating factor	Ta≧25°C ,On our standard PCB	～11.1	mW/℃
Rth(j-a)	Junction-ambient air thermal resistance	On our standard PCB	～90	℃/W
Tj	Junction temperature		-40～125	℃
Topr	Operation temperature		-40～105	℃
Tstg	Storage temperature	On PCB	-55～150	℃
TL	Solder reflow condition	Pb-free	255:10s, max260	℃

RECOMMENDED OPERATING CONDITIONS

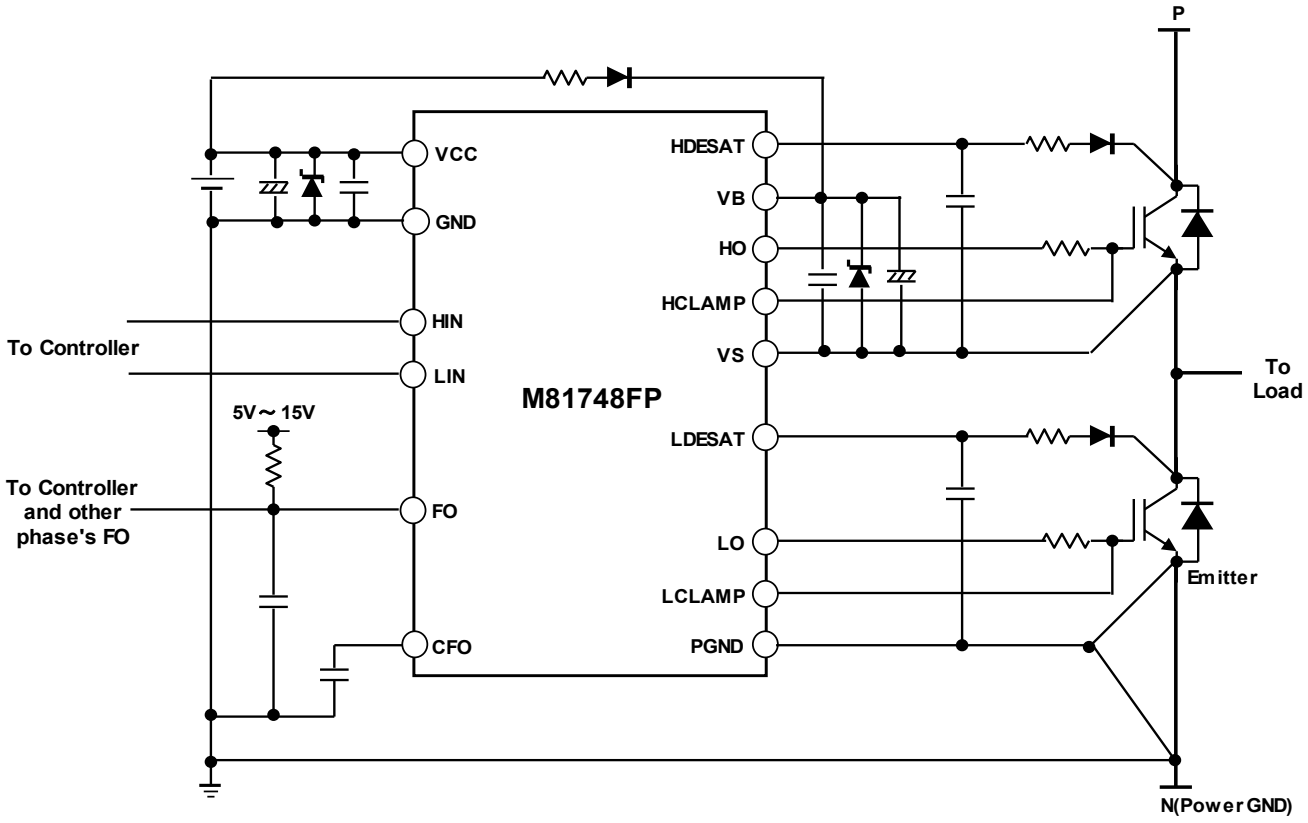
For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND unless otherwise specified.

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_B	High side floating supply absolute voltage		V_S+13.5	V_S+15	V_S+20	V
V_S	High side floating supply offset voltage	V_{BS}> 13.5V	-5	-	900	V
V_{BS}	High side floating supply voltage	$V_{BS}=V_B-V_S$	13.5	15	20	V
V_{HO}	High side output voltage		V_S	-	V_S+20	V
V_{HCLAMP}	High side CLAMP input/output voltage		V_S	-	V_S+20	V
V_{HDESAT}	High side DESAT input/output voltage		V_S	-	V_S+20	V
V_{CC}	Low side fixed supply voltage		13.5	15	20	V
V_{LO}	Low side output voltage		0	-	V_{CC}	V
V_{LCLAMP}	Low side CLAMP input/output voltage		0	-	V_{CC}	V
V_{LDESAT}	Low side DESAT input/otuput voltage		0	-	V_{CC}	V
V_{IN}	Logic input voltage	HIN, LIN,	0	-	V_{CC}	V
V_{FO}	FO input/output voltage		0	-	V_{CC}	V

THERMAL DERATING FACTOR CHARACTERISTIC (MAXIMUM RATING)



TYPICAL CONNECTION



Note: If HVIC is working in high noise environment, it is recommended to connect a 1nF ceramic capacitor to FO pin.
It is recommended to connect PGND pin to Emitter and Power GND(N). If PGND pin is not connected to Power GND(N), please pay attention to a noise between PGND pin and Power GND(N).

ELECTRICAL CHARACTERISTICS (Ta=25℃, VCC=VBS (=VB–VS)=15V, unless otherwise specified)

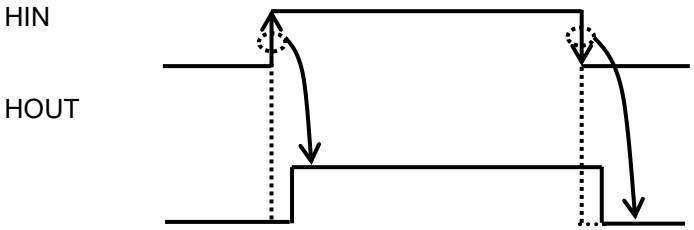
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{FS}	High side leakage current	V_B = V_S = 1200V	-	-	10	uA
I_{BS}	V_{BS} quiescent supply current	HIN = LIN = 0V	-	0.7	1.4	mA
I_{CC}	V_{CC} quiescent supply current	HIN = LIN = 0V	-	1.2	2.4	mA
V_{OH}	High level output voltage	I_O = 20mA, HO, LO	14.5	-	-	V
V_{OL}	Low level output voltage	I_O = -20mA, HO, LO	-	-	0.5	V
V_{IH}	High level input threshold voltage	HIN, LIN	4.0	-	-	V
V_{IL}	Low level input threshold voltage	HIN, LIN	-	-	1.0	V
I_{IH}	High level input bias current	V_{IN} = 5V	0.6	1.0	1.4	mA
I_{IL}	Low level input bias current	V_{IN} = 0V	0.00	0.00	0.01	mA
tFilter	Input signals filter time	HIN on-pulse	100	-	500	ns
		HIN off-pulse	100	-	500	ns
		LIN on-pulse	100	-	500	ns
		LIN off-pulse	100	-	500	ns
		FO off-pulse	100	-	500	ns
V_{HCT}	High side active Miller clamp NMOS input threshold voltage	V_{IN} = 0V	-	3.0	4.0	V
V_{LCT}	Low side active Miller clamp NMOS input threshold voltage	V_{IN} = 0V	-	3.0	4.0	V
T_W	Active Miller clamp NMOS filter time	V_{IN} = 0V	-	400	-	ns
V_{OLFO}	Low level FO output voltage	I_{FO} = 1mA	-	-	0.4	V
V_{IHFO}	High level FO input threshold voltage		4.0	-	-	V
V_{ILFO}	Low level FO input threshold voltage		-	-	1.0	V
V_{BSuvr}	V_{BS} supply UV reset voltage		10.5	11.5	12.5	V
V_{BSuvt}	V_{BS} supply UV trip voltage		9.7	10.7	11.7	V
V_{BSuvh}	V_{BS} supply UV hysteresis voltage	V_{BSuvh} = V_{BSuvr}-V_{BSuvt}	0.4	0.8	-	V
tV_{BSuv}	V_{BS} supply UV filter time		4	8	16	us
V_{LPOR}	Low side VCC POR trip voltage		7.0	9.0	11.0	V
I_{OH}	Output high level short circuit pulsed current	HO(LO) = 0V, V_{IN} = 5V, PW ≦ 10us	1.6	2.0	-	A
I_{OL1}	Output low level short circuit pulsed current	HO(LO) = 15V, V_{IN} = 0V, PW ≦ 10us	-1.6	-2.0	-	A
I_{OL2}	Active Miller clamp NMOS output low level short circuit pulsed current	HCLAMP(LCLAMP) = 15V, V_{IN} = 0V, PW ≦ 10us	-1.6	-2.0	-	A
tdLH(HO)	High side turn-on propagation delay	HO short to HCLAMP, CL = 1nF	0.7	1.0	1.3	us
tdHL(HO)	High side turn-off propagation delay	HO short to HCLAMP, CL = 1nF	0.7	1.0	1.3	us
tdLH(LO)	Low side turn-on propagation delay	LO short to LCLAMP, CL = 1nF	0.7	1.0	1.3	us
tdHL(LO)	Low side turn-off propagation delay	LO short to LCLAMP, CL = 1nF	0.7	1.0	1.3	us
tr	Output turn-on rise time	CL = 1nF	5	20	40	ns
tf	Output turn-off fall time	CL = 1nF	5	20	40	ns
DtdLH	Delay matching, high side turn-on and low side turn-off	tdLH(HO)-tdHL(LO)	-0.15	0.00	0.15	us
DtdHL	Delay matching, high side turn-off and low side turn-on	tdLH(LO)-tdHL(HO)	-0.15	0.00	0.15	us
I_{CHG}	Blanking Capacitor Charging Current	V_{DESAT} = 2V	-0.13	-0.24	-0.33	mA
I_{DSCHG}	Blanking Capacitor Discharge Current	V_{DESAT} = 7V	10	30	-	mA
V_{DESAT}	DESAT Threshold		6	6.5	7.5	V
$t_{DESAT(90\%)}$	DESAT Sense to 90%VO Delay	CL = 1nF	-	0.17	0.34	us
$t_{DESAT(10\%)}$	DESAT Sense to 10%VO Delay	CL= 1nF	-	0.30	0.60	us
$t_{DESAT(FAULT)\_H}$	HDESAT Sense to Low Level FAULT Signal Delay	R_F = 15kΩ	-	0.40	0.50	us
$t_{DESAT(FAULT)\_L}$	LDESAT Sense to Low Level FAULT Signal Delay	R_F = 15kΩ	-	0.25	0.50	us
$t_{DESAT(LOW)}$	DESAT Sense to DESAT Low Propagation Delay	C_{DESAT} = 1nF	-	0.25	-	us
t_{FO}	FO timer	CFO=1nF	-	110	-	us

Note: Typ is not specified

FUNCTION TABLE (Q: Keep previous status)

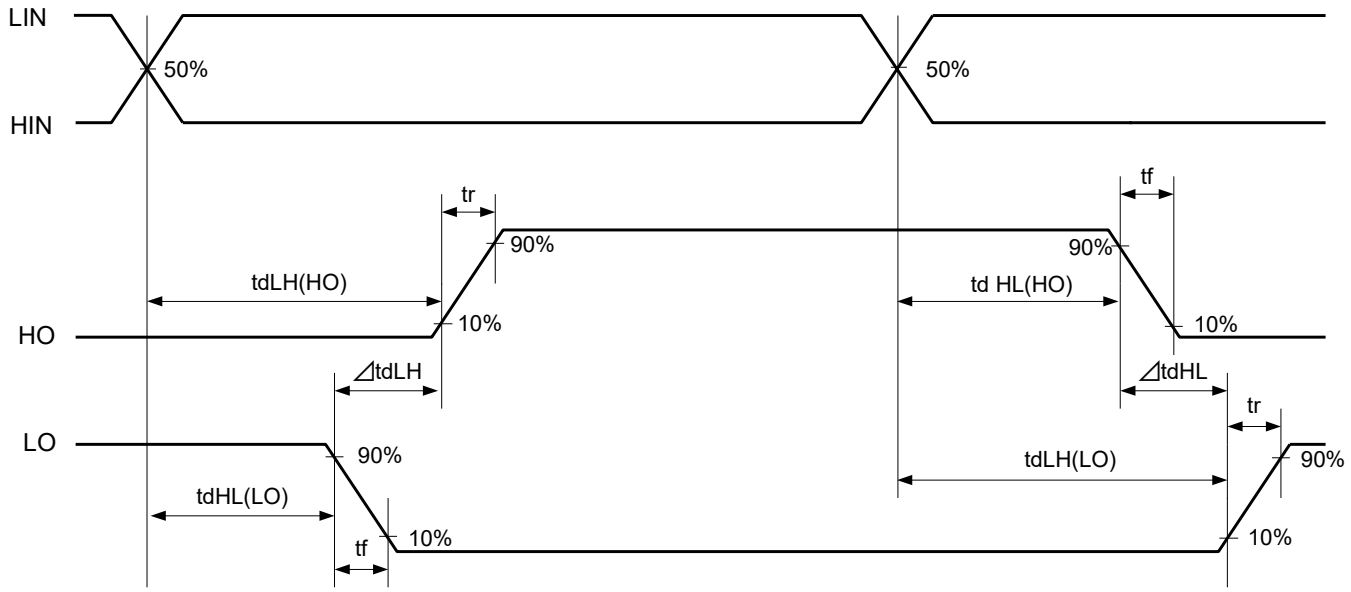
HIN	LIN	FO (Input)	HDESAT	LDESAT	V_{BS}/ UV	HO	LO	FO (Output)	Behavioral status
L	L	-	L	L	H	L	L	H	
L	H	-	L	L	H	L	H	H	
H	L	-	L	L	H	H	L	H	
H	H	-	L	L	H	L	L	H	Interlock active
H	X	-	H	X	H	L	L	L	Hige side DESAT
X	H	-	X	H	H	L	L	L	Low side DESAT
X	X	L	X	X	X	L	L	-	Output shuts down when FO = L
X	H	-	L	L	L	L	H	H	V_{BS} power reset is tripping when LIN = H

Note1 : "L" status of VBS/UV indicates a high side UV condition.
Note2 : In the case of both input signals (HIN and LIN) are "H", output signals (HO and LO) keep previous status.
Note3 : X (HIN) : L→H or H→L. Other : H or L.
Note4 : Output signal (HO) is triggered by the edge of input signal.
Note5 : Please see FUNCTIONAL DESCRIPTION 7(p.8) for detailed sequences of desaturation



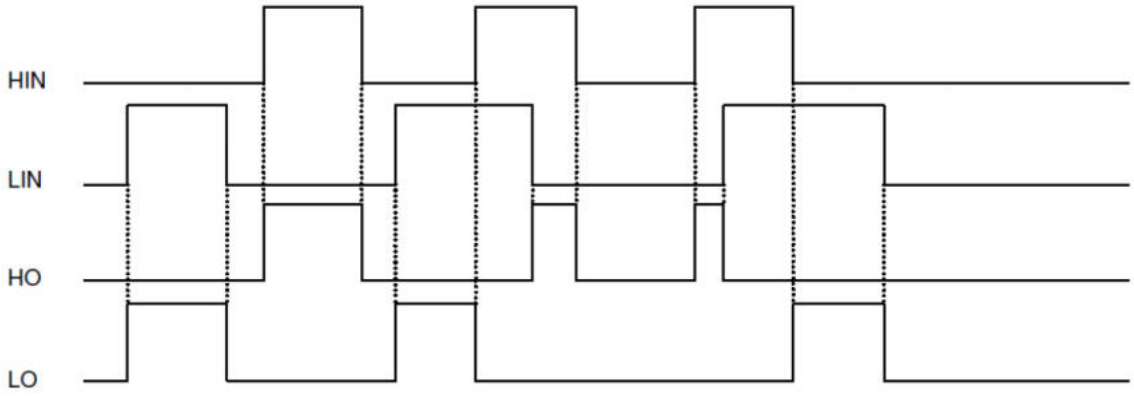
FUNCTIONAL DESCRIPTION

1. INPUT/OUTPUT TIMING DIAGRAM



2. INPUT/OUTPUT TIMING DIAGRAM

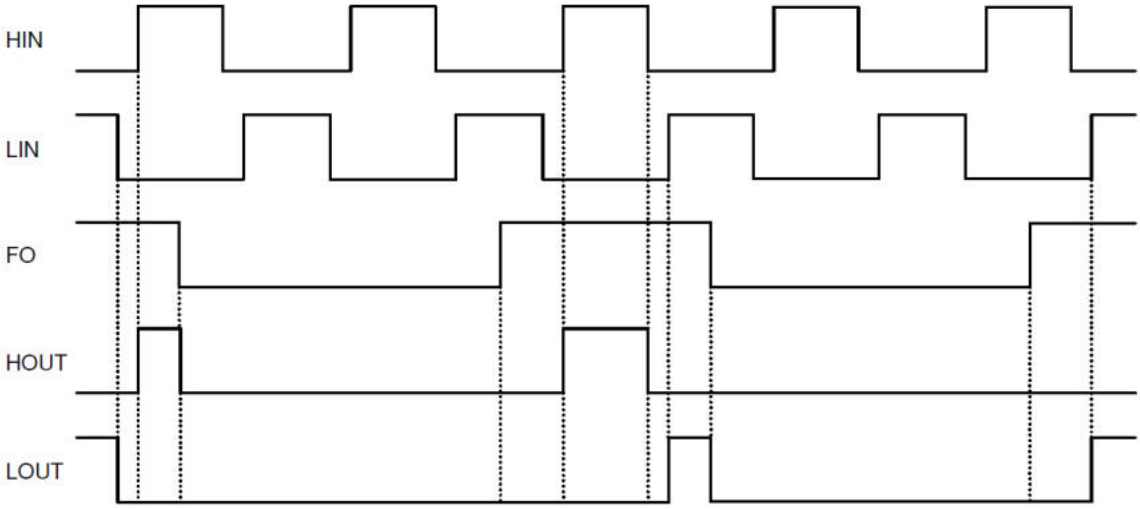
When the input signals (HIN/LIN) are high level at the same time, the outputs (HO/LO) shuts down.



Note1 : The minimum input pulse width at HIN/LIN should be to more than 500ns (because of HIN/LIN input noise filter circuit).
Note2 : Delay times between input and output signals are not shown in the figure above.

3. FO INPUT TIMING DIAGRAM

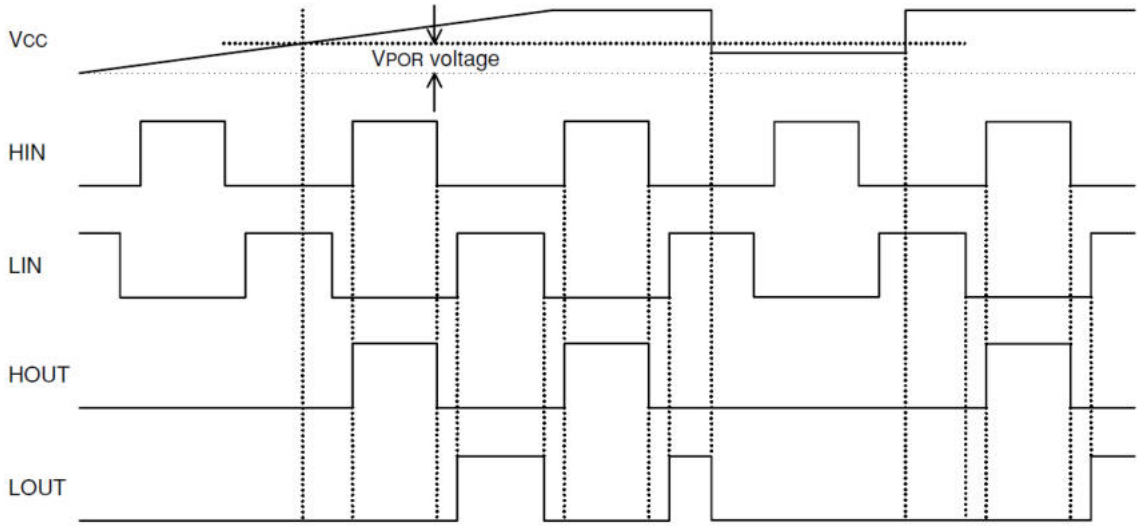
When FO is pulled down to low level in case the FO of other phases becomes low level (fault happened) or the MCU/DSP sets FO to low level, the outputs (HOUT, LOUT) of the driver will be shut down. As soon as FO goes high again, the output will respond to the following active input signal.



Note1 : Delay times between input and output signals are not shown in the figure above.
Note2 : The minimum FO pulse width should be more than 500ns (because of FO input filter circuit).

4. LOW SIDE VCC SUPPLY POWER RESET SEQUENCE

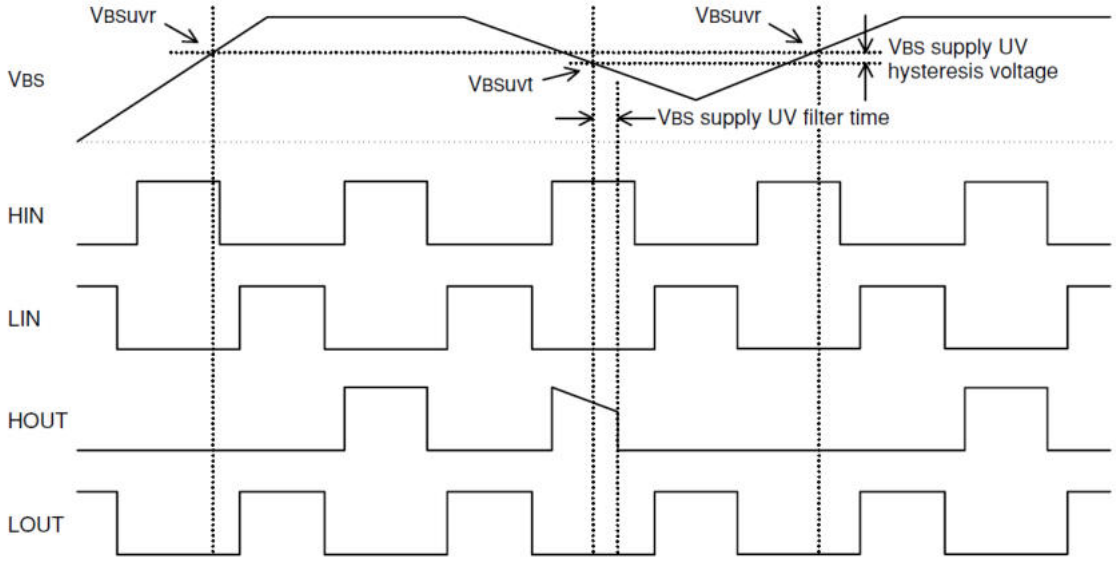
When the VCC supply voltage is lower than power reset trip voltage, the power reset gets active and the outputs (LOUT) become “L”. As soon as the VCC supply voltage goes higher than the power reset trip voltage, the outputs will respond to the following active input signals.



Note1 : Delay times between input and output signals are not shown in the figure above

5. HIGH SIDE VBS SUPPLY UNDER VOLTAGE LOCKOUT SEQUENCE

When VBS supply voltage drops below the VBS supply UV trip voltage and the duration in this status exceeds the VBS supply UV filter time, the output of the high side is locked. As soon as the VBS supply voltage rises above the VBS supply UV reset voltage, the output will respond to the following active HIN signal.

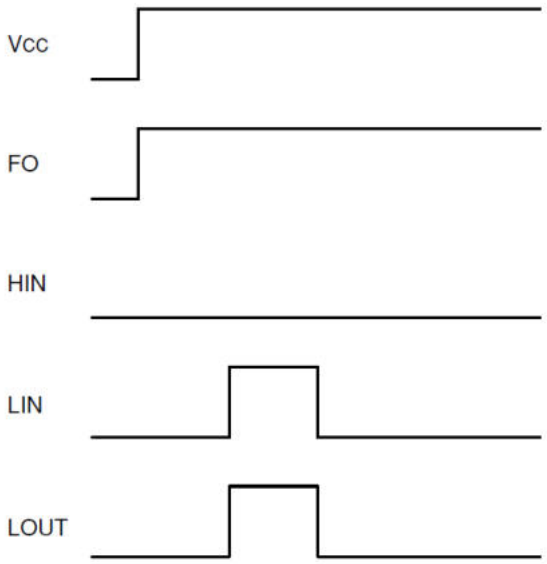


Note1 : Delay times between input and output signals are not shown in the figure above.

6. POWER START-UP SEQUENCE

At power supply start-up the following sequence is recommended when bootstrap supply topology is used.

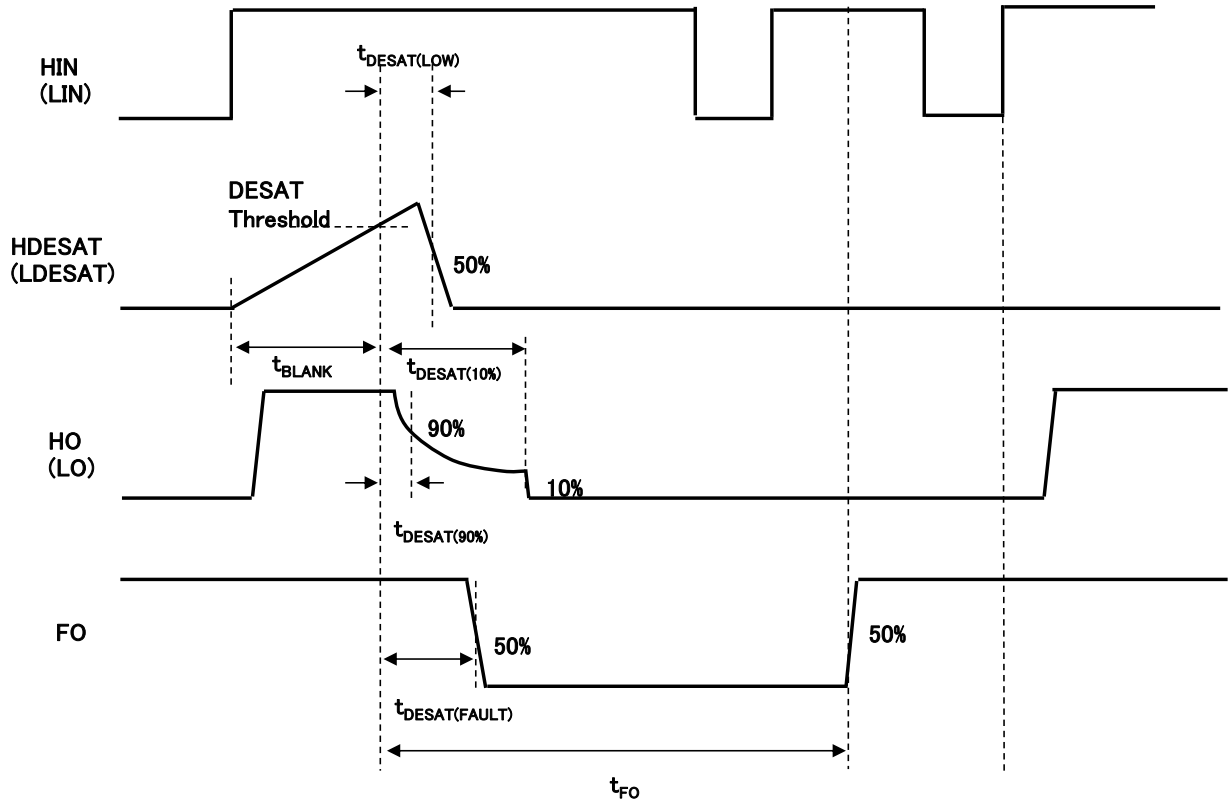
① Apply VCC.
② Make sure that FO is at high level.
③ Set LIN to high level and HIN to low level so that bootstrap capacitor could be charged.
④ Set LIN to low level.



Note : If two power supply are used for supplying VCC and VBS individually, it is recommended to set VCC first and then set VBS.

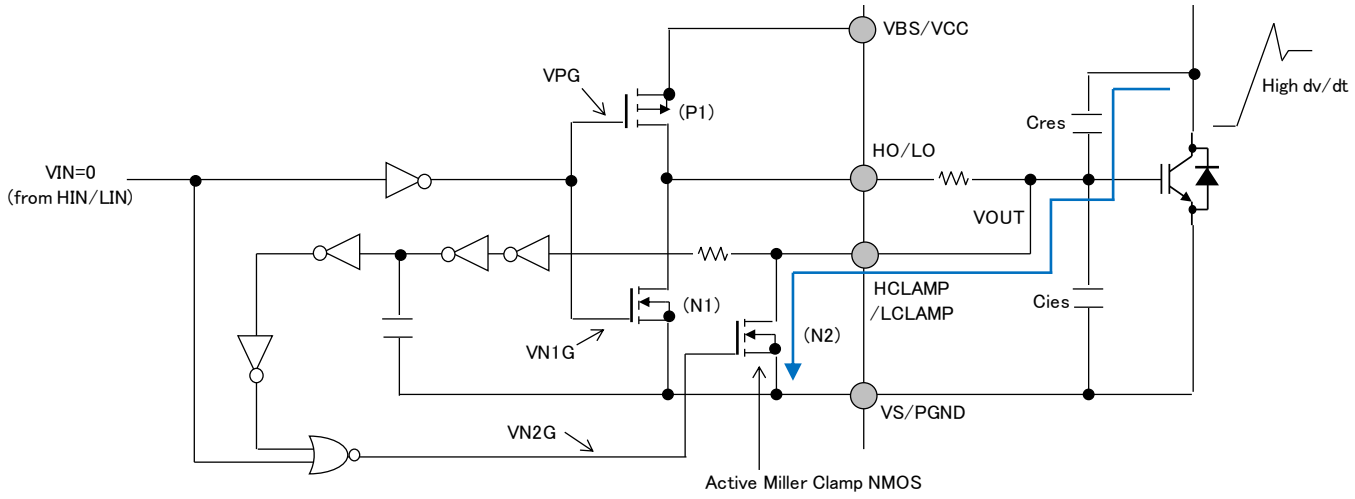
7. DESATURATION DETECTION AND HIGH CURRENT PROTECTION

HDESAT(LDESAT) detects the IGBT Vce voltage. When the IGBT is ON and the DESAT voltage exceeds DESAT threshold voltage, HO(LO) output slowly falls to a low level to softly turn-off the IGBT and prevent high di/dt noises. And FO output falls to a low level to transmit the fault signal to the micro controller. Once the fault condition is detected, all input signals are ignored during the tFO period to complete the soft shutdown.

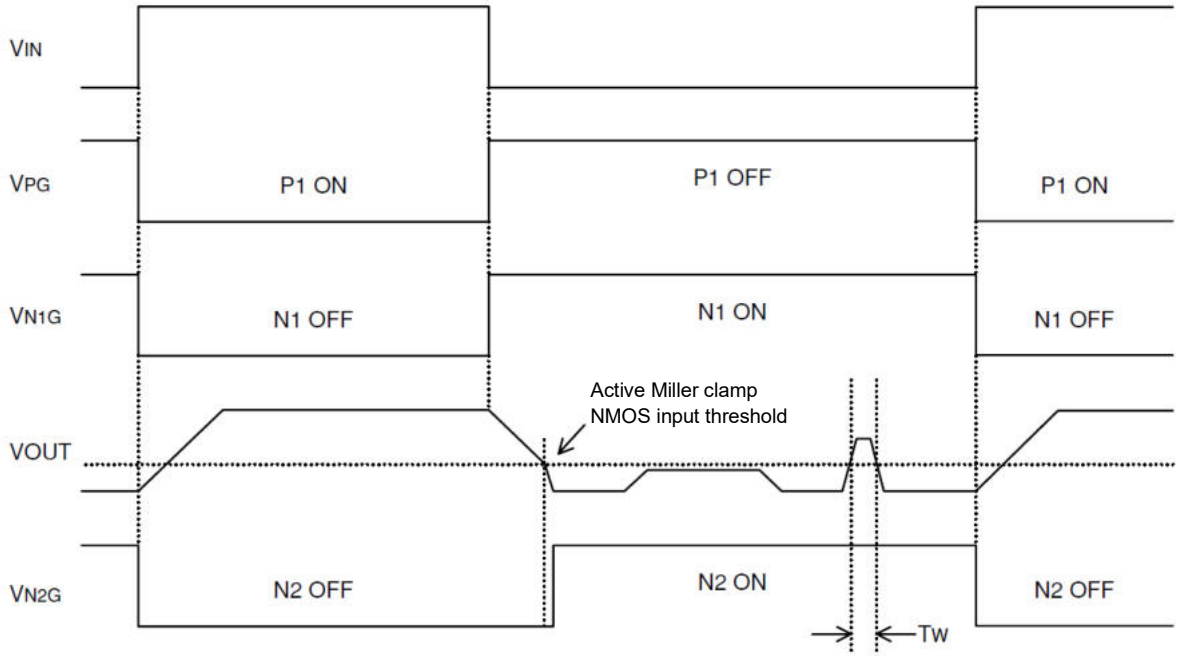


8. ACTIVE MILLER CLAMP NMOS OUTPUT TIMING DIAGRAM

The structure of the output driver stage is shown in following figure. This circuit structure employs a solution for the problem of the Miller current through Cres in IGBT switching applications. Instead of driving the IGBT gate to a negative voltage to increase the safety margin, this circuit structure uses a NMOS to establish a low impedance path to prevent the self-turn-on due to the parasitic Miller capacitor in power switches.

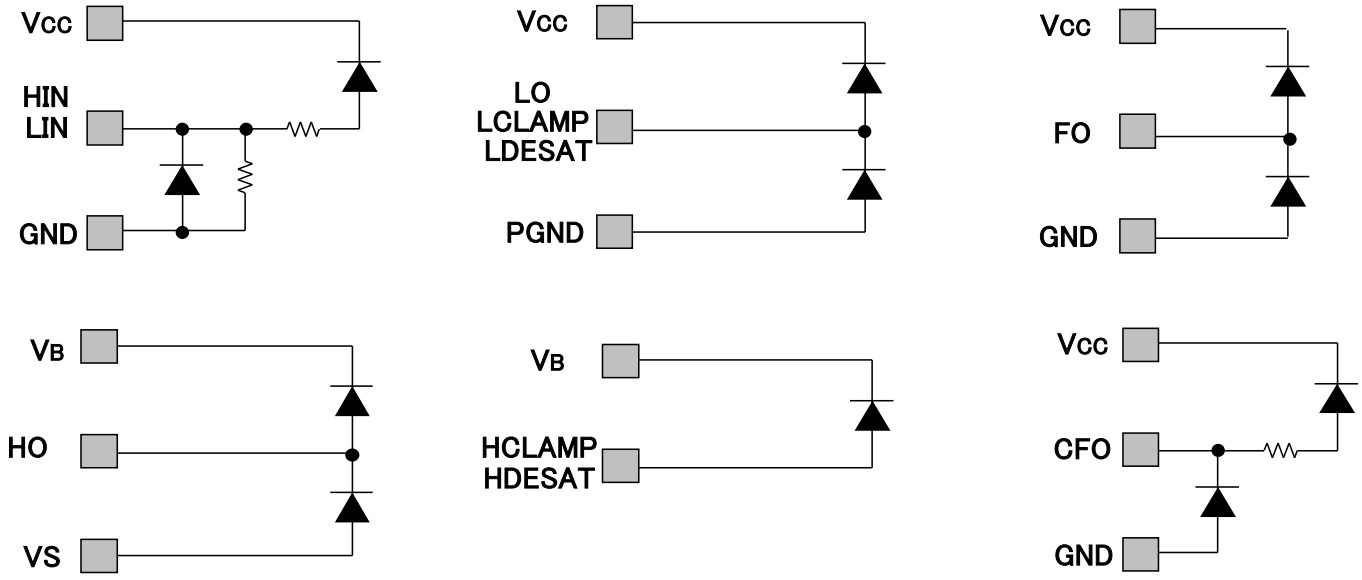


When HIN/LIN is at low level and the voltage of the VOUT (IGBT gate voltage) is below active Miller clamp NMOS input threshold voltage, the active Miller clamp NMOS is being turned on and opens a low resistive path for the Miller current through Cres.



Active Miller clamp NMOS keeps turn-on if Tw does not exceed active Miller clamp NMOS filter time

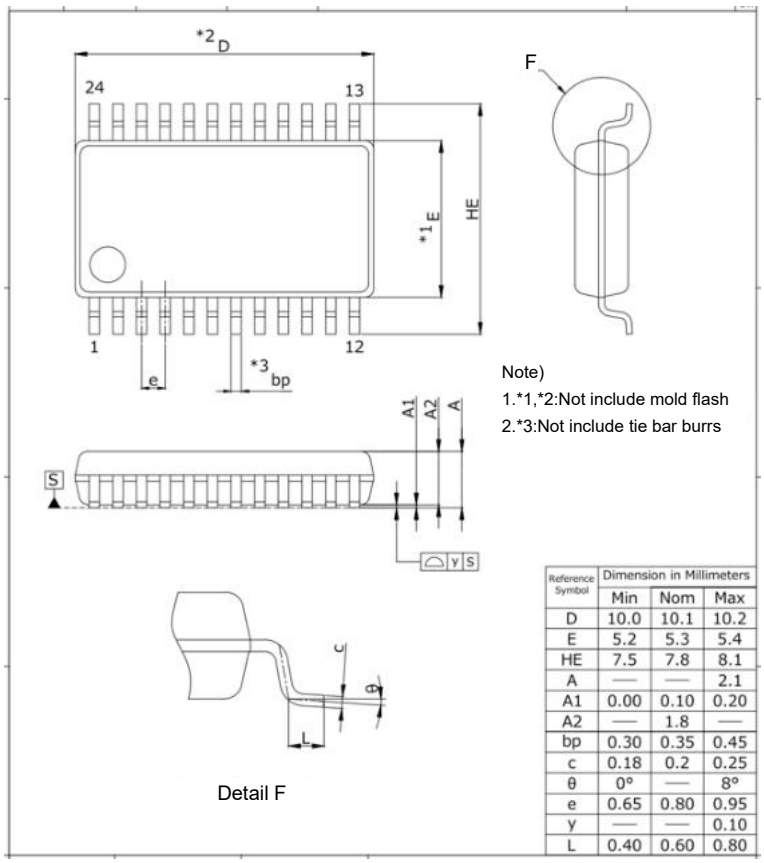
INTERNAL DIODE CLAMP CIRCUITS FOR INPUT AND OUTPUT



ENVIRONMENTAL CONSCIOUSNESS

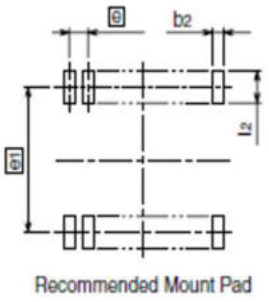
M81748FP is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU+(EU)2015/863.

PACKAGE OUTLINE



Note)
1.*1,*2:Not include mold flash
2.*3:Not include tie bar burrs

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
HE	7.5	7.8	8.1
A	—	—	2.1
A1	0.00	0.10	0.20
A2	—	1.8	—
bp	0.30	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
e	0.65	0.80	0.95
y	—	—	0.10
L	0.40	0.60	0.80



Recommended Mount Pad

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
e1	—	7.62	—
l2	1.27	—	—
e	—	0.8	—
b2	—	0.5	—

The above is one example.
Please design the mount pad with your evaluation.

Main Revision for this Edition

Rev.	Date	Revision	
		Pages	Points
A	3 Feb. 2015	-	New making
B	22 Nov. 2016	2	RECOMMENDED OPERATING CONDITIONS: Maximum voltage of V_{BS} is changed to 20V from 16.5V. Maximum voltage of V_{CC} is changed to 20V from 16.5V.
C	28 Apr. 2021	-	Update format
D	2 Jul 2024	- 3 4	"Active Miller effect clamp." was changed to "Active Miller clamp." Removed the Zener diode between HDESAT and VS and between LDESAT and PGND. The standard value of "Active Miller clamp NMOS filter time(Tw)" has been added.

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