MITSUBISHI ELECTRIC

<HVIC>

M81749FP

600V HIGH VOLTAGE 3PHASE BRIDGE DRIVER

DESCRIPTION

M81749FP is high voltage Power MOSFET and IGBT gate driver for 3phase bridge applications.

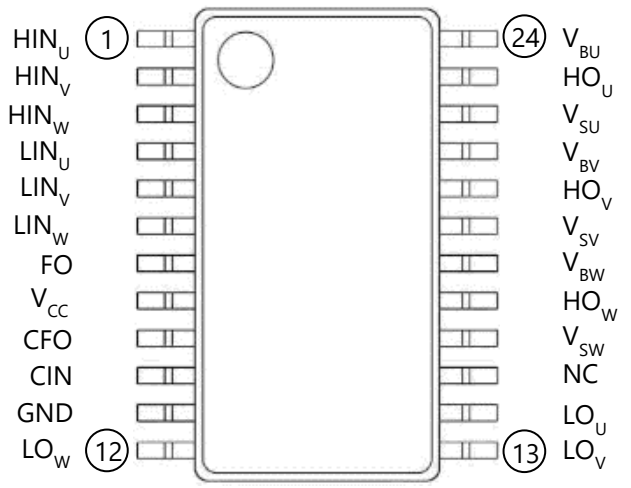
FEATURES

- ●Floating Supply Voltage ····· 600V
- ●Output Current ····· ···· +200mA/-350ma(Typ.)
- ●3Phase Bridge Driver
- ●Under Voltage (UV) Lockout
- ●Short Circuit (SC) Lockout
- ● Failure Output(FO) terminal which can output Fault signals to communicate with controllers
- ● Capacitor with a Failure-Output pulse width timer function(CFO)
- ●24-Lead SSOP PACKAGE

APPLICATIONS

MOSFET and IGBT module driver for refrigerator, air-conditioner, washing machine, AC-servomotor, inverter and general purposes.

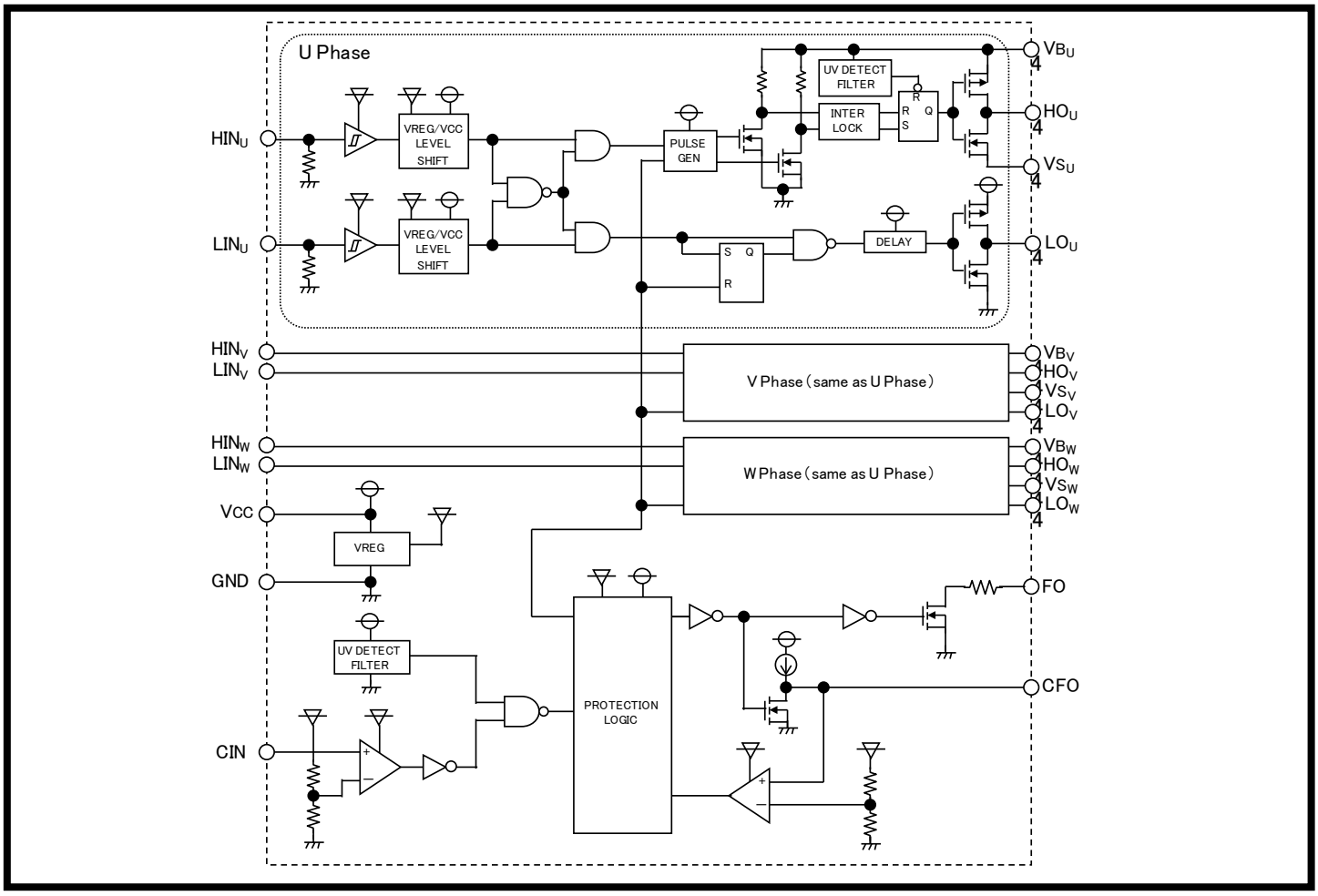
PIN CONFIGURATION (TOP VIEW)



Outline:SSOP24

NC:NO CONNECTION

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C unless otherwise specified) (* :U or V or W Phase)

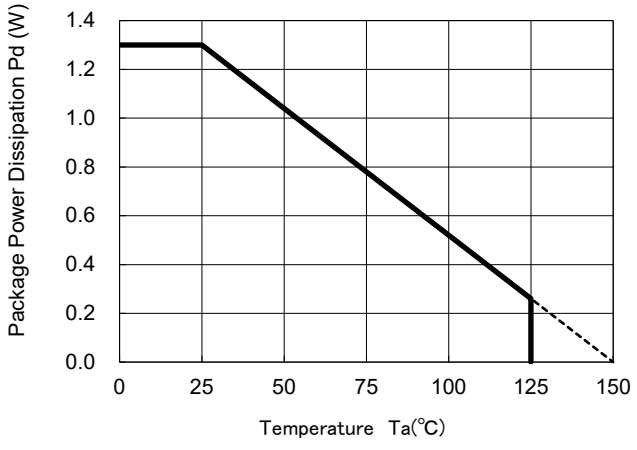
Symbol	Parameter	Test conditions	Ratings	Unit
V_{B*}	High Side Floating Supply Absolute Voltage		-0.5 ～ 624	V
V_{S*}	High Side Floating Supply Offset Voltage		V_{B*}-24 ～ V_{B*}+0.5	V
V_{BS}	High Side Floating Supply Voltage	$V_{BS}=V_{B*}-V_{S*}$	-0.5 ～ 24	V
V_{HO}	High Side Output Voltage		V_{S*}-0.5 ～ V_{B*}+0.5	V
V_{CC}	Low Side Fixed Supply Voltage		-0.5 ～ 24	V
V_{LO}	Low Side Output Voltage		-0.5 ～ Vcc+0.5	V
V_{IN}	Logic Input Voltage	HIN*,LIN* Terminal	-0.5 ～ Vcc+0.5	V
V_{FO}	FO Output Voltage	FO Terminal	-0.5 ～ Vcc+0.5	V
I_{FO}	FO Output Current	FO Terminal	0 ～ 1	mA
V_{CIN}	Current Sense Input Voltage	CIN Terminal	-0.5 ～ Vcc+0.5	V
V_{CFO}	CFO Input Voltage	CFO Terminal	-0.5 ～ Vcc+0.5	V
Pd	Package Power Dissipation	Ta= 25 °C ,On Board	1.3	W
Kθ	Linear Derating Factor	Ta> 25 °C ,On Board	10.4	mW/℃
Rth(j-c)	Junction-Case Thermal Resistance		96	℃/W
Tj	Junction Temperature		-40 ～ +150	℃
Topr	Operation Temperature		-40 ～ +125	℃
Tstg	Storage Temperature	On Board	-40 ～ +150	℃
TL	Solder Reflow Condition	Pb-free	255:10s,max 260	℃

RECOMMENDED OPERATING CONDITIONS (* :U or V or W Phase)

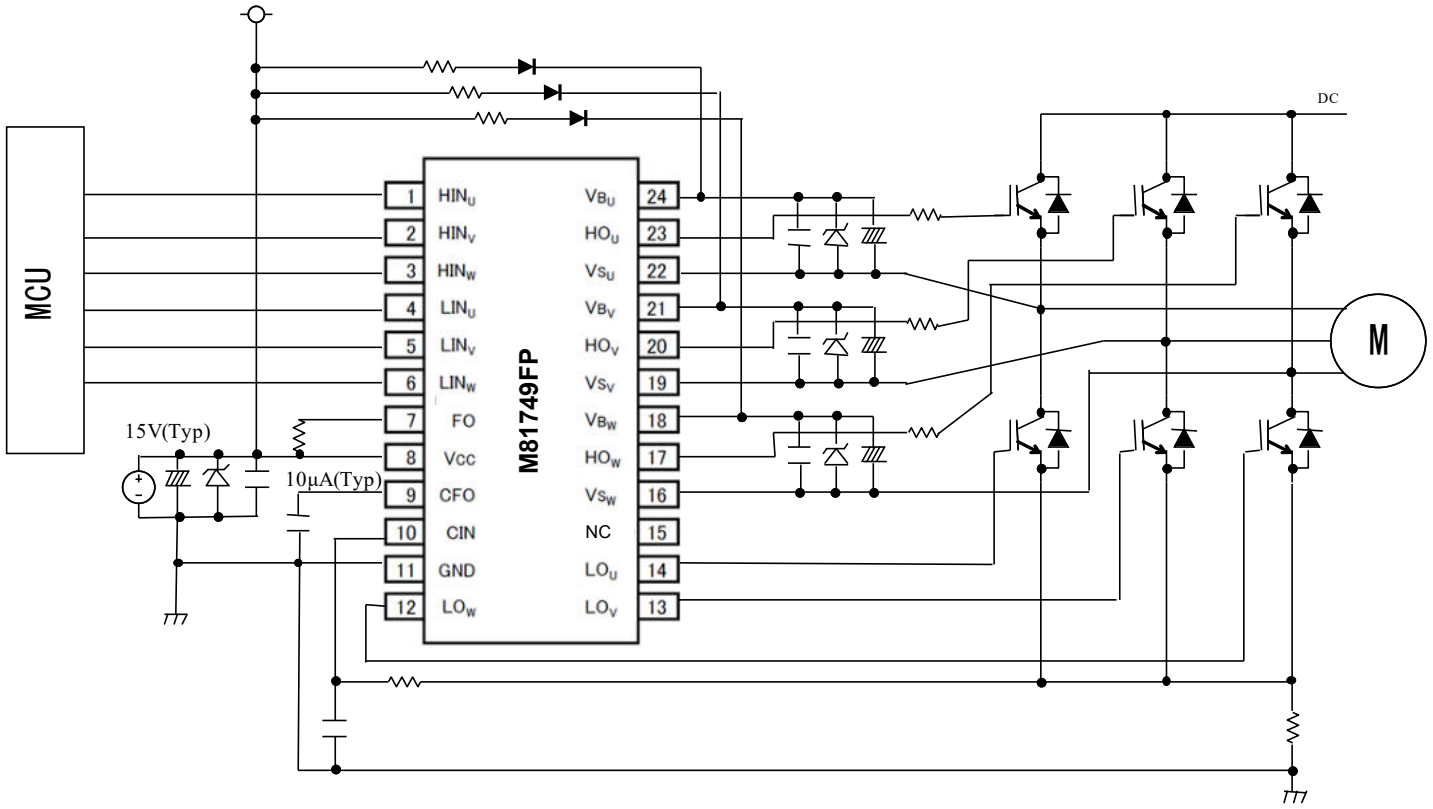
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{B*}	High Side Floating Supply Absolute Voltage		V_S+10	—	V_S+20	V
V_{S*}	High Side Floating Supply Offset Voltage	V_{B*}>10V	-5	—	500	V
V_{BS}	High Side Floating Supply Voltage	$V_{BS}=V_{B*}-V_{S*}$	10	—	20	V
V_{HO}	High Side Output Voltage		V_{S*}	—	V_{B*}	V
V_{CC}	Low Side Fixed Supply Voltage		10	—	20	V
V_{LO}	Low Side Output Voltage		0	—	V_{CC}	V
V_{IN}	Logic Input Voltage	HIN*,LIN* Terminal	0	—	V_{CC}	V
V_{FO}	FO Output Voltage	FO Terminal	0	—	V_{CC}	V
V_{CIN}	Current Sense Input Voltage	CIN Terminal	0	—	V_{CC}	V
V_{CFO}	CFO Input Voltage	CFO Terminal	0	—	V_{CC}	V

Note : For proper operation, the device should be used within the recommended conditions

THERMAL DERATING FACTOR CHARACTERISTIC (MAXIMUM RATING)



TYPICAL CONNECTION



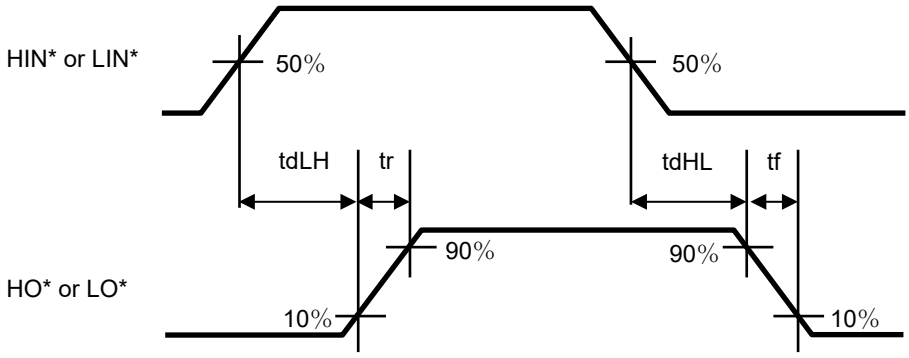
CIN : The time constant RC should be set so that SC current is shut down within the short circuit tolerance(time) of the power elements to use and shutdown time of HVIC and the power elements.

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=V_{BS}(=V_{B*}-V_{S*})=15V, unless otherwise specified) (* :U or V or W Phase)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*1	Max.	
I_{FS}	Floating Supply Leakage Current	V_{B*} = V_{S*} = 600V, Value per 1phase	—	—	1.0	uA
I_{BS}	V_{BS} Standby Current	HIN*=LIN* = 0V, Value per 1phase	—	0.2	0.5	mA
I_{CC}	V_{CC} Standby Current	HIN*=LIN* = 0V	0.5	1.0	2.0	mA
V_{OH}	High Level Output Voltage	I_O = -20mA, HO*,LO* Terminal	13.6	14.2	—	V
V_{OL}	Low Level Output Voltage	I_O = 20mA, HO*,LO* Terminal	—	0.3	0.6	V
V_{IH}	High Level Input Threshold Voltage *2	HIN*,LIN* Terminal	2.7	—	—	V
V_{IL}	Low Level Input Threshold Voltage *3	HIN*,LIN* Terminal	—	—	0.8	V
I_{IH}	High Level Input Bias Current	HIN*,LIN* = 5V	—	25	100	uA
I_{IL}	Low Level Input Bias Current	HIN*,LIN* = 0V	—	—	2.0	uA
V_{BSuvr}	V_{BS} Supply UV Reset Voltage		7.0	8.4	9.8	V
V_{BSuvt}	V_{BS} Supply UV Trip Voltage		6.5	7.85	9.0	V
V_{BSuvh}	V_{BS} Supply UV Hysteresis Voltage		0.3	0.55	—	V
t_{VBSuv}	V_{BS} Supply UV Filter Time		—	7.5	—	us
V_{CCuvr}	V_{CC} Supply UV Reset Voltage		7.0	8.4	9.8	V
V_{CCuvt}	V_{CC} Supply UV Trip Voltage		6.5	7.85	9.0	V
V_{CCuvh}	V_{CC} Supply UV Hysteresis Voltage		0.3	0.55	—	V
t_{VCCuv}	V_{CC} Supply UV Filter Time		—	7.5	—	us
I_{OH}	Output High Level Short Circuit Pulsed Current	V_O = 0V, V_{IN} = 5V, PW < 10ms *4	120	200	—	mA
I_{OL}	Output Low Level Short Circuit Pulsed Current	V_O = 15V, V_{IN} = 0V, PW < 10ms *4	250	350	—	mA
R_{OH}	Output High Level On Resistance	I_O = -20mA, R_{OH} = (V_{CC} - V_{OH}) / I_O	—	40	70	Ω
R_{OL}	Output Low Level On Resistance	I_O = 20mA, R_{OL} = V_{OL} / I_O	—	15	30	Ω
t_{dLH}(HO)	High Side Turn-On Propagation Delay	CL = 1000pF between HO*-V_{S*}	—	150	300	ns
t_{dHL}(HO)	High Side Turn-Off Propagation Delay	CL = 1000pF between HO*-V_{S*}	—	130	230	ns
t_{rH}	High Side Turn-On Rise Time	CL = 1000pF between HO*-V_{S*}	—	130	220	ns
t_{fH}	High Side Turn-Off Fall Time	CL = 1000pF between HO*-V_{S*}	—	50	80	ns
t_{dLH}(LO)	Low Side Turn-On Propagation Delay	CL = 1000pF between LO*-GND	—	150	300	ns
t_{dHL}(LO)	Low Side Turn-Off Propagation Delay	CL = 1000pF between LO*-GND	—	130	230	ns
t_{rL}	Low Side Turn-On Rise Time	CL = 1000pF between LO*-GND	—	130	220	ns
t_{fL}	Low Side Turn-Off Fall Time	CL = 1000pF between LO*-GND	—	50	80	ns
⊿tdLH	Turn-On Propagation Delay Matching	|tdLH(HO)-tdLH(LO)|	—	0	30	ns
⊿tdHL	Turn-Off Propagation Delay Matching	|tdHL(HO)-tdHL(LO)|	—	0	30	ns
V_{FOH}	FO High Level Output Voltage	V_{CIN} = 0V, FO = 10kΩ to V_{CC}	14.9	15.0	—	V
V_{FOL}	FO Low Level Output Voltage	V_{CIN} = 1.5V, I_{FO} = 1mA	—	—	0.95	V
I_{FOH}	FO Leak Current	V_{CIN} = 0V, V_{FO} = V_{CC}	—	—	1.0	uA
t_{wFOP}	FO Pulse Output Width	CFO = 22nF	7	11	15	ms
t_{SC1}	SC Shut Down Propagation Delay 1	CIN : 0V → 1.5V, CIN to OUT	400	620	900	ns
t_{SC2}	SC Shut Down Propagation Delay 2	CIN : 0V → 1.5V, CIN to FO	350	520	750	ns
t_{SC3}	SC Filter Time	CIN pulse width : 0V → 1.5V→0V to FO=H→L	100	380	—	ns
V_{SC}	SC Trip Voltage	CIN voltage at FO:H→L	0.8	1.0	1.2	V
V_{CFOT}	CFO Threshold Voltage		4.5	5.0	5.5	V
I_{CFO}	CFO Source Current	CFO = 0V	-14	-10	-7	uA

*1 Typ. is not specified.
*2 Please set High level input voltage more than the minimum value of limits.
*3 Please set Low level input voltage less than the maximum value of limits.
*4 The short circuit pulse cannot be continuously.

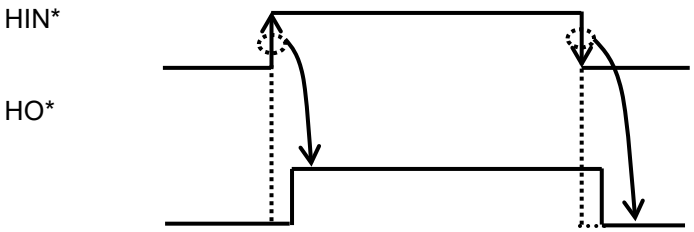
INPUT/OUTPUT TIMING DIAGRAM (* :U or V or W Phase)



FUNCTION TABLE (* :U or V or W Phase)

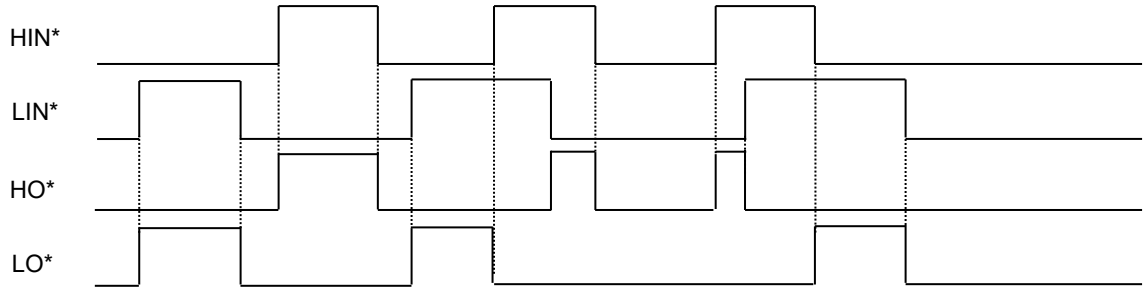
HIN*	LIN*	V_{BS}UV	V_{CC}UV	CIN	HO*	LO*	FO	Behavioral state
H→L	L	H	H	L	L	L	H	HO* = L, LO* = L
H→L	H	H	H	L	L	H	H	LO* = H
L→H	L	H	H	L	H	L	H	HO* = H
L→H	H	H	H	L	L	L	H	HO* = L, LO* = L when HIN*=LIN=H
X	L	L	H	L	L	L	H	HO* = L when V_{BS}UV is detected
H→L	H	L	H	L	L	H	H	LO* = H when V_{BS}UV is detected
L→H	H	L	H	L	L	L	H	HO* = L, LO* = L when HIN*=LIN=H and V_{BS}UV is detected
H→L	X	H	L	L	L	L	L	LO* = L when V_{CC}UV is detected
L→H	X	H	L	L	L	L	L	HO* = L,LO* = L when V_{CC}UV is detected
X	X	X	X	H	L	L	L	HO* = L,LO* = L when SC is detected

Note1 : “L” state of VBS UV, VCC UV means that VCC (VBS) Supply become under UV trip voltage.
Note2 : “H” state of CIN means that CIN become SC trip voltage.
Note3 : In the case of both input signals (HIN* and LIN*) are “H”, output signals (HO* and LO*) become “L”.
Note4 : X (HIN*) : L→H or H→L. X (LIN*) : H or L.
Note5 : Output Signal (HO*) is triggered by the edge of input signal.



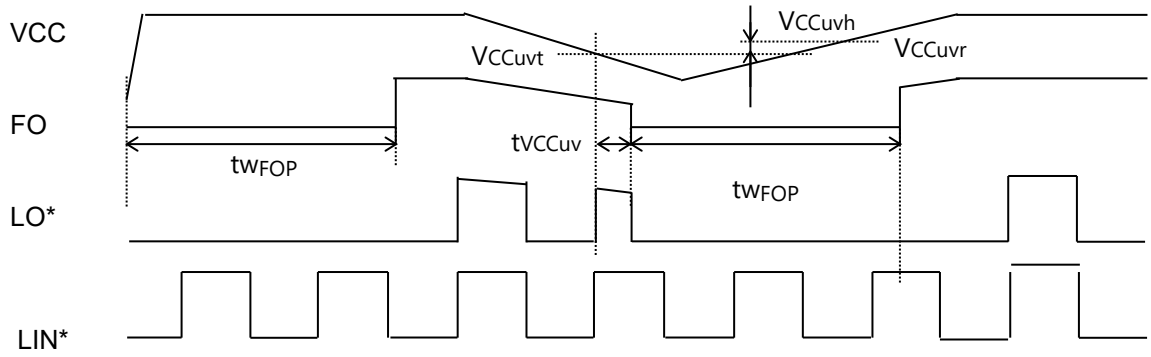
FUNCTION TIMING DIAGRAM (* :U or V or W Phase)

1. Input/Output Timing Diagram
High Active, in the case of both input signals (HIN*, LIN*) are “H”, output signals (HO*, LO*) become “L”.

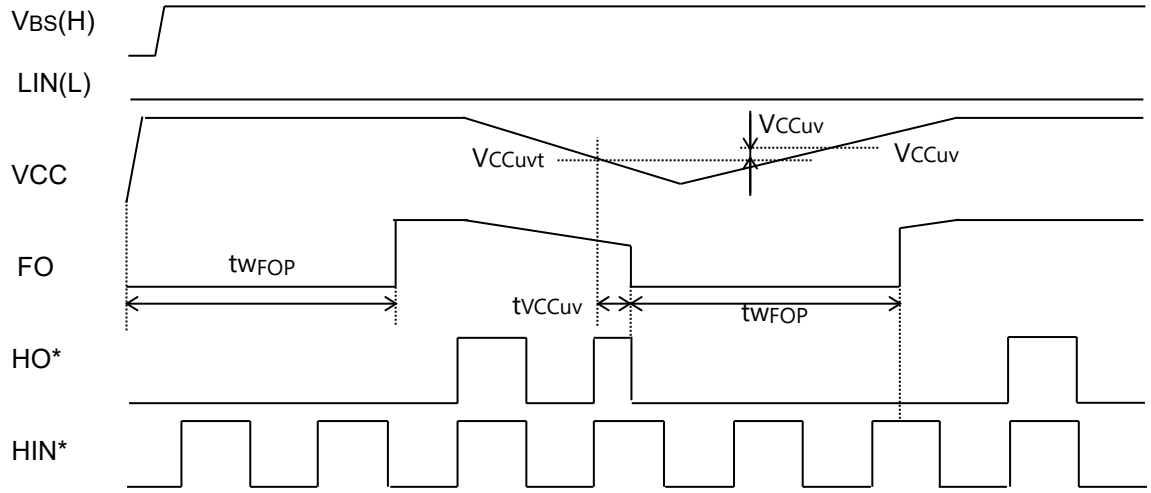


2. V_{CC} (V_{BS}) Supply Under Voltage (UV) Lockout Timing Diagram

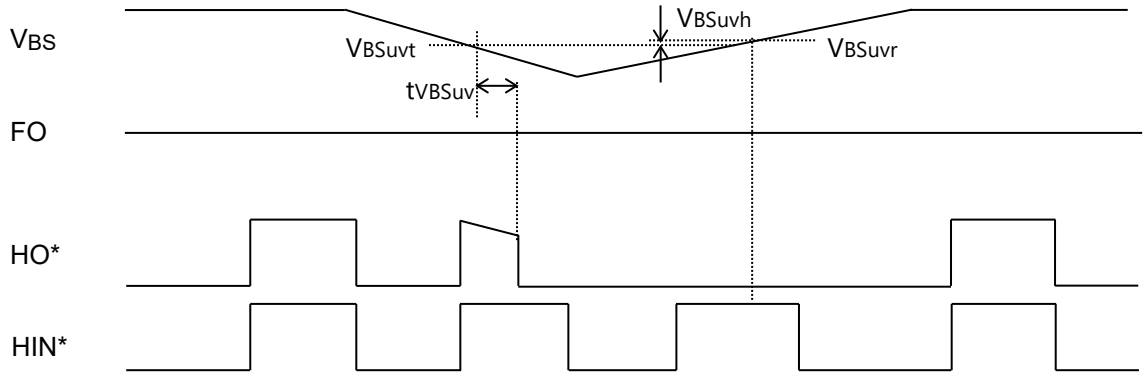
If V_{CC} supply voltage drops below UV trip voltage (V_{CC}uvt) for V_{CC} supply UV filter time, FO output signal become “L” and LO* output signal is shut down.
And then, if V_{CC} supply voltage rises over UV reset voltage and longer than FO Pulse Output Width , FO output signal become “H” and LO* output signal will respond to the next active LIN* signal(L→H). (same as power supply start-up sequence)



If V_{CC} supply voltage drops below UV trip voltage (V_{CC}uvt) for V_{CC} supply UV filter time, FO output signal become “L” and HO* output signal is shut down.
And then, if V_{CC} supply voltage rises over UV reset voltage and longer than FO Pulse Output Width, FO output signal become “H” and HO* output signal will respond to the next active HIN* signal(L→H). (same as power supply start-up sequence)
(LIN*=“L”, V_{CC}>V_{BS})

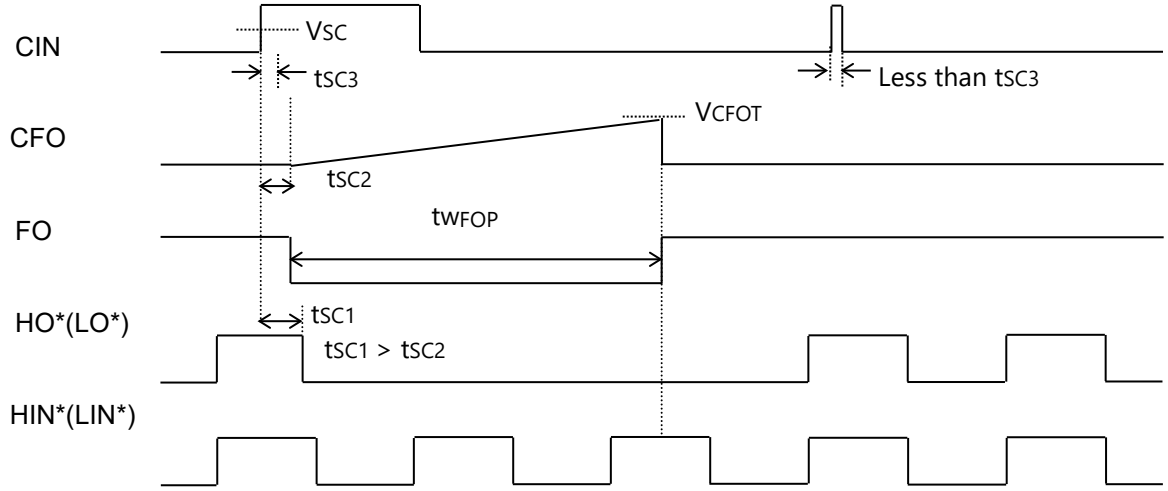


If V_{BS} supply voltage drops below UV trip voltage (V_{BS}uvt) for V_{BS} supply UV filter time, HO* output signal is shut down.
And then, if V_{BS} supply voltage rises over UV reset voltage, HO* output signal will respond to the next active HIN* signal(L→H).
During this period, FO output signal keeps “H”.



3. Short Circuit (SC) Lockout Timing Diagram

If CIN terminal voltage keeps higher than SC trip voltage (V_{SC}) for SC filter time, FO output signal become “L” and HO* (or LO*) output signal is shut down.
And then, if CIN terminal voltage is lower than SC trip voltage and longer than FO Pulse Output Width, FO output signal become “H” and HO*(or LO*) output signal will respond to the next active HIN* (LIN*) signal(L→H).



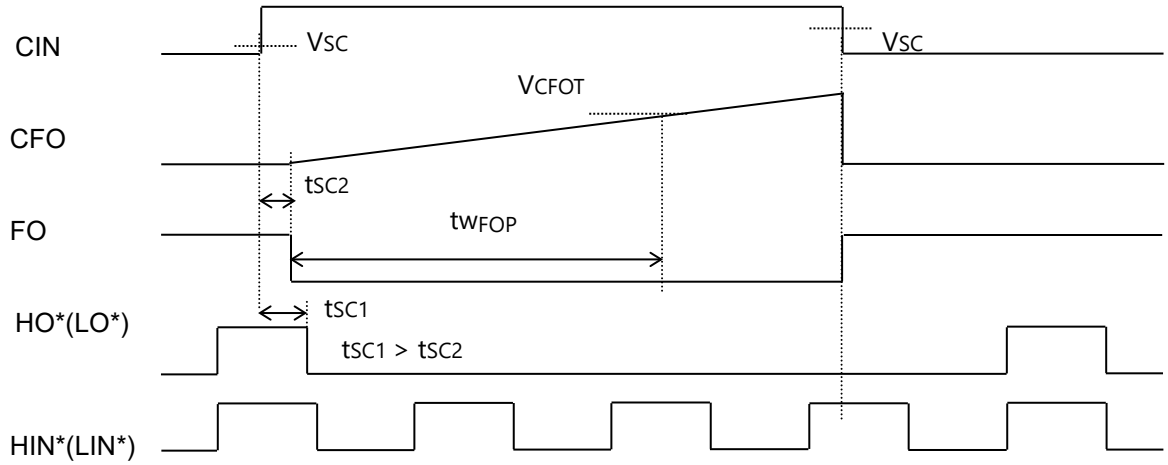
Note1 : FO Pulse Output Width (tw_{FOP}) sets in the following calculation formulas.

$$tw_{FOP} = C\ (\text{CFO external capacitor}) \times V_{CFOT} / I_{CFO}$$

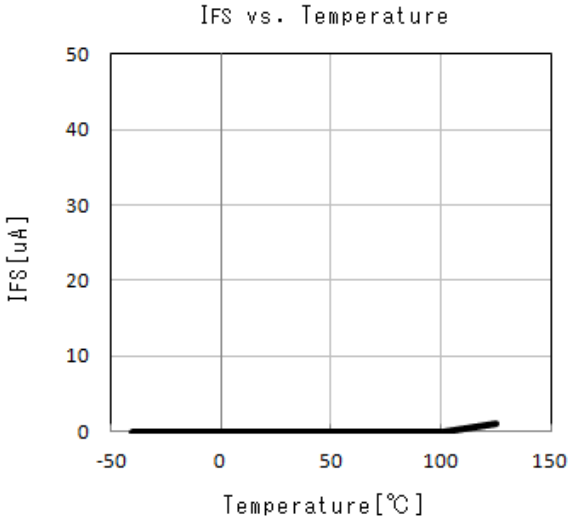
Example: When the external capacitor at CFO terminal is 22nF, tw_{FOP} is calculated as below.

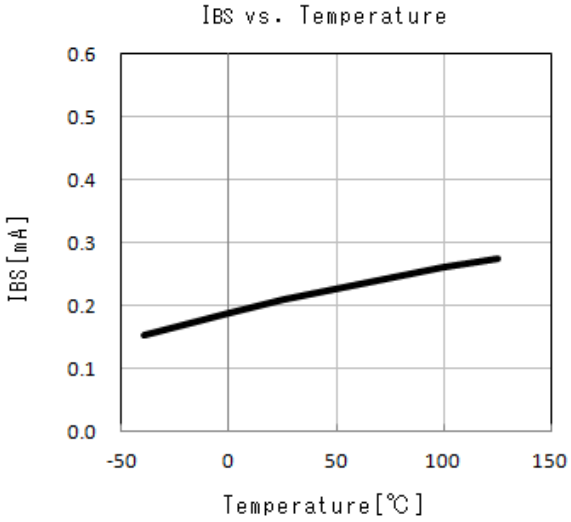
$$tw_{FOP} = C\ (22nF) \times V_{CFOT}(5.0V) / I_{CFO}(10\mu A) = 11ms$$

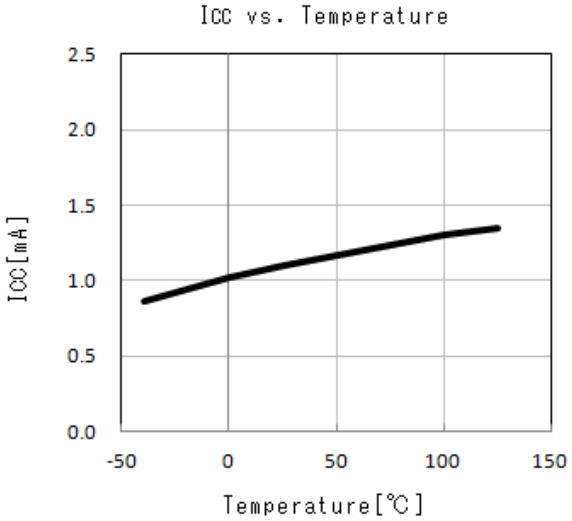
Note2: If CIN terminal voltage keeps higher than SC trip voltage (V_{SC}) over SC filter time, FO output signal keeps “L” and HO* (or LO*) output signal keeps shut down.
And then, if CIN terminal voltage is lower than SC trip voltage, FO output signal become “H” and HO*(or LO*) output signal will respond to the next active HIN*(LIN*) signal(L→H).

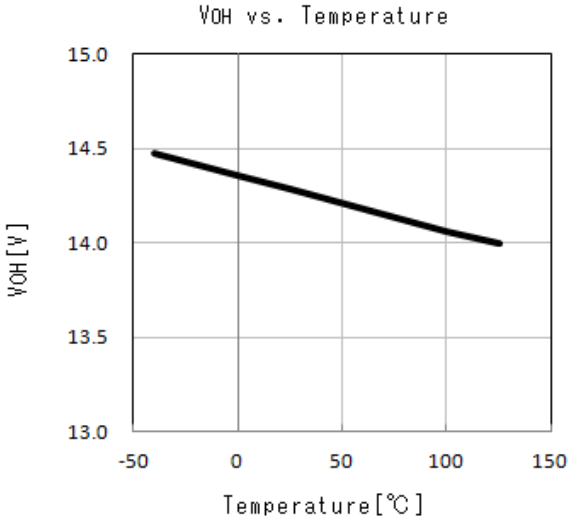


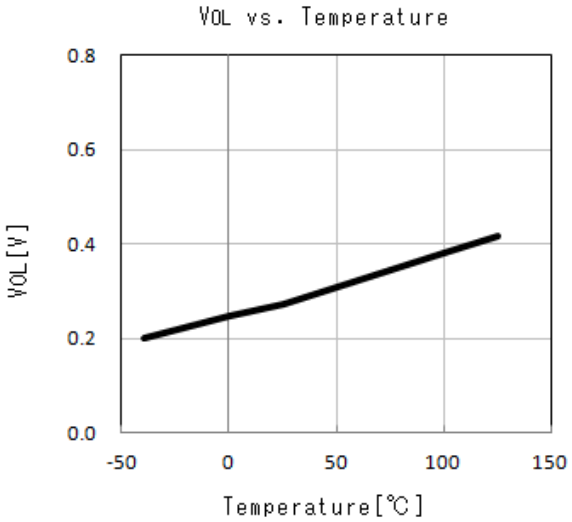
PERFORMANCE CURVES (* :U or V or W Phase)

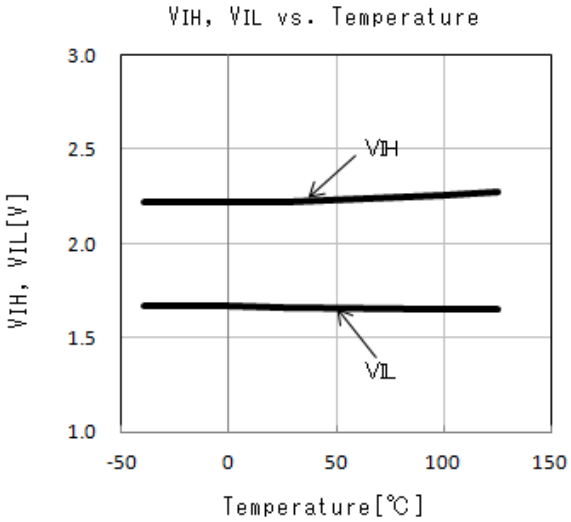




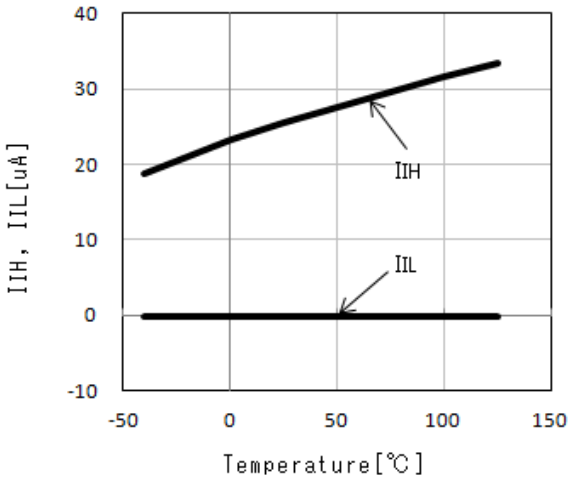




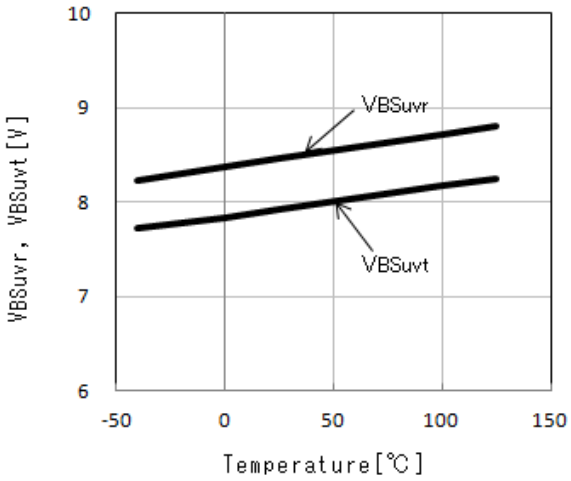




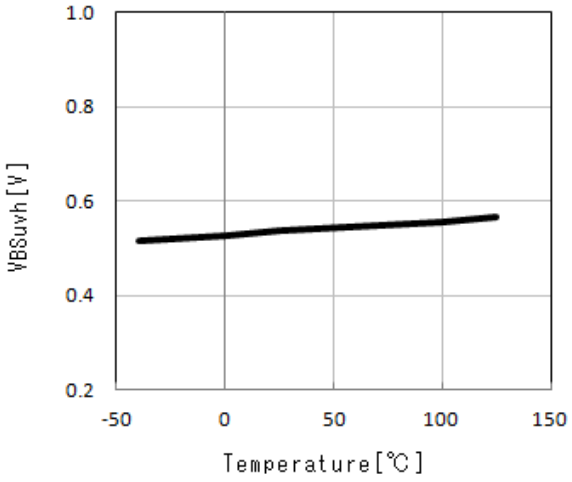
IIH, IIL vs. Temperature



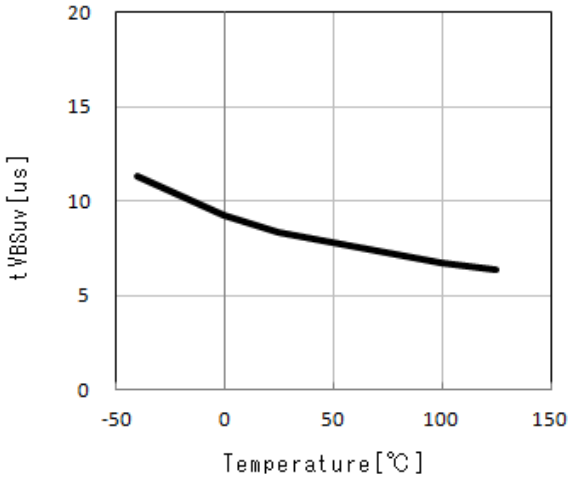
VBSuvr, VBSuvt vs. Temperature



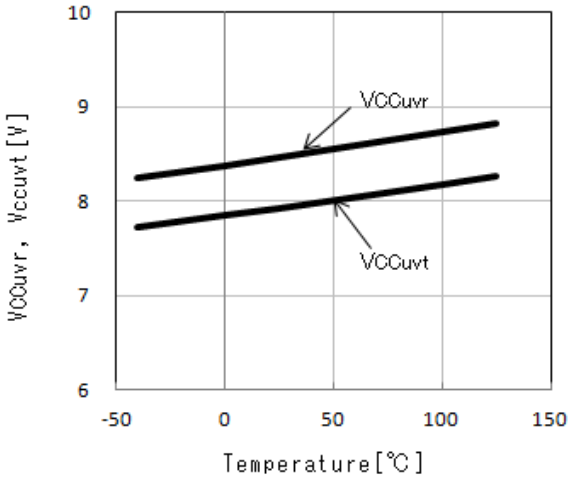
VBSuvh vs. Temperature



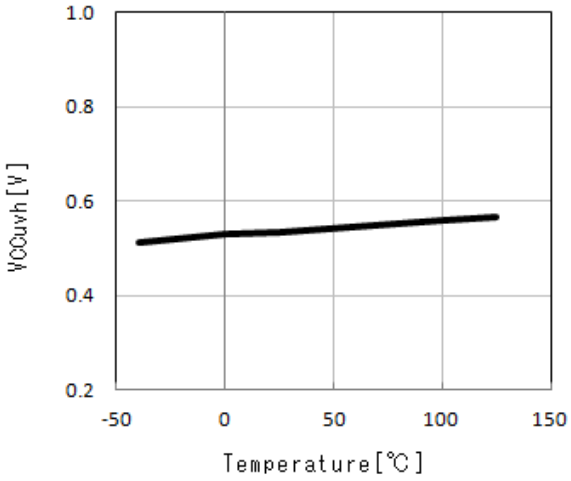
tVBSuv vs. Temperature



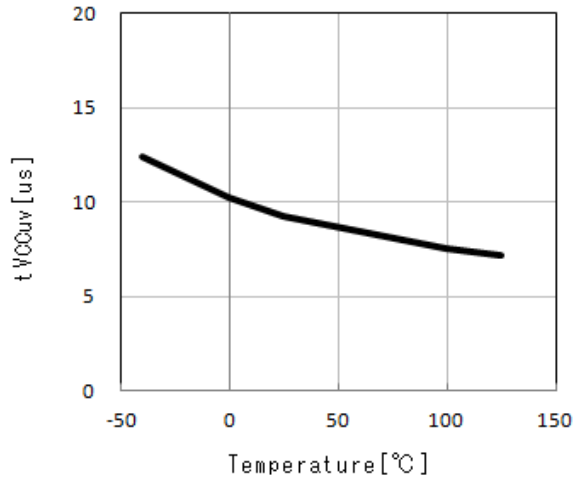
VCCuvr, VCCuvt vs. Temperature



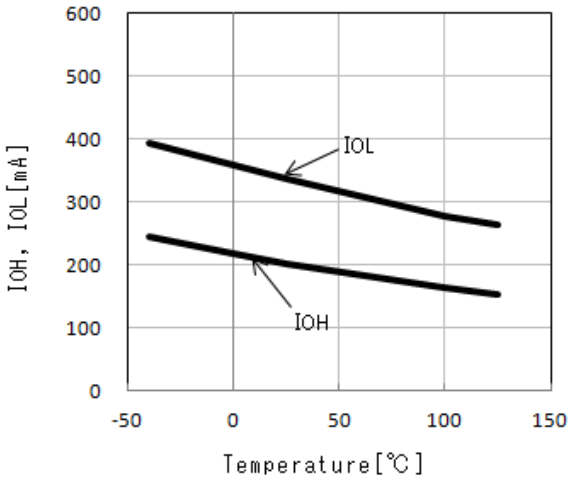
VCCuvh vs. Temperature



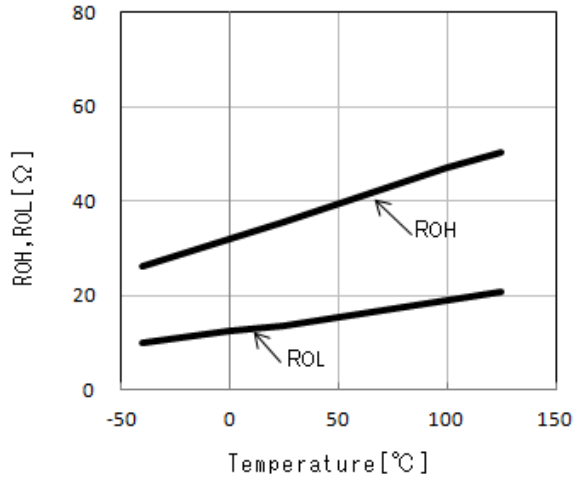
tVCCuv vs. Temperature



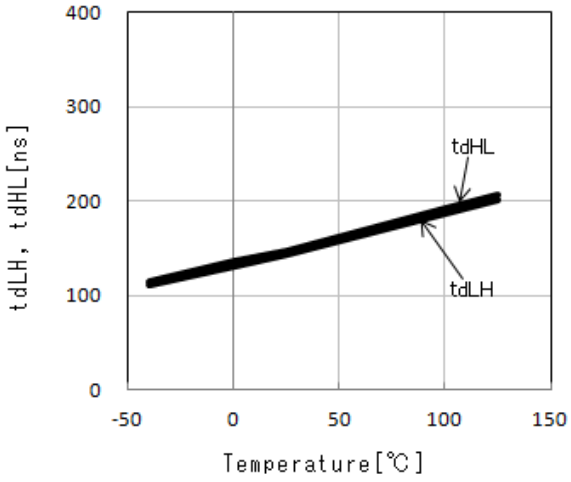
IOH, IHL vs. Temperature



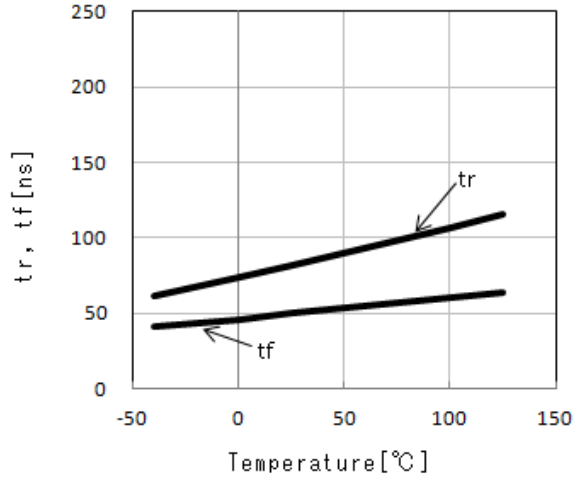
ROH, ROL vs. Temperature



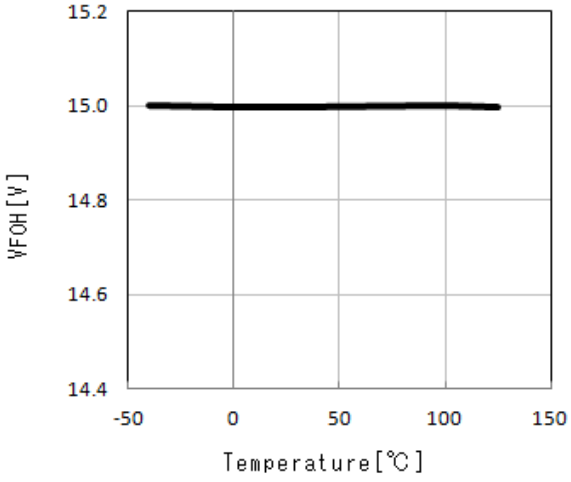
tdLH, tdHL vs. Temperature



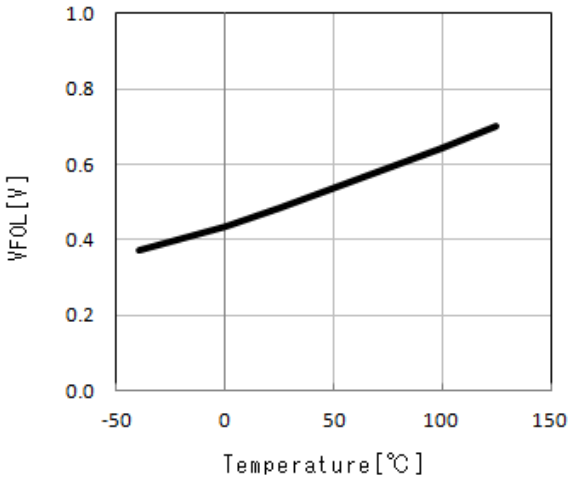
tr, tf vs. Temperature



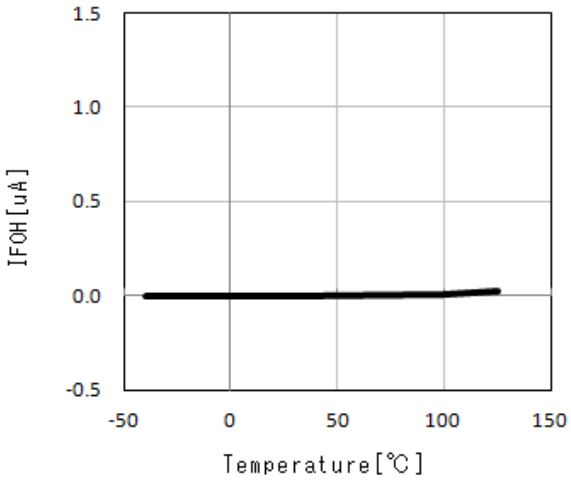
VFOH vs. Temperature



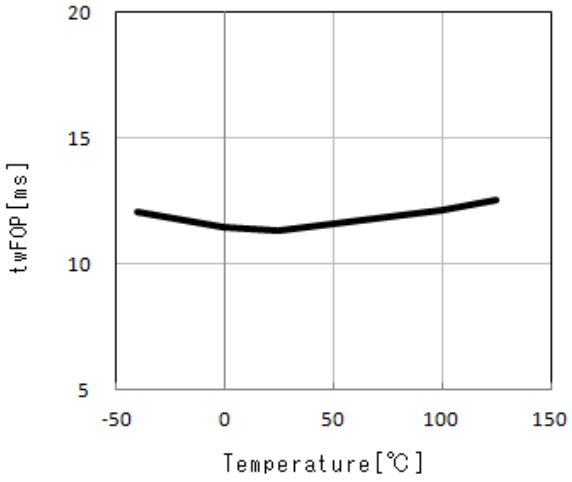
VFOL vs. Temperature



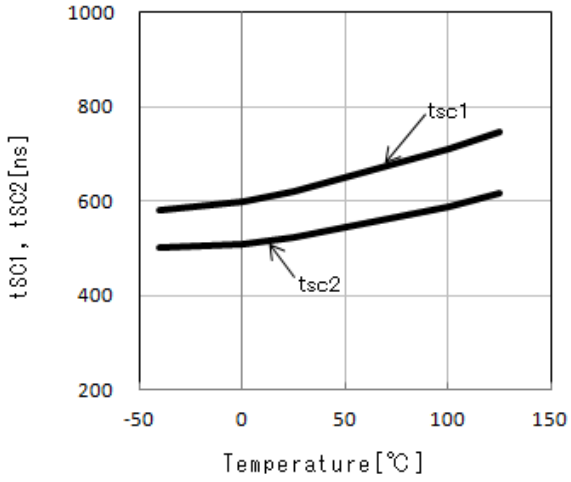
IFOH vs. Temperature



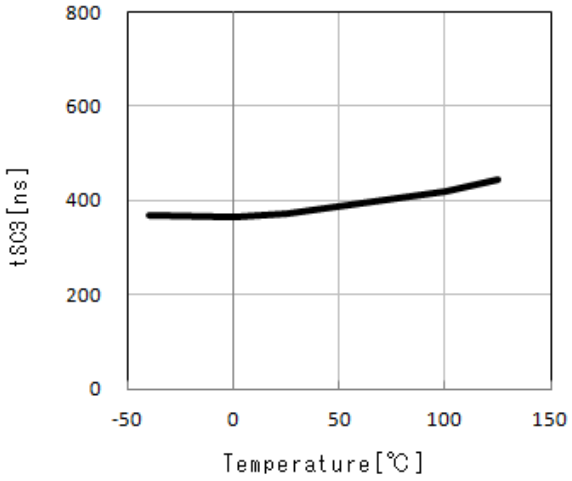
twFOP(CFO=22nF) vs. Temperature



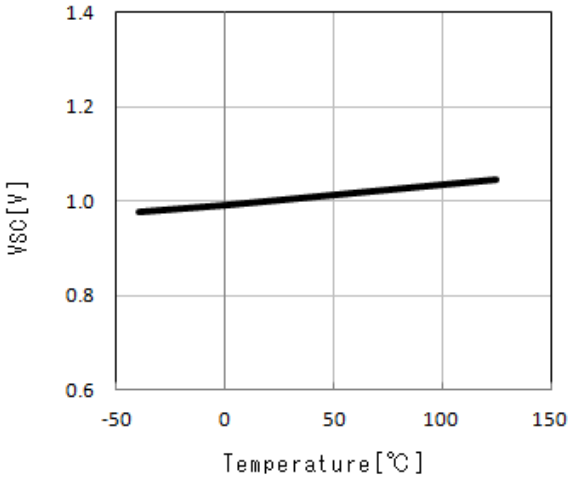
tSC1, tSC2 vs. Temperature

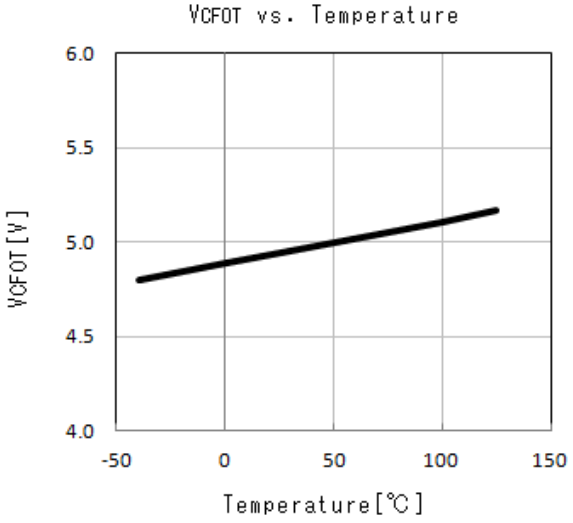


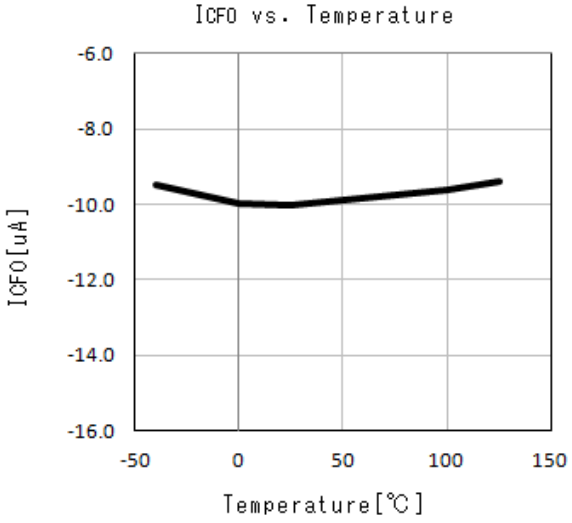
tSC3 vs. Temperature

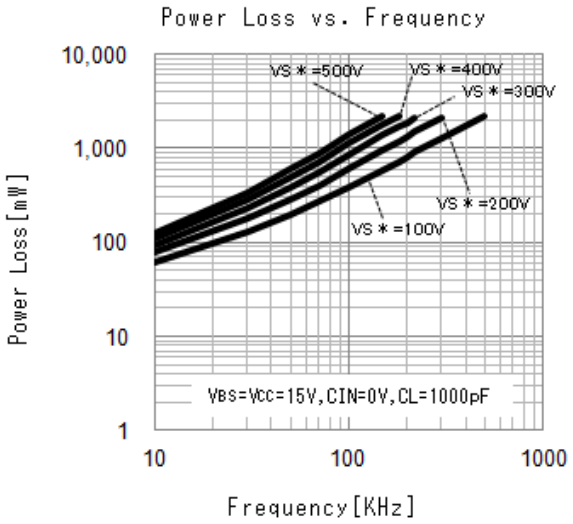


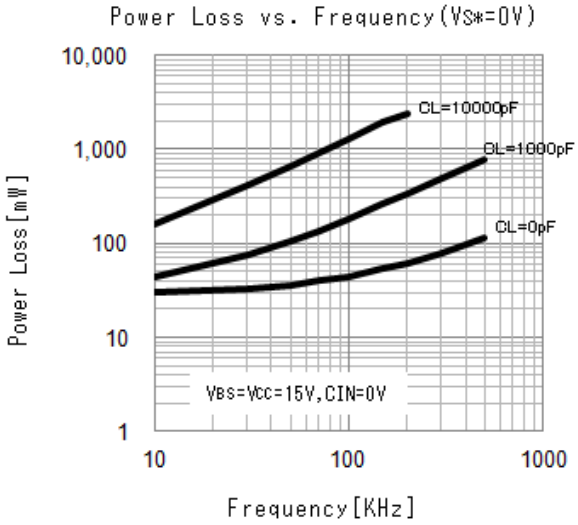
VSC vs. Temperature




VCFOT vs. Temperature
VCFOT[V]
6.0
5.5
5.0
4.5
4.0
-50
0
50
100
150
Temperature[℃]


ICFO vs. Temperature
ICFO[uA]
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-50
0
50
100
150
Temperature[℃]


Power Loss vs. Frequency
Power Loss[mW]
10,000
1,000
100
10
1
10
100
1000
Frequency[KHz]
VS＊=500V
VS＊=400V
VS＊=300V
VS＊=200V
VS＊=100V
VBS=VCC=15V,CIN=0V,CL=1000pF


Power Loss vs. Frequency(VS*=0V)
Power Loss[mW]
10,000
1,000
100
10
1
10
100
1000
Frequency[KHz]
CL=10000pF
CL=1000pF
CL=0pF
VBS=VCC=15V,CIN=0V

NOTES (* :U or V or W Phase)

1) Allowable supply voltage transient
It is recommended to supply V_{CC} firstly and supply V_{BS} secondly. In the case of shutting off supply voltage, please shut off V_{BS} firstly and shut off V_{CC} secondly.
When applying VCC and VBS, power supply should be applied slowly.
If it rises rapidly, output signal (HO* or LO*) may be malfunction.

2) Supply voltage start up or restart after shut down
If V_{CC} supply is less than 10V(outside of RECOMMENDED OPERATING CONDITIONS), there is some possibility that output does not change in response to input.
Please evaluate carefully about supply start up or restart after shutdown in your application systems.

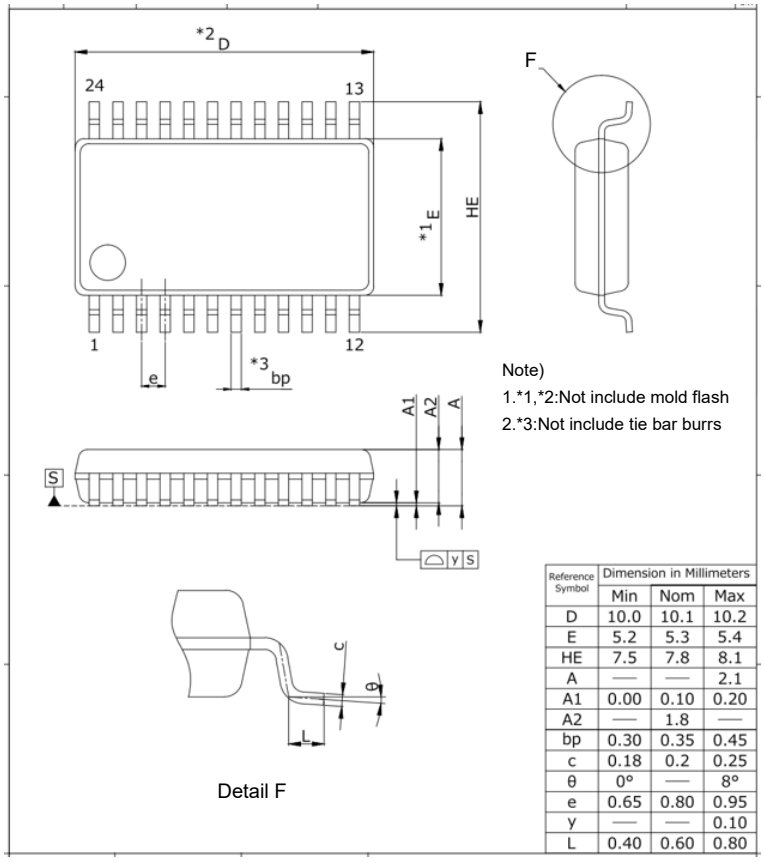
3) V_{B*} supply voltage
Please use V_{B*} supply voltage within RECOMMENDED OPERATING CONDITIONS (V_{S*} +10V < V_{B*}).
If V_{B*} supply voltage is used on the other conditions, output signal HO* may be malfunction.
Please evaluate carefully about V_{B*} supply voltage in your application systems.

4) Processing between IC terminals
As for this product, the terminal of low voltage part and high voltage part are arranged across the NC terminal (The 14th: LO_U, The 16th: V_{SW}). In addition, terminals between 3phase of high voltage parts are adjacent (The 18th: V_{BW}, The 19th: V_{SV}) (The 21th: V_{BV}, The 22th: V_{SU}).
Therefore, if insulation space distance of those terminals can not be enough, please coat between those terminals.

ENVIRONMENTAL CONSCIOUSNESS

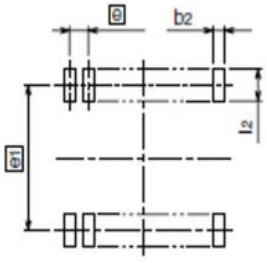
M81749FP is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU+(EU)2015/863.

PACKAGE OUTLINE



Note)
1.*1,*2:Not include mold flash
2.*3:Not include tie bar burrs

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
HE	7.5	7.8	8.1
A	—	—	2.1
A1	0.00	0.10	0.20
A2	—	1.8	—
bp	0.30	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
e	0.65	0.80	0.95
y	—	—	0.10
L	0.40	0.60	0.80



Recommended Mount Pad

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
e1	—	7.62	—
l2	1.27	—	—
e	—	0.8	—
b2	—	0.5	—

The above is one example.
Please design the mount pad with your evaluation.

Main Revision for this Edition

Rev.	Date	Revision	
		Pages	Points
A	10 Mar.2015	-	New
B	21 Apr. 2015	2	RECOMMENDED OPERATING CONDITIONS “VB*>10V” (Test condition of VS*) was added.
		5	FUNCTION TABLE “HO* = L, LO* = L when HIN*=LIN=H and V_{BS}UV is detected” was added. “Note2 : “H” state of CIN means that CIN become SC trip voltage.” was added.
C	28 Apr. 2021	-	Update format

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