MITSUBISHI ELECTRIC

<HVIC>

M81770FP

600V HIGH VOLTAGE HALF BRIDGE DRIVER

DESCRIPTION

M81770FP is high voltage Power MOSFET and IGBT module driver for half bridge applications.

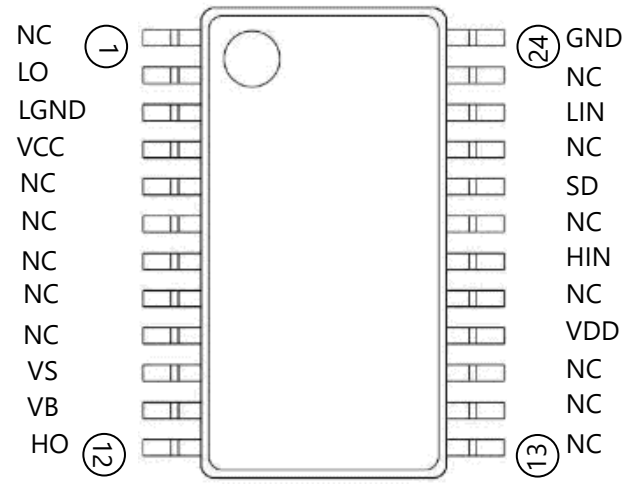
FEATURES

- ●FLOATIONG SUPPLY VOLTAGE.....600V
- ● OUTPUT CURRENT.....±3.25A(Typ)
- ● HALF BRIDGE DRIVER
- ● SSOP-24 PACKAGE

APPLICATIONS

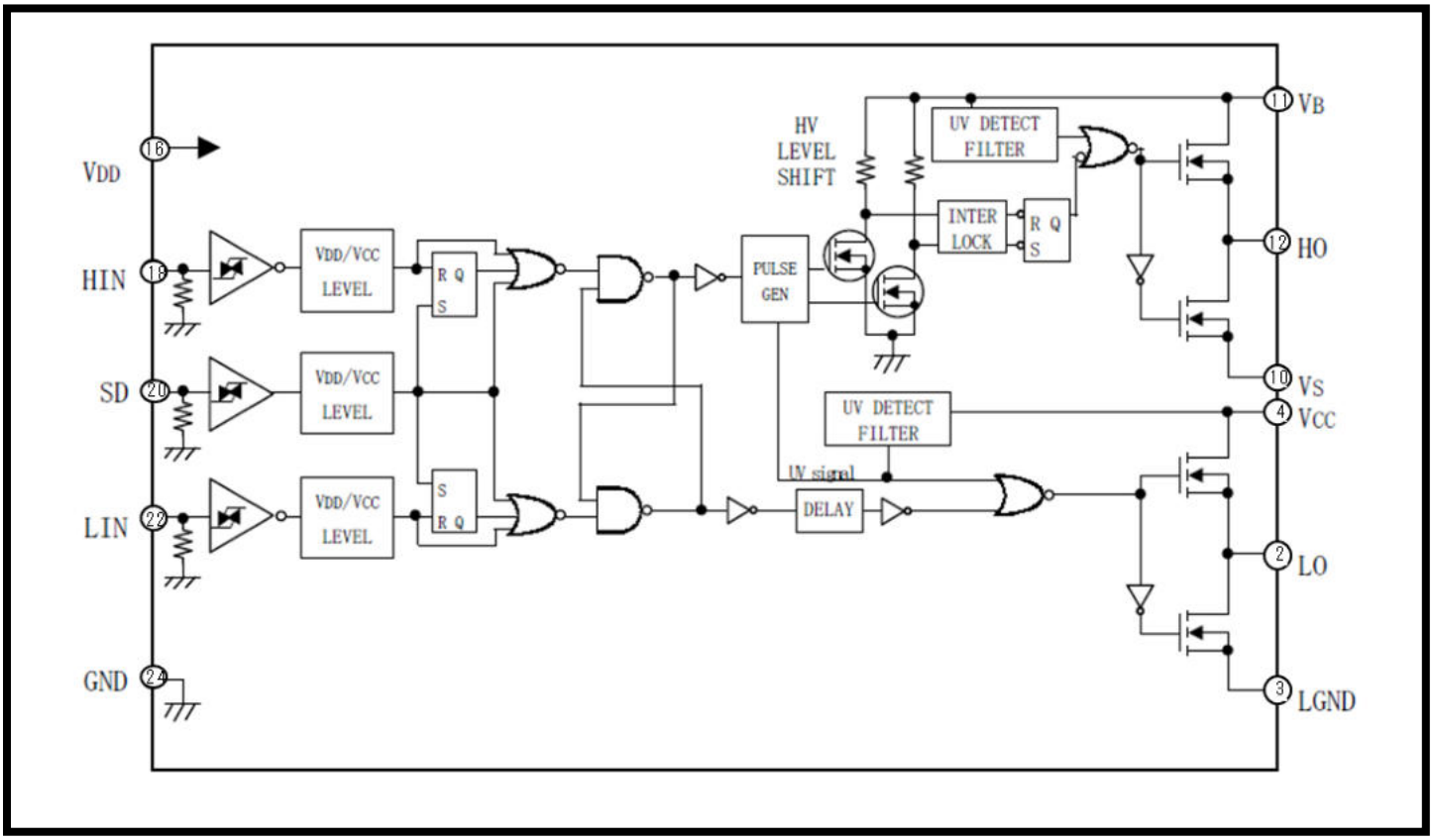
PDP. HID lamp.
MOSFET and IGBT module inverter driver for refrigerator, air-conditioner, washing machine, servomotor and general purpose.

PIN CONFIGURATION (TOP VIEW)



Outline:SSOP24
NC:NO CONNECTION

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C unless otherwise specified)

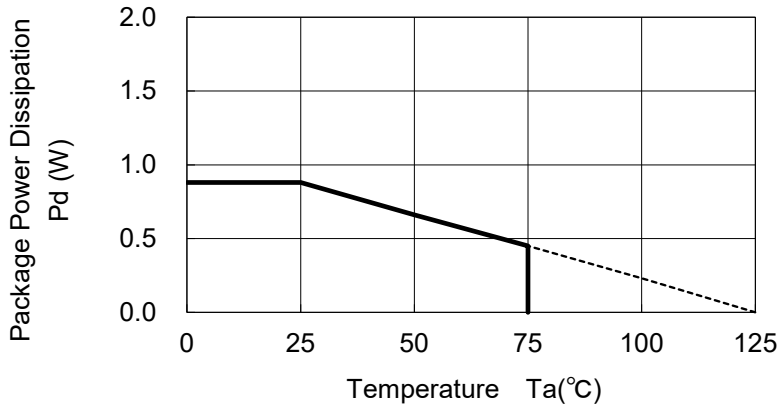
Symbol	Parameter	Test conditions	Ratings	Unit
VB	High Side Floating Supply Absolute Voltage		- 0.5 ~ 624	V
VS	High Side Floating Supply Offset Voltage		VB - 24 ~ VB + 0.5	V
VBS	High Side Floating Supply Voltage	$V_{BS} = V_B - V_S$	- 0.5 ~ 24	V
VHO	High Side Output Voltage		VS - 0.5 ~ VB + 0.5	V
VCC	Low Side Fixed Supply Voltage		- 0.5 ~ 24	V
VLO	Low Side Output Voltage		- 0.5 ~ VCC + 0.5	V
VDD	Logic Supply Voltage		- 0.5 ~ VCC + 0.5	V
VIN	Logic Input Voltage	HIN,LIN Terminal	- 0.5 ~ VDD + 0.5	V
SD	Shut Down Input Voltage	SD Terminal	- 0.5 ~ VDD + 0.5	V
LGND	Low Side Return Offset Voltage	VCC-LGNG<24V	- 5 ~ VCC + 0.5	V
dVS/dt	Allowable Offset Supply Voltage Transient		± 50	V/ns
Pd	Package Power Dissipation	Ta = 25°C ,On Board	0.88	W
Kθ	Linear Derating Factor	Ta > 25°C ,On Board	-8.8	mW/℃
Rth(j-c)	Junction-Case Thermal Resistance		50	℃/W
Tj	Junction Temperature		- 20 ~ 125	℃
Topr	Operation Temperature	On Board	- 20 ~ 75	℃
Tstg	Storage Temperature		- 40 ~ 125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VB	High Side Floating Supply Absolute Voltage		VS + 10	—	VS + 20	V
VS	High Side Floating Supply Offset Voltage	V_B > 10V	- 5	—	500	V
VBS	High Side Floating Supply Voltage	$V_{BS} = V_B - V_S$	10	—	20	V
VHO	High Side Output Voltage		VS	—	VB	V
VCC	Low Side Fixed Supply Voltage		10	—	20	V
VLO	Low Side Output Voltage		0	—	VCC	V
VDD	Logic Supply Voltage		4.5	—	20	V
VIN	Logic Input Voltage	HIN, LIN Terminal	0	—	VDD	V
SD	Shut Down Input Voltage	SD Terminal	0	—	VDD	V
LGND	Low Side Return Offset Voltage	VCC-LGND < 24V	- 5	—	5	V

Note : For proper operation, the device should be used within the recommended conditions

THERMAL DERATING FACTOR CHARACTERISTIC (MAXIMUM RATING)



ELECTRICAL CHARACTERISTICS (Ta=25°C,VCC=VBS(=VB-VS)=15V, LGND=0V unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*1	Max.	
IFS	Floating Supply Leakage Current	$V_B = V_S = 600V$	—	—	1.0	uA
IBS	VBS Standby Current		—	0.35	0.7	mA
ICC	VCC Standby Current		—	0.85	1.5	mA
IDD	VDD Standby Current		—	—	10	uA
VOH	High Level Output Voltage	I_O = 0A, LO,HO Terminal	13.8	14.4	—	V
VOL	Low Level Output Voltage	I_O = 0A, LO,HO Terminal	—	—	0.1	V
VIH15	High Level Input Threshold Voltage	HIN,LIN Terminal	—	8.4	9.5	V
VIL15	Low Level Input Threshold Voltage	HIN,LIN Terminal	6.0	6.8	—	V
VIH5	High Level Input Threshold Voltage	HIN,LIN Terminal (VDD=5V)	—	3.1	4.1	V
VIL5	Low Level Input Threshold Voltage	HIN,LIN Terminal (VDD=5V)	1.4	2.4	—	V
VISDH15	Shutdown High Level Input Threshold Voltage	HIN,LIN Terminal	—	8.4	9.5	V
VISDL15	Shutdown Low Level Input Threshold Voltage	HIN,LIN Terminal	6.0	6.8	—	V
VISDH5	Shutdown High Level Input Threshold Voltage	HIN,LIN Terminal (VDD=5V)	—	3.1	4.1	V
VISDL5	Shutdown Low Level Input Threshold Voltage	HIN,LIN Terminal (VDD=5V)	1.4	2.4	—	V
IIH	High Level Input Bias Current	V_{IN} = 15V	—	75	150	uA
IIL	Low Level Input Bias Current	V_{IN} = 0V	—	—	1.0	uA
VBS_{uvr}	VBS Supply UV Reset Voltage		7.5	8.6	9.7	V
VBS_{uvh}	VBS Supply UV Hysteresis Voltage		0.1	0.4	0.7	V
$tVBS_{uv}$	VBS Supply UV Filter Time		—	10	—	us
VCC_{uvr}	VCC Supply UV Reset Voltage		7.5	8.6	9.7	V
VCC_{uvh}	VCC Supply UV Hysteresis Voltage		0.1	0.4	0.7	V
$tVCC_{uv}$	VCC Supply UV Filter Time		—	10	—	us
IOH	Output High Level Short Circuit Pulsed Current	VO = 0V, VIN = 15V, PW < 10us	—	-3.25	—	A
IOL	Output Low Level Short Circuit Pulsed Current	VO = 15V, VIN = 0V, PW < 10us	—	3.25	—	A
ROH	Output High Level On resistance	IO = -200mA, ROH = (VOH-VO)/IO	—	12	16	Ω
ROL	Output Low Level On resistance	IO = 200mA, ROL = VO/IO	—	2.5	3.5	Ω
$t_dLH(HO)$	High Side Turn-On Propagation Delay	CL=1000pF between HO–VS(VDD=5V)	270	—	470	ns
$t_dHL(HO)$	High Side Turn-Off Propagation Delay	CL=1000pF between HO–VS(VDD=5V)	230	—	430	ns
t_rH	High Side Turn-On Rise Time	CL=1000pF between HO–VS(VDD=5V)	—	40	60	ns
t_fH	High Side Turn-Off Fall Time	CL=1000pF between HO–VS(VDD=5V)	—	20	35	ns
$t_dLH(LO)$	Low Side Turn-On Propagation Delay	CL=1000pF between LO–LGND(VDD=5V)	270	—	470	ns
$t_dHL(LO)$	Low Side Turn-Off Propagation Delay	CL=1000pF between LO–LGND(VDD=5V)	230	—	430	ns
t_rL	Low Side Turn-On Rise Time	CL=1000pF between LO–LGND(VDD=5V)	—	40	60	ns
t_fL	Low Side Turn-Off Fall Time	CL=1000pF between LO–LGND(VDD=5V)	—	20	35	ns
⊿tdLH	Turn-On Propagation Delay Matching	|tdLH(HO) - tdLH(LO)|	—	—	130	ns
⊿tdHL	Turn-Off Propagation Delay Matching	|tdHL(HO) - tdHL(LO)|	—	—	130	ns
tSD	Shutdown Propagation Delay	CL=1000pF between HO–VS CL=1000pF between LO–LGND(VDD=5V)	230	—	430	ns

* Typ. is not specified.

FUNCTION TABLE (X:H or L)

HIN	LIN	VBS UV	VCC UV	HO	LO	SD	Behavioral state
L	L	H	H	L	L	L	LO = L, HO = L
L	H	H	H	L	H	L	LO = H
H	L	H	H	H	L	L	HO = H
H	H	H	H	*	*	L	
X	L	L	H	L	L	L	LO = OFF, HO = OFF, VBS UV tripped
X	H	L	H	L	H	L	LO = ON, HO = OFF, VBS UV tripped
L	X	H	L	L	L	L	LO = OFF, HO = OFF, VCC UV tripped
H	X	H	L	L	L	L	LO = OFF, HO = OFF, VCC UV tripped
X	X	H	H	L	L	H	LO = OFF, HO = OFF, SD = ON

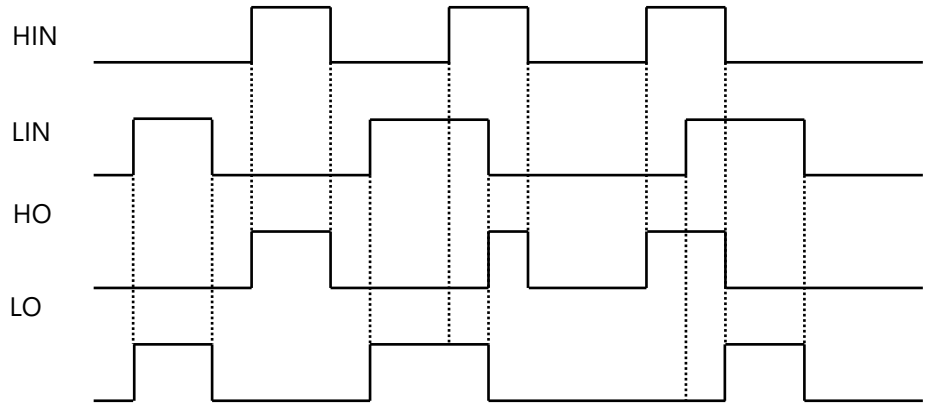
Note : “L” state of VBS UV and VCC UV means that UV trip voltage.

- If both input signals are “H”, refer to TIMING DIAGRAM.

TIMING DIAGRAM

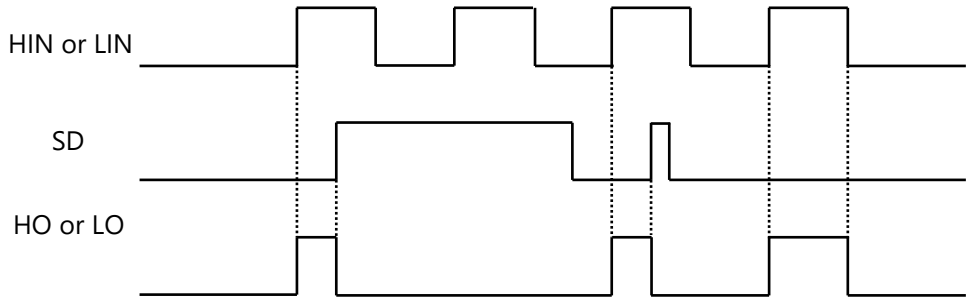
1.Input/Output Timing Diagram

When input signal (HIN or LIN) is “H”, then output signal (HO or LO) is “H”.
In the case of both input signals (HIN and LIN) are “H”, first coming input signal (HIN or LIN) “H” is only accepted.
Corresponding this signal, output signal (HO or LO) becomes “H”.
Corresponding the other signal (LIN or HIN), output signal (LO or HO) keeps “L”.



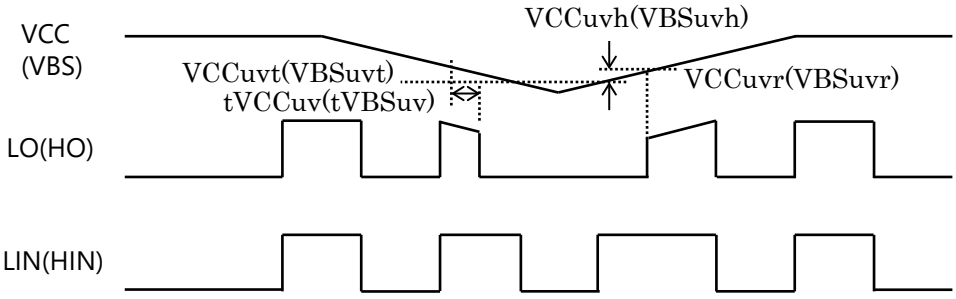
2.Shutdown Input Timing Diagram

When shutdown input signal (SD) is “H”, then output signals (HO and LO) are “L”.
Output signals (HO and LO) keep “L” by shutdown input signal (SD) is “L” until next input signal (HIN or LIN) is “H”.



3.VCC (VBS) Supply Under Voltage Lockout Timing Diagram

If VCC supply voltage drops below UV trip voltage (VCCuvt) for VCC supply UV filter time, LO output signal is shut down. And then, if VCC supply voltage rises over UV reset voltage, LO will return to the usual operation mode. Both HI side and Low side have the same sequence.



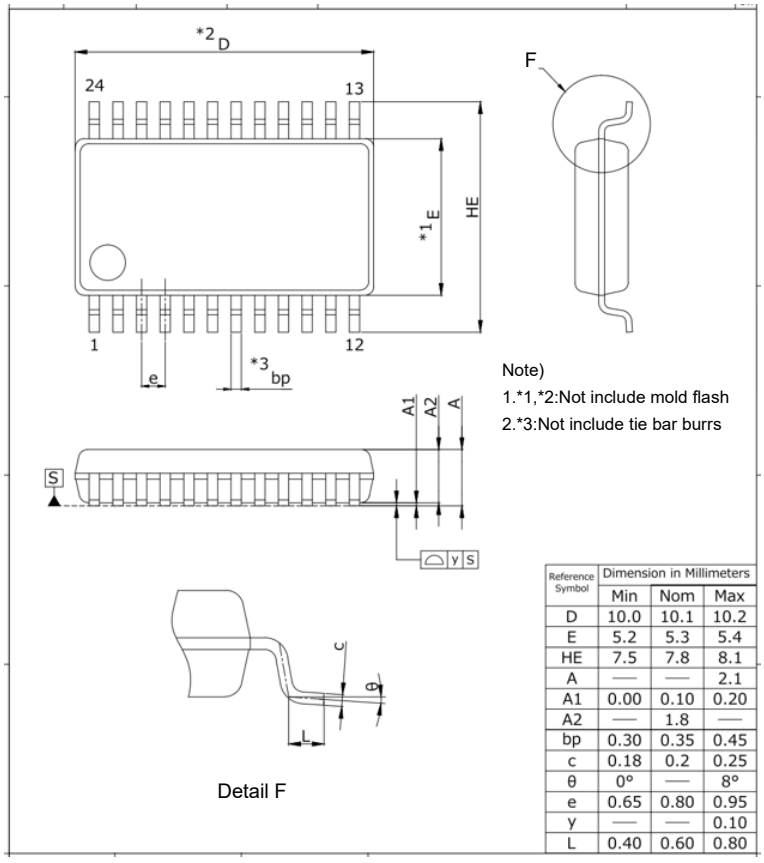
4.Allowable supply voltage transient

It is recommended to supply VCC first and supply VDD and VBS in that order.
To cut off the power supply voltage, first shut down VBS and shut down in the order VDD and VCC.
When applying VCC,VDD and VBS, power supply should be applied slowly.
If it rises rapidly, output signal (HO or LO) may be malfunction.

ENVIRONMENTAL CONSCIOUSNESS

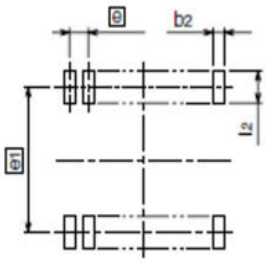
M81770FP is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU+(EU)2015/863.

PACKAGE OUTLINE



Note)
1.*1,*2:Not include mold flash
2.*3:Not include tie bar burrs

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
HE	7.5	7.8	8.1
A	—	—	2.1
A1	0.00	0.10	0.20
A2	—	1.8	—
bp	0.30	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
e	0.65	0.80	0.95
y	—	—	0.10
L	0.40	0.60	0.80



Recommended Mount Pad

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
e1	—	7.62	—
l2	1.27	—	—
e	—	0.8	—
b2	—	0.5	—

The above is one example.
Please design the mount pad with your evaluation.

Main Revision for this Edition

Rev.	Date	Revision	
		Pages	Points
A	14 Jul. 2017	-	New
B	02 Feb. 2018	-	“PRELIMINARY” was deleted
C	28 Apr. 2021	1 7 -	Add OUTLINE (SOP16 and SSOP24) Add PACKAGE OUTLINE1,2 Update format
D	10 Jan. 2023	1 6	Delete Outline:SOP16(Not recommended for new designs) Delete PACKAGE OUTLINE(Not recommended for new designs)
E	31 Jan. 2023	1	Delete SOP-16 in FEATURES.

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