

<Intelligent Power Modules>

# PM50CG1AP065/PM50CG1APL065

FLAT-BASE TYPE  
INSULATED PACKAGE



## FEATURE

- a) Adopting Full-Gate CSTBT™ chip.
- b) The over-temperature protection which detects the chip surface temperature of CSTBT™ is adopted.
- c) Error output signal is available from each protection upper and lower arm of IPM.
- d) Outputting an error signal corresponding to the abnormal state (error mode identification)

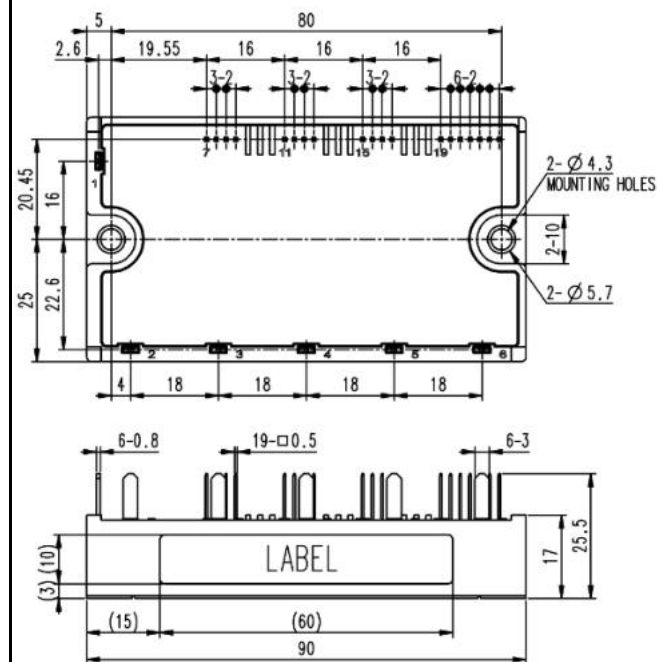
UL Recognized under UL1557, File No. E323585

This product is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU and (EU)2015/863.

## APPLICATION

General purpose inverter, servo drives and other motor controls

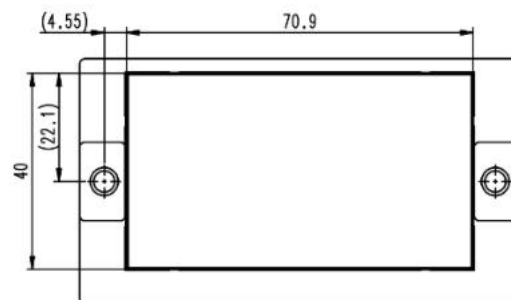
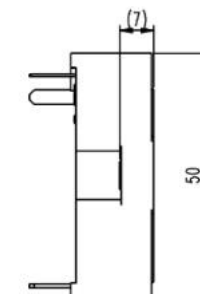
## PACKAGE OUTLINES



## Dimensions in mm

Tolerance otherwise specified

Division of Dimension		Tolerance
0.5	to 3	±0.2
over 3	to 6	±0.3
over 6	to 30	±0.5
over 30	to 120	±0.8
over 120	to 400	±1.2



## TERMINAL CODE

---CG1AP type---

1.NC, 2.P, 3.NC, 4.U, 5.V, 6.W, 7.V<sub>UPC</sub>, 8.U<sub>FO</sub>, 9.U<sub>P</sub>, 10.V<sub>UP1</sub>, 11.V<sub>VPC</sub>, 12.V<sub>FO</sub>, 13.V<sub>P</sub>, 14.V<sub>VP1</sub>, 15.V<sub>WPC</sub>, 16.W<sub>FO</sub>, 17.W<sub>P</sub>, 18.V<sub>WP1</sub>, 19.V<sub>NC</sub>, 20.V<sub>N1</sub>, 21.NC, 22.U<sub>N</sub>, 23.V<sub>N</sub>, 24.W<sub>N</sub>, 25.F<sub>O</sub>

---CG1APL type---

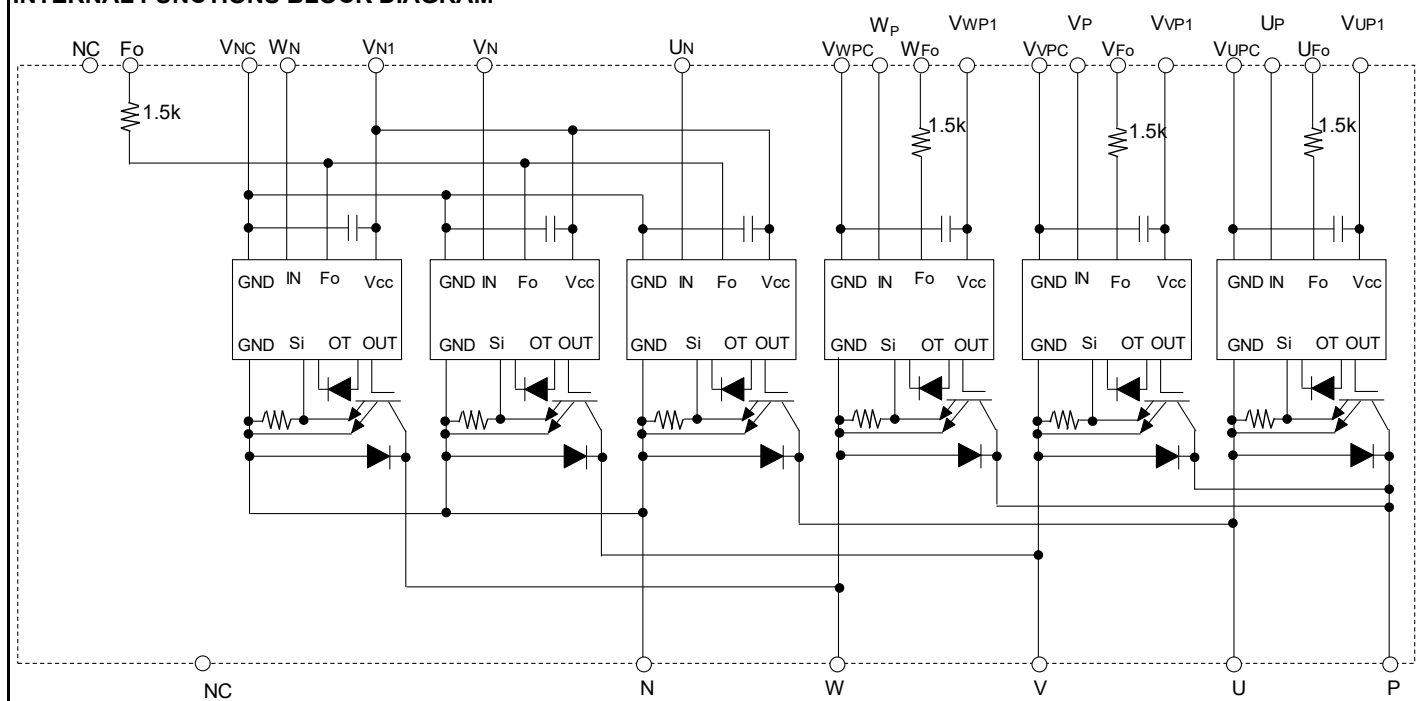
1.N, 2.P, 3.NC, 4.U, 5.V, 6.W, 7.V<sub>UPC</sub>, 8.U<sub>FO</sub>, 9.U<sub>P</sub>, 10.V<sub>UP1</sub>, 11.V<sub>VPC</sub>, 12.V<sub>FO</sub>, 13.V<sub>P</sub>, 14.V<sub>VP1</sub>, 15.V<sub>WPC</sub>, 16.W<sub>FO</sub>, 17.W<sub>P</sub>, 18.V<sub>WP1</sub>, 19.V<sub>NC</sub>, 20.V<sub>N1</sub>, 21.NC, 22.U<sub>N</sub>, 23.V<sub>N</sub>, 24.W<sub>N</sub>, 25.F<sub>O</sub>

## PM50CG1AP065/PM50CG1APL065

HIGH POWER SWITCHING USE

INSULATED TYPE

## INTERNAL FUNCTIONS BLOCK DIAGRAM



## MAXIMUM RATINGS (Tvj = 25°C, unless otherwise noted)

## INVERTER PART

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CES}$	Collector-Emitter Voltage	$V_D=15\text{ V}$ , $V_{CIN}=15\text{ V}$	650	V
$I_C$	Collector Current	$T_C=25\text{ }^\circ\text{C}$	50	A
$I_{CRM}$		Pulse	100	
$P_{tot}$	Total Power Dissipation	$T_C=25\text{ }^\circ\text{C}$	240	W
$I_E$	Emitter Current (Free-wheeling Diode Forward current)	$T_C=25\text{ }^\circ\text{C}$	50	A
$I_{ERM}$		Pulse	100	
$T_{vj}$	Junction Temperature	(Note5)	-20 ~ +150	$^\circ\text{C}$

\*: Tc measurement point is just under the chip.

## CONTROL PART

Symbol	Parameter	Conditions	Ratings	Unit
$V_D$	Supply Voltage	Applied between: $V_{UP1}-V_{UPC}$ , $V_{VP1}-V_{VPC}$ , $V_{WP1}-V_{WPC}$ , $V_{N1}-V_{NC}$	20	V
$V_{CIN}$	Input Voltage	Applied between: $U_P-V_{UPC}$ , $V_P-V_{VPC}$ , $W_P-V_{WPC}$ , $U_N$ , $V_N$ , $W_N-V_{NC}$	20	V
$V_{FO}$	Fault Output Supply Voltage	Applied between: $U_{FO}-V_{UPC}$ , $V_{FO}-V_{VPC}$ , $W_{FO}-V_{WPC}$ , $F_O-V_{NC}$	20	V
$I_{FO}$	Fault Output Current	Sink current at $U_{FO}$ , $V_{FO}$ , $W_{FO}$ , $F_O$ terminals	20	mA

## TOTAL SYSTEM

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(Prot)}$	Supply Voltage Protected by SC	$V_D = 13.5\text{ V} \sim 16.5\text{ V}$ , Inverter Part, $T_{vj}=+125\text{ }^\circ\text{C}$ start	400	V
$T_{stg}$	Storage Temperature	-	-40 ~ +125	$^\circ\text{C}$
$T_C$	Operating Case Temperature	(Note5)	-20 ~ +125	$^\circ\text{C}$
$V_{isol}$	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base plate, AC 1min, RMS	2500	V

\*: Tc measurement point is just under the chip.

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## THERMAL RESISTANCE

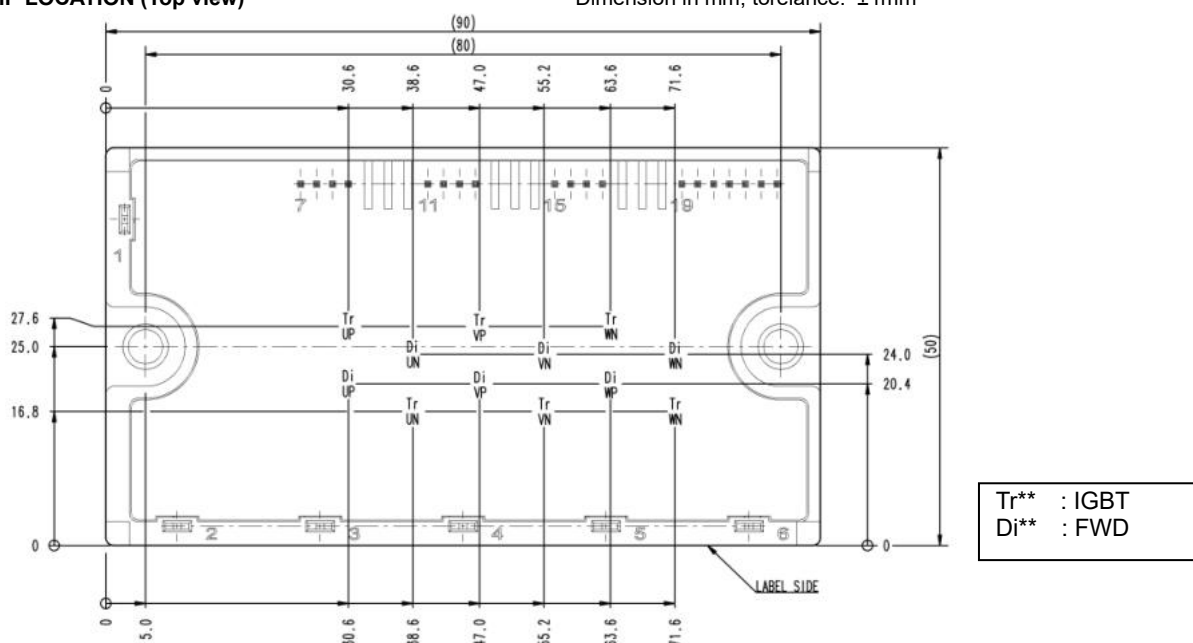
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Thermal Resistance	Junction to case, IGBT, per 1 element (Note1)	-	-	0.52	K/W
$R_{th(j-c)D}$		Junction to case, FWD, per 1 element (Note1)	-	-	0.88	
$R_{th(c-s)}$	Contact Thermal Resistance	Case to heat sink, per 1 module, Thermal grease applied (Note.1, 2, 5)	-	19.1	-	K/kW

Note1. If you use this value,  $R_{th(s-a)}$  should be measured just under the chips.

Note2. Typical value is by thermally conductive grease of  $\lambda=0.9W/(m \cdot K)$ ,  $D_{(C-S)}=50 \mu m$ .

## CHIP LOCATION (Top view)

Dimension in mm, tolerance:  $\pm 1mm$



## ELECTRICAL CHARACTERISTICS (Tvj= 25°C, unless otherwise noted)

### INVERTER PART

Symbol	Parameter	Conditions			Limits			Unit
					Min.	Typ.	Max.	
$V_{CEsat}$	Collector-Emitter Saturation Voltage	$V_D=15\text{ V}$ , $I_C=50\text{ A}$	$T_{vj}=25\text{ }^{\circ}\text{C}$	Terminal	-	-	1.7	V
				Chip	-	1.25	-	
		$V_{CIN}=0\text{ V}$ , Pulsed, (Fig.1)	$T_{vj}=125\text{ }^{\circ}\text{C}$	Terminal	-	-	1.95	
				Chip	-	1.33	-	
$V_{EC}$	Emitter-Collector Voltage	$V_D=15\text{ V}$ , $I_E=50\text{ A}$ ,	$T_{vj}=25\text{ }^{\circ}\text{C}$	Terminal	-	-	1.9	V
				Chip	-	1.40	-	
		$V_{CIN}=15\text{ V}$ , pulsed, (Fig.2)	$T_{vj}=125\text{ }^{\circ}\text{C}$	Terminal	-	-	2.0	
				Chip	-	1.45	-	
$t_{on}$	Switching Time	$V_D=15\text{ V}$ , $V_{CIN}=0\text{ V}\leftrightarrow 15\text{ V}$ , $V_{CC}=300\text{ V}$ , $I_C=50\text{ A}$ , $T_{vj}=125\text{ }^{\circ}\text{C}$ , Inductive Load (Fig.3, 4)			0.3	0.6	1.2	$\mu\text{s}$
$t_{rr}$					-	0.2	0.65	
$t_{c(on)}$					-	0.17	0.75	
$t_{off}$					-	1.0	2.3	
$t_{c(off)}$					-	0.13	0.4	
$I_{CES}$	Collector-Emitter Cut-off Current	$V_{CE}=V_{CES}$ , $V_D=15\text{ V}$ , $V_{CIN}=15\text{ V}$ (Fig.5)	$T_{vj}=25\text{ }^{\circ}\text{C}$	-	-	1	mA	
			$T_{vj}=125\text{ }^{\circ}\text{C}$	-	-	10		

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**ELECTRICAL CHARACTERISTICS** (Tvj = 25°C, unless otherwise noted)**CONTROL PART**

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I <sub>D</sub>	Circuit Current	V <sub>D</sub> =15 V, V <sub>CIN</sub> =15 V	-	4	6	mA
				12	18	
		V <sub>D</sub> =15 V, V <sub>CIN</sub> =0 V ↔ 15 V, V <sub>CC</sub> =400 V I <sub>C</sub> =0A, Tvj=125 °C, f <sub>C</sub> ≤20kHz	-	10	12	
				29	35	
V <sub>th(ON)</sub>	Input ON Threshold Voltage	Applied between: U <sub>P</sub> -V <sub>UPC</sub> , V <sub>P</sub> -V <sub>VPC</sub> , W <sub>P</sub> -V <sub>WPC</sub> , U <sub>N</sub> , V <sub>N</sub> , W <sub>N</sub> -V <sub>NC</sub>	1.2	1.5	1.8	V
V <sub>th(OFF)</sub>	Input OFF Threshold Voltage		1.7	2.0	2.3	
SC	Short Circuit Trip Level	-20≤Tvj≤125 °C, V <sub>D</sub> =15 V (Fig.3, 6)	100	-	-	A
t <sub>d(SC)</sub>	Short Circuit Current Delay Time	V <sub>D</sub> =15 V, Tvj=125 °C (Fig.3, 6)	-	2.0	-	μs
OT	Over Temperature Protection	Detect temperature of IGBT chip surface	Trip level	150	-	°C
OT <sub>(hys)</sub>			Hysteresis	-	20	
UV <sub>t</sub>	Supply Circuit	-	Trip level	11.0	12.0	V
UV <sub>r</sub>	Under-Voltage Protection		Reset level	-	12.5	
I <sub>FO(H)</sub>	Fault Output Current	V <sub>D</sub> =15 V, V <sub>FO</sub> =15 V (Note3)	-	-	0.01	mA
I <sub>FO(L)</sub>			-	10	15	
t <sub>FO</sub>	Fault Output Pulse Width	V <sub>D</sub> =15 V (Note3)	OT	-	8.0	ms
			UV	-	4.0	
			SC	-	2.0	

Note3. Fault output is given only when the internal SC, OT &amp; UV protections schemes of either upper or lower arm device operate to protect it.

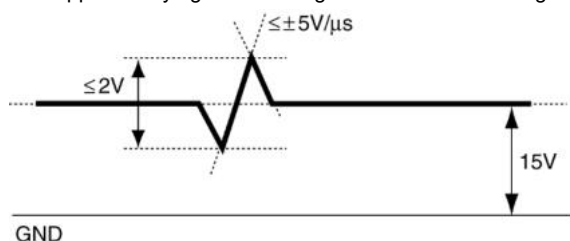
**MECHANICAL RATINGS AND CHARACTERISTICS**

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
M <sub>s</sub>	Mounting Torque	Mounting part screw : M4	1.5	1.7	2.0	N•m
m	mass	-	-	175	-	g

**RECOMMENDED CONDITIONS FOR USE**

Symbol	Parameter	Conditions	Recommended value	Unit
V <sub>CC</sub>	Supply Voltage	Applied across P-N terminals	≤ 400	V
V <sub>D</sub>	Control Supply Voltage	Applied between : V <sub>UP1</sub> -V <sub>UPC</sub> , V <sub>VP1</sub> -V <sub>VPC</sub> , V <sub>WP1</sub> -V <sub>WPC</sub> , V <sub>N1</sub> -V <sub>NC</sub> (Note4)	15.0±1.5	V
V <sub>CIN(ON)</sub>	Input ON Voltage	Applied between : U <sub>P</sub> -V <sub>UPC</sub> , V <sub>P</sub> -V <sub>VPC</sub> , W <sub>P</sub> -V <sub>WPC</sub> , U <sub>N</sub> , V <sub>N</sub> , W <sub>N</sub> -V <sub>NC</sub>	≤ 0.8	V
V <sub>CIN(OFF)</sub>	Input OFF Voltage		≥ 9.0	
f <sub>PWM</sub>	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
t <sub>dead</sub>	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig.7)	≥ 2.0	μs

Note4. With ripple satisfying the following conditions: dv/dt swing ≤ ±5 V/μs, Variation ≤ 2 V peak to peak



Note5. Long term performance related to thermal conductive material such as thermal grease (including but not limited to aspects such as the increase of thermal resistance due to pumping out, etc.) should be verified under your specific application conditions. Each temperature condition (Tvj, Tc) must be maintained below the maximum rated temperature throughout consideration of the temperature rise even for long term usage.

## PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage ( $V_D$ ), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.

After this, the specified ON and OFF level setting for each input signal should be done.

2. When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above  $V_{CES}$  rating of the device.

(These test should not be done by using a curve tracer or its equivalent.)

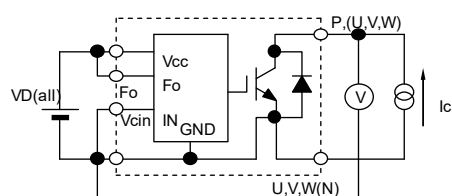


Fig.1  $V_{CESat}$  Test

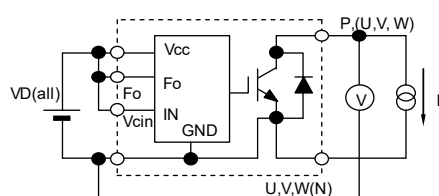


Fig.2  $V_{EC}$  Test

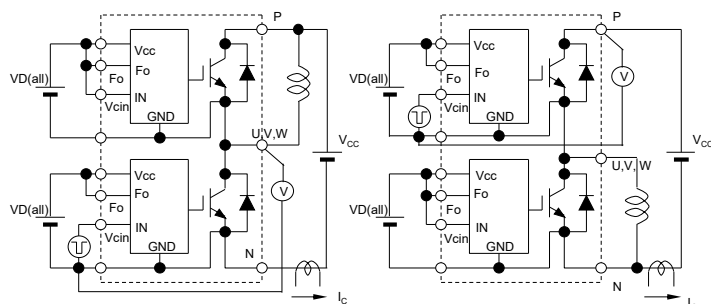


Fig.3 Switching time and SC test circuit

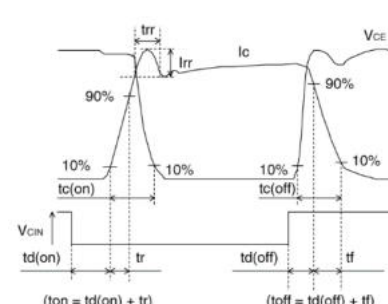


Fig.4 Switching time test waveform

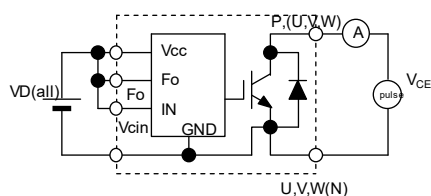


Fig.5  $I_{CES}$  Test

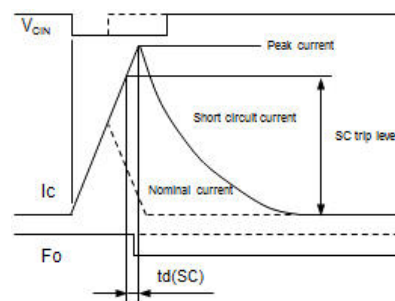
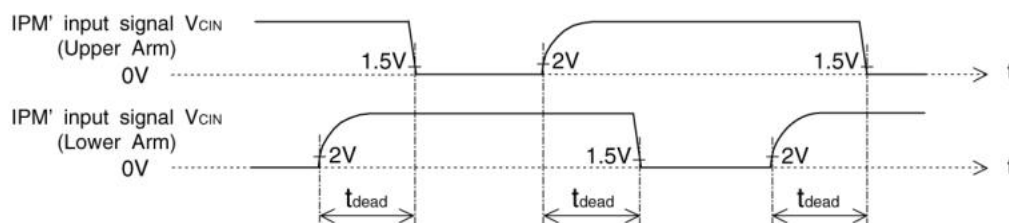


Fig.6 SC test waveform



1.5V: Input on threshold voltage  $V_{th(on)}$  typical value, 2V: Input off threshold voltage  $V_{th(off)}$  typical value

Fig. 7 Dead time measurement point example

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HIGH POWER SWITCHING USE

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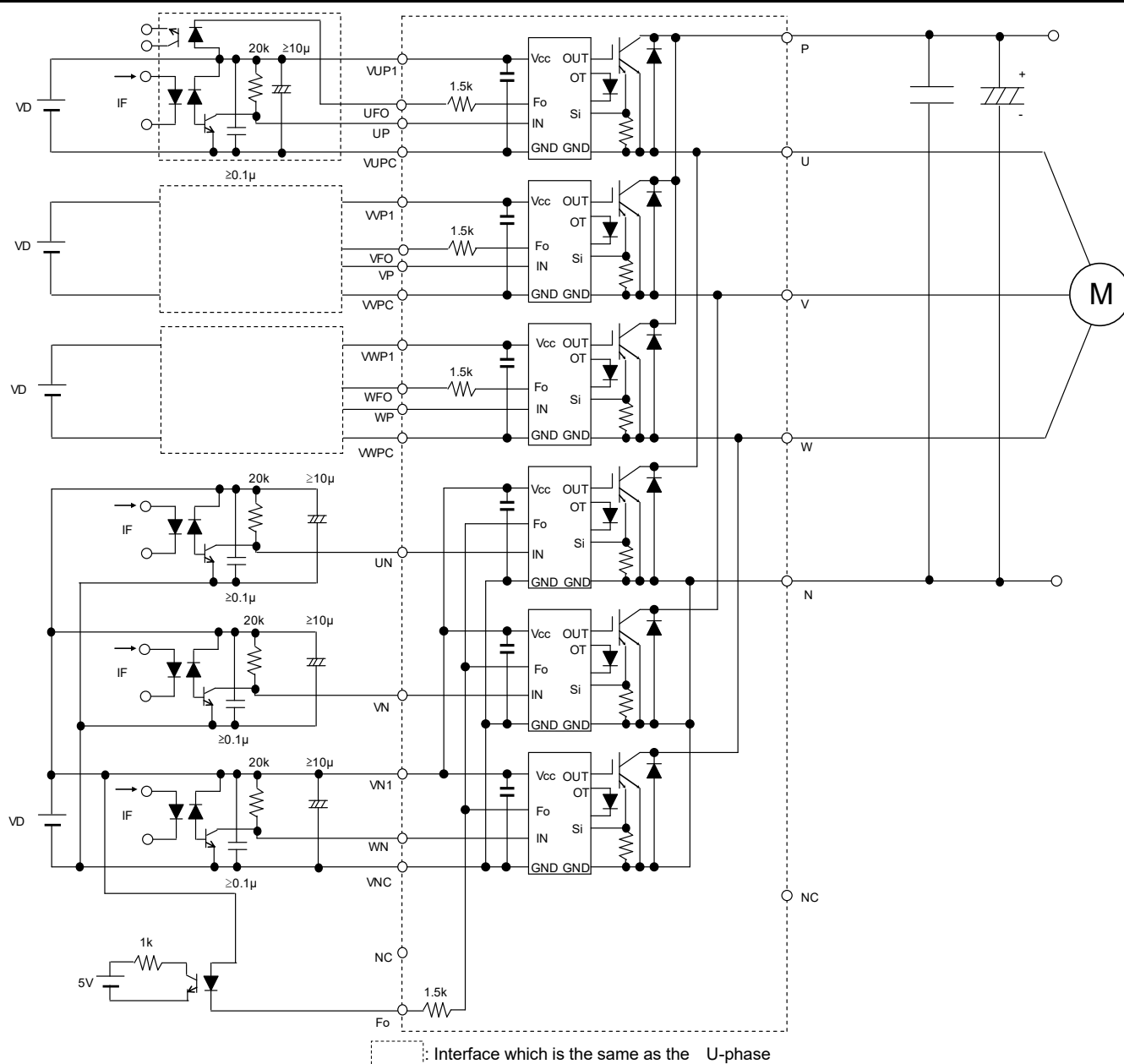
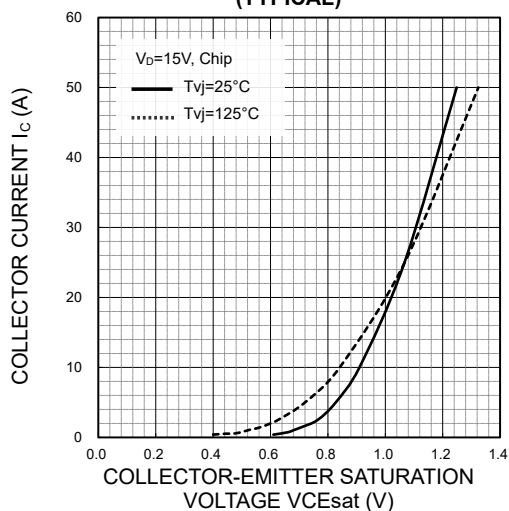
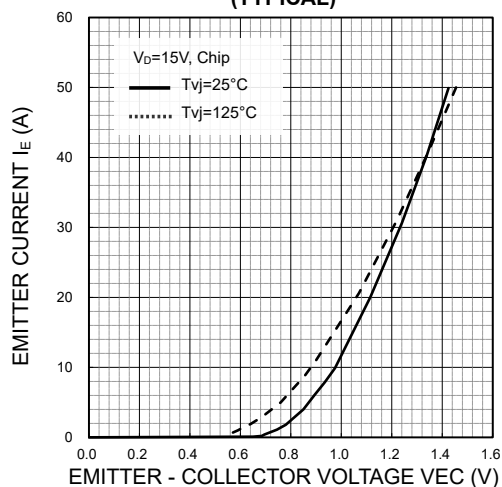
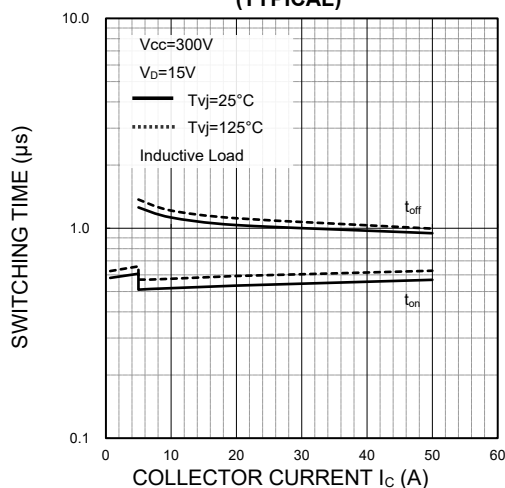
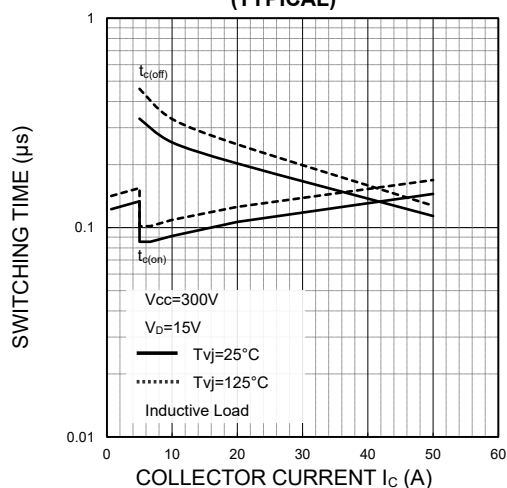
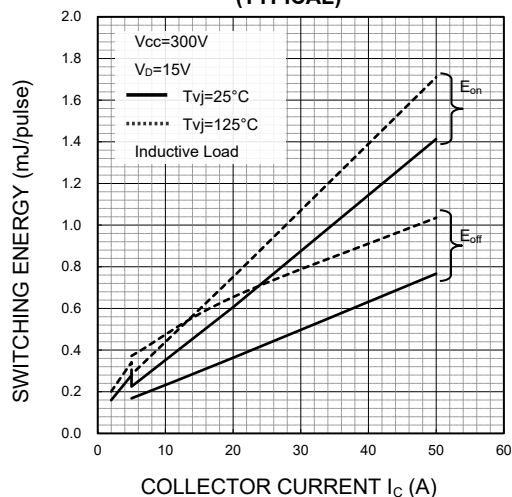
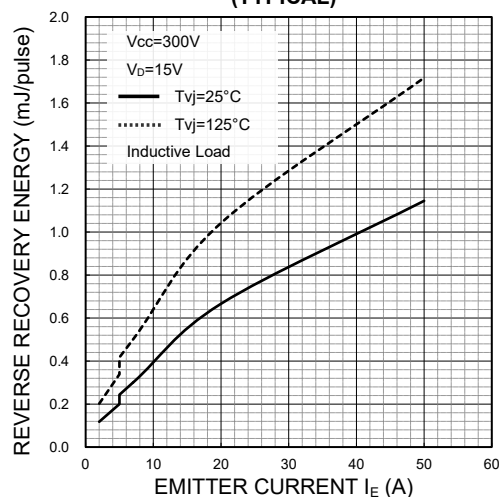


Fig. 8 Application Example Circuit

**NOTES FOR STABLE AND SAFE OPERATION ;**

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers:  $t_{PLH}$ ,  $t_{PHL} \leq 0.8\mu s$ , Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 4 isolated control power supplies ( $V_D$ ). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.

## PERFORMANCE CURVES

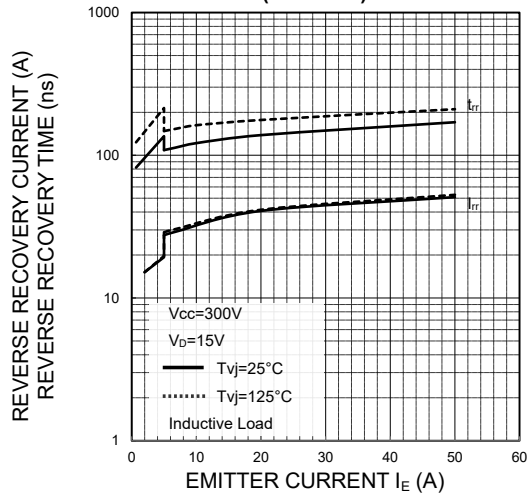
COLLECTOR-EMITTER SATURATION  
VOLTAGE (VS.  $I_C$ ) CHARACTERISTICS  
(TYPICAL)FREE WHEELING DIODE FORWARD  
CHARACTERISTICS  
(TYPICAL)SWITCHING TIME ( $t_{on}$ ,  $t_{off}$ )  
CHARACTERISTICS  
(TYPICAL)SWITCHING TIME ( $t_{c(on)}$ ,  $t_{c(off)}$ )  
CHARACTERISTICS  
(TYPICAL)SWITCHING ENERGY CHARACTERISTICS  
(TYPICAL)FREE WHEELING DIODE REVERSE  
RECOVERY ENERGY CHARACTERISTICS  
(TYPICAL)

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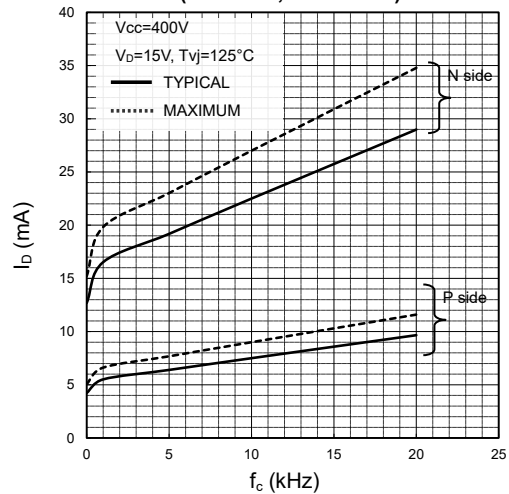
HIGH POWER SWITCHING USE

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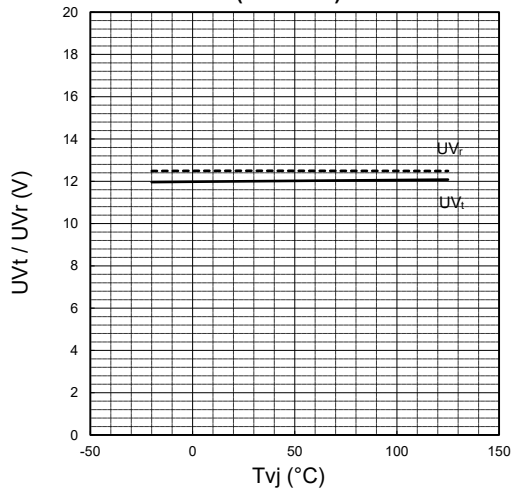
**FREE WHEELING DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)**



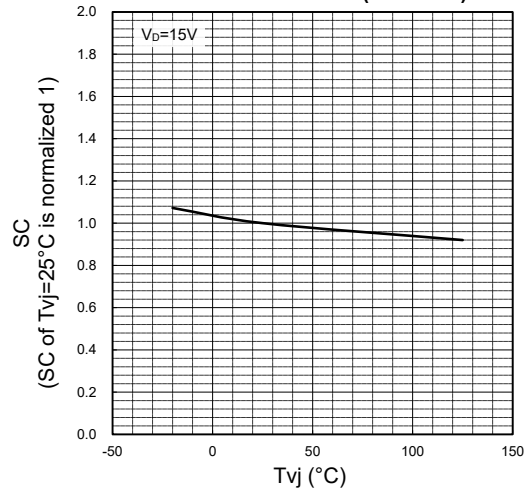
**$I_D$  VS.  $f_c$  CHARACTERISTICS (TYPICAL, MAXIMUM)**



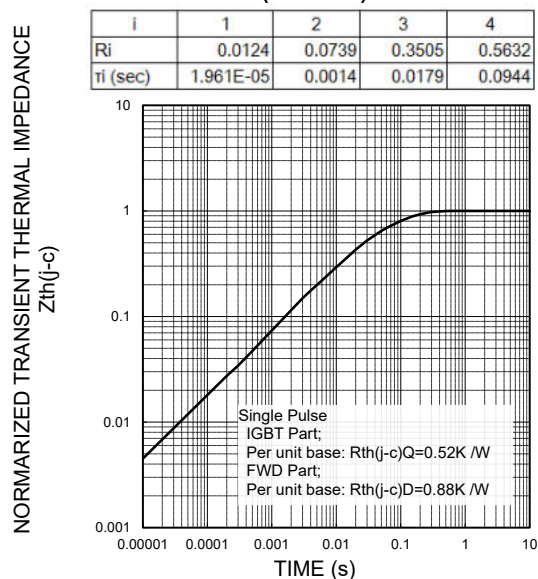
**UV TRIP LEVEL VS.  $T_{vj}$  CHARACTERISTICS (TYPICAL)**



**SC TRIP LEVEL VS.  $T_{vj}$  CHARACTERISTICS (TYPICAL)**



**TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (TYPICAL)**



Note: The characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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