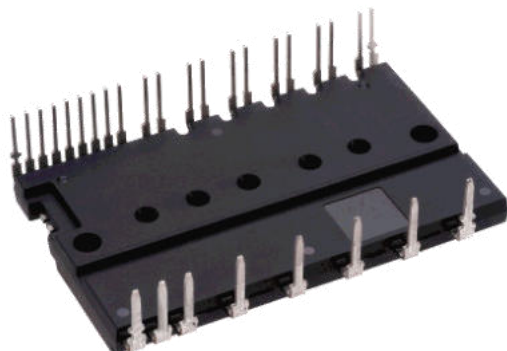


< DIPIPM >

PSS50S73F6

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



MAIN FUNCTION AND RATINGS

- 3 phase DC/AC inverter
- 600V / 50A (CSTBT)
- N-side IGBT open emitter
- Built-in bootstrap diodes with current limiting resistor

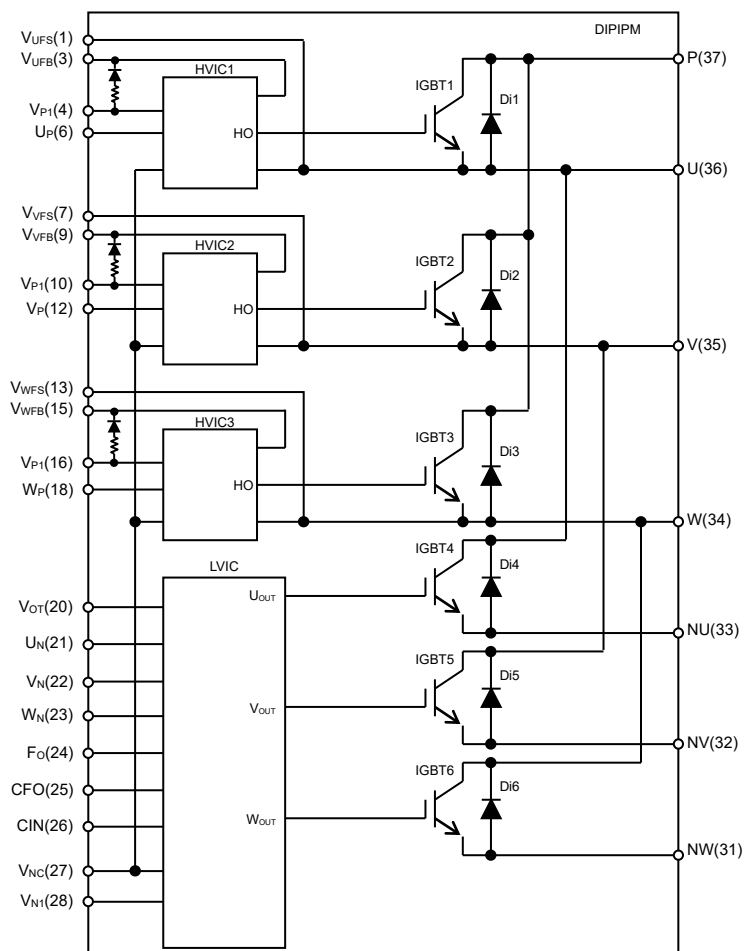
APPLICATION

- AC 100~240Vrms(DC voltage:400V or below) class low power motor control

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC),
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply)
- Temperature output : Outputting LVIC temperature by analog signal
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU, NV, NW	500	V
V_{CES}	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$ (Note 1)	30	A
I_{OP}	Output current (peak)	Sine-wave, $T_C = 25^\circ\text{C}$, $f \geq 1\text{Hz}$	50	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$, less than 1ms	100	A
T_{jop}	Operation junction temperature	Continuous operation (Note 2)	-30~+150	$^\circ\text{C}$
T_{jmax}	Maximum junction temperature	Temporally operation (e.g. overload)	175	$^\circ\text{C}$

Note 1: Pulse width and period are limited due to junction temperature.

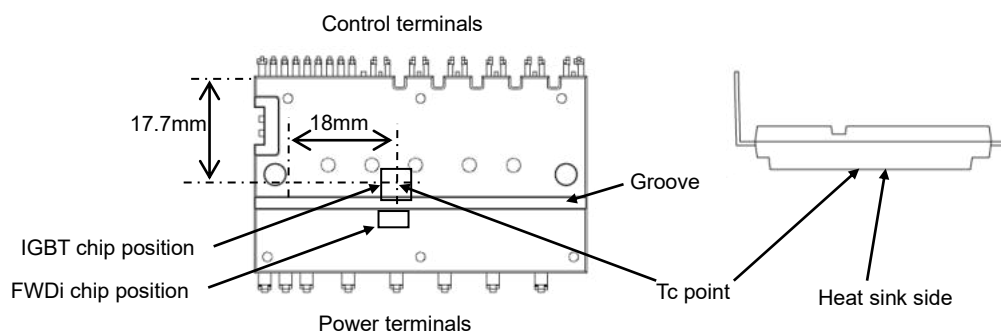
Note 2: The maximum junction temperature rating of built-in power chips is $175^\circ\text{C} (@T_C \leq 125^\circ\text{C})$. However, to ensure safe operation of DIIPM, the average junction temperature should be limited to $T_{j(Ave)} \leq 150^\circ\text{C} (@T_C \leq 125^\circ\text{C})$.

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between $V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$	20	V
V_{DB}	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	20	V
V_{IN}	Input voltage	Applied between U_P , V_P , W_P-V_{PC} , U_N , V_N , W_N-V_{NC}	$-0.5 \sim V_D + 0.5$	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	$-0.5 \sim V_D + 0.5$	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between $CIN-V_{NC}$	$-0.5 \sim V_D + 0.5$	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(Prot)}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5 \sim 16.5\text{V}$, Inverter Part $T_j = 150^\circ\text{C}$, non-repetitive, less than $2\mu\text{s}$	400	V
T_C	Module case operation temperature	Measurement point of T_C is provided in Fig.1	-30~+125	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~+125	$^\circ\text{C}$
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	V_{rms}

Fig. 1: T_C MEASUREMENT POINT**THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	-	-	1.0	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	2.0	K/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about $+100\mu\text{m} \sim +200\mu\text{m}$ on the contacting surface of DIIPM and heat sink. The contacting thermal resistance between DIIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.3K/W (per 1/6 module, grease thickness: $20\mu\text{m}$, thermal conductivity: $1.0\text{W/m}\cdot\text{k}$).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V _{CE(sat)}	Collector-emitter saturation voltage	V _D =V _{DB} = 15V, V _{IN} = 5V	I _C = 50A, T _J = 25°C	-	1.40	1.70	V
			I _C = 50A, T _J = 125°C	-	1.55	1.90	
V _{EC}	FWDi forward voltage	V _{IN} = 0V, -I _C = 50A		-	1.60	2.10	V
t _{on}	Switching times	V _{CC} = 300V, V _D = V _{DB} = 15V I _C = 50A, T _J = 125°C, V _{IN} = 0↔5V Inductive Load (upper-lower arm)		1.05	1.65	2.30	µs
t _{C(on)}				-	0.50	0.80	µs
t _{off}				-	2.00	2.60	µs
t _{C(off)}				-	0.20	0.40	µs
t _{rr}				-	0.60	-	µs
I _{CES}	Collector-emitter cut-off current	V _{CE} =V _{CES}	T _J = 25°C	-	-	1	mA
			T _J = 125°C	-	-	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I _D	Circuit current	Total of V _{P1} -V _{NC} , V _{N1} -V _{NC}	V _D =15V, V _{IN} =0V	-	-	6.00	mA
			V _D =15V, V _{IN} =5V	-	-	6.00	
I _{DB}		Each part of V _{UFB} - V _{UFS} , V _{VFB} - V _{VFS} , V _{WFB} - V _{WFS}	V _D =V _{DB} =15V, V _{IN} =0V	-	-	0.55	
			V _D =V _{DB} =15V, V _{IN} =5V	-	-	0.55	
V _{SC(ref)}	Short circuit trip level	V _D = 15V (Note 4)		0.45	0.48	0.51	V
UV _{DBt}	P-side Control supply under-voltage protection(UV)	T _J ≤125°C	Trip level	10.0	-	12.0	V
UV _{DBr}			Reset level	10.5	-	12.5	V
UV _{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV _{Dr}			Reset level	10.8	-	13.0	V
V _{OT}	Temperature Output	LVIC Temperature=85°C, Pull down R=5.1kΩ (Note 5)		2.51	2.64	2.76	V
V _{FOH}	Fault output voltage	V _{SC} = 0V, F _O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V _{FOL}		V _{SC} = 1V, I _{FO} = 1mA		-	-	0.95	V
t _{FO}	Fault output pulse width	C _{FO} =22nF (Note 6)		1.6	2.4	-	ms
I _{IN}	Input current	V _{IN} = 5V		0.70	1.00	1.50	mA
V _{th(on)}	ON threshold voltage	Applied between U _P , V _P , W _P , U _N , V _N , W _N -V _{NC}		-	2.10	2.60	V
V _{th(off)}	OFF threshold voltage			0.80	1.30	-	
V _{th(hys)}	ON/OFF threshold hysteresis voltage			0.35	0.80	-	
V _F	Bootstrap Di forward voltage	I _F =10mA including voltage drop by limiting resistor (Note 7)		0.5	0.9	1.3	V
R	Built-in limiting resistance	Included in bootstrap Di		16	20	24	Ω

Note 4 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the current rating.

5 : DIIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIIPM. Temperature of LVIC vs. VOT output characteristics is described in Fig. 3.

6 : Fault signal F_O outputs when SC or UV protection works. F_O pulse width is different for each protection modes. At SC failure, F_O pulse width is a fixed width which is specified by the capacitor connected to C_{FO} terminal. ($C_{FO}=9.1 \times 10^{-6} \times t_{FO} [F]$), but at UV failure, F_O outputs continuously until recovering from UV state. (But minimum F_O pulse width is the specified time by C_{FO} .)

7 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of bootstrap Di V_F-I_F curve (@ $T_a=25^\circ\text{C}$) including voltage drop by limiting resistor (Right chart is enlarged chart.)

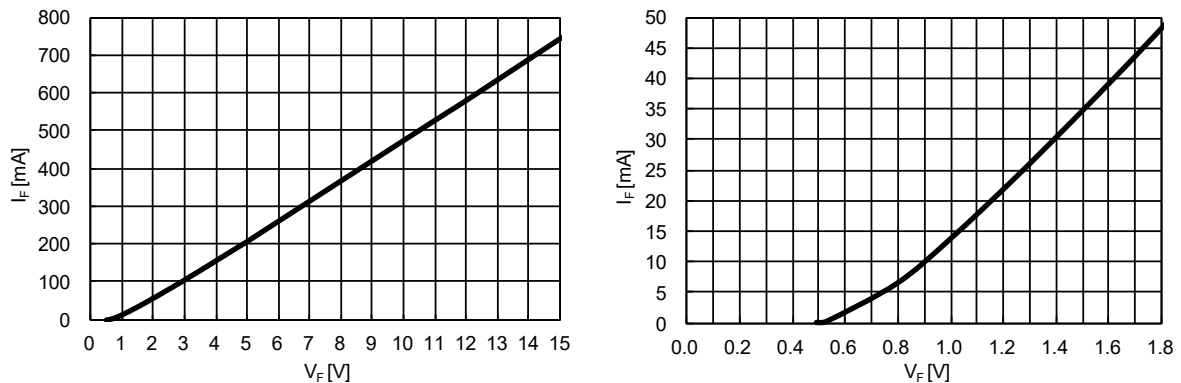
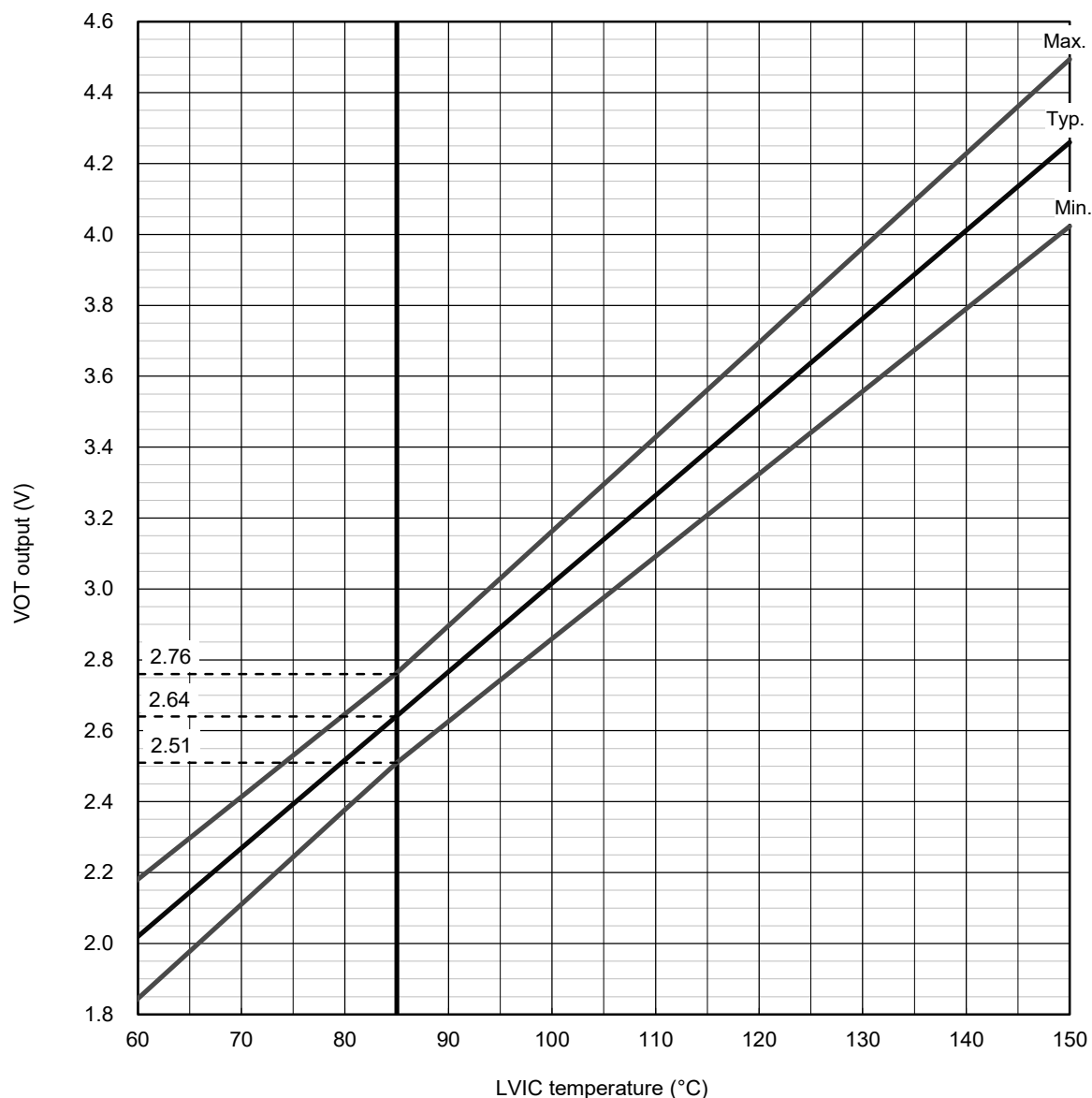
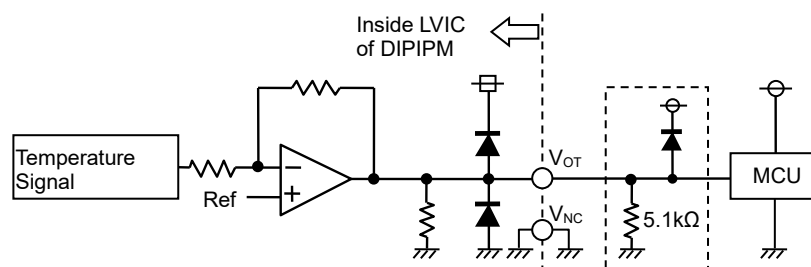


Fig. 3 Temperature of LVIC vs. V_{OT} output characteristicsFig. 4 V_{OT} output circuit

- (1) It is recommended to insert 5kΩ (5.1kΩ is recommended) pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra circuit current, which is calculated approximately by V_{OT} output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V_{OT} for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
- (2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and V_{OT} output for preventing over voltage destruction.
- (3) In the case of not using V_{OT} , leave V_{OT} output NC (No Connection).

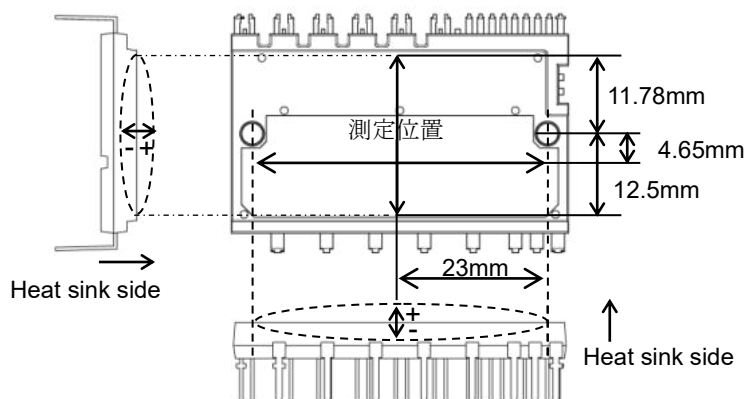
Refer the application note for this product about the usage of V_{OT} .

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Standard	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 8)	JEITA-ED-4701	0.59	0.78	0.98	N·m
Terminal pulling strength	Load 10N	JEITA-ED-4701	10	-	-	s
Terminal bending strength	Load 5N, 90deg. Bend	JEITA-ED-4701	2	-	-	times
Weight		-	-	21	-	g
Heat-sink flatness	(Note 9)	-	-50	-	100	μm

Note 8: Plain washers (ISO 7089~7094) are recommended.

Note 9: Measurement point of heat sink flatness

**RECOMMENDED OPERATION CONDITIONS**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
V_D	Control supply voltage	Applied between V_{P1} - V_{NC} , V_{N1} - V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB} - V_{UFS} , V_{VFB} - V_{VFS} , V_{WFB} - V_{WFS}	13.0	15.0	18.5	V
ΔV_D , ΔV_{DB}	Control supply variation		-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal	2.0	-	-	μs
f_{PWM}	PWM input frequency	$T_C \leq 125^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$	-	-	20	kHz
PWIN(on) PWIN(off)	Minimum input pulse width	(Note 10)	0.7	-	-	μs
			1.5	-	-	
V_{NC}	V_{NC} variation	Between V_{NC} -NU, NV, NW (including surge)	-5.0	-	+5.0	V

Note 10: DIIPM might not make response if the input signal pulse width is less than PWIN(on) / PWIN(off). Moreover, if it makes response to shorter turning off signal than PWIN(off), DIIPM might make delayed response in case of rated current or more. Please refer below about delayed response.

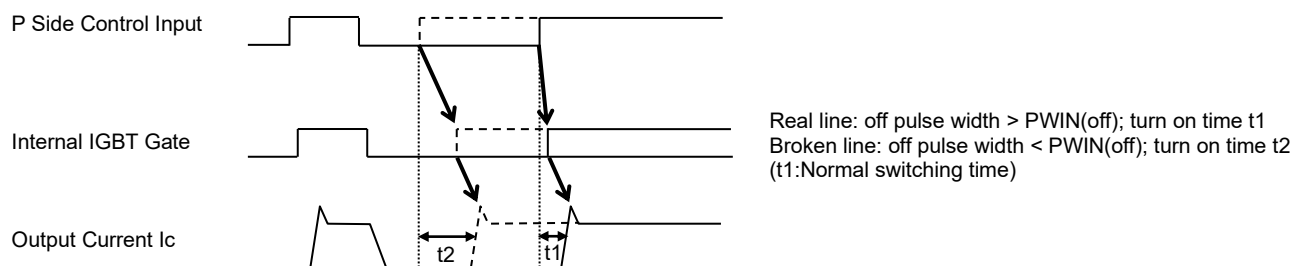
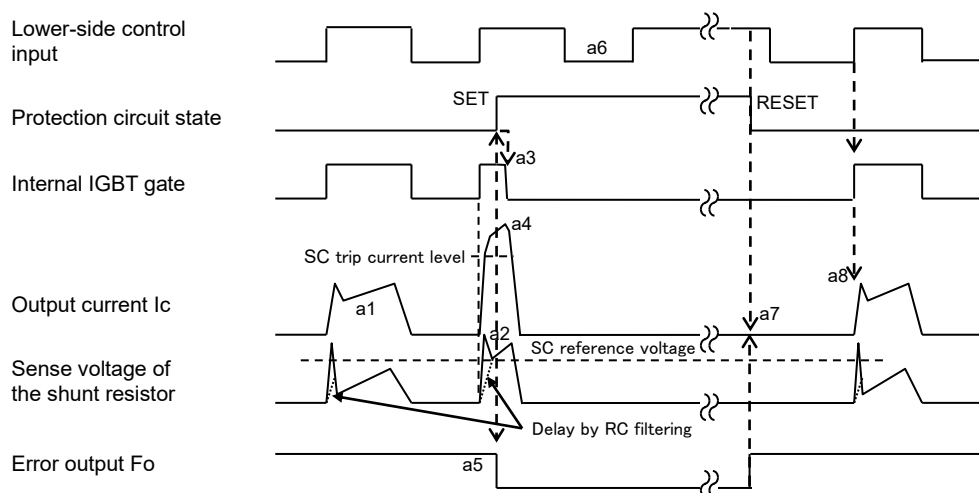
Delayed Response against Shorter Input Off Signal than PWIN(off) (P-side only, above rated current)

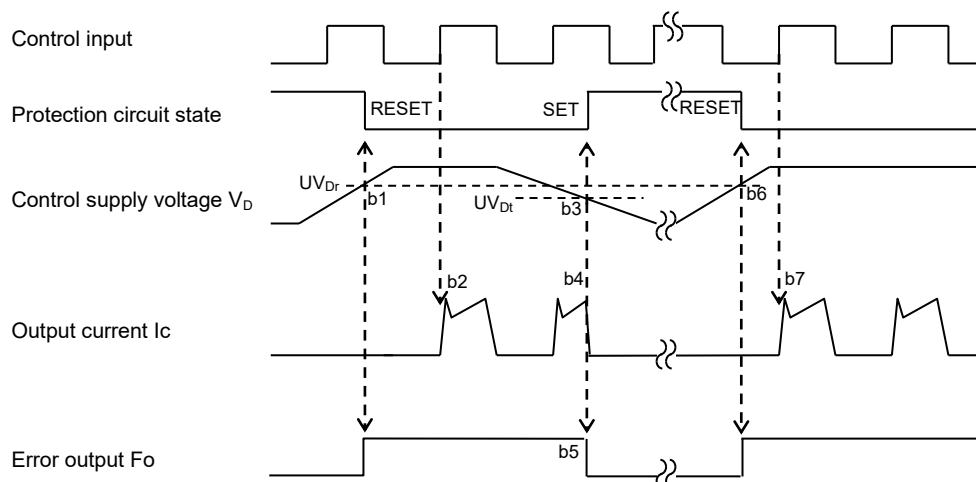
Fig. 5 Timing Charts of The DIIPM Protective Functions

[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger)
(It is recommended to set RC time constant 1.5~2.0 μ s so that IGBT shut down within 2.0 μ s when SC.)
- a3. All N-side IGBT's gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. F_o outputs. The pulse width of the F_o signal is set by the external capacitor C_{FO} .
- a6. Input = "L": IGBT OFF
- a7. F_o finishes output, but IGBTs don't turn on until inputting next ON signal (L $\rightarrow$ H).
- (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.

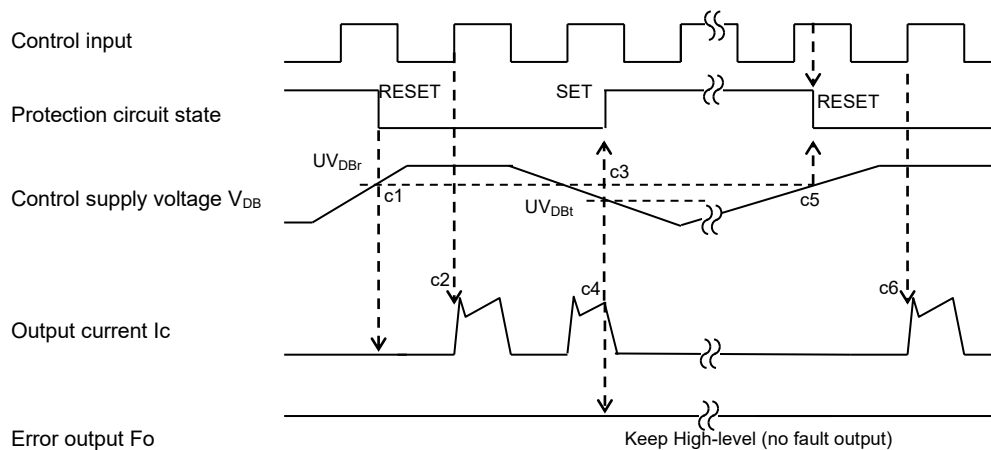
**[B] Under-Voltage Protection (N-side, UV_D)**

- b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal (L $\rightarrow$ H).
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- b2. Normal operation: IGBT ON and outputs current.
- b3. V_D level drops to under voltage trip level. (UV_{Dt}).
- b4. All N-side IGBTs turn OFF in spite of control input condition.
- b5. F_o outputs for the period set by the capacitance C_{FO} , but output is extended during V_D keeps below UV_{Dr} .
- b6. V_D level reaches UV_{Dr} .
- b7. Normal operation: IGBT ON and outputs current.



[C] Under-Voltage Protection (P-side, UV_{DB})

- c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr} , IGBT turns on by next ON signal (L→H).
- c2. Normal operation: IGBT ON and outputs current.
- c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
- c4. IGBT of the correspond phase only turns OFF in spite of control input signal level, but there is no F_o signal output.
- c5. V_{DB} level reaches UV_{DBr} .
- c6. Normal operation: IGBT ON and outputs current.



The diagram illustrates a 3-phase motor driver circuit. It features an MCU connected to three HVICs and one LVIC. The HVICs drive three IGBTs (IGBT1, IGBT2, IGBT3) and the LVIC drives three IGBTs (IGBT4, IGBT5, IGBT6). Each IGBT is paired with a diode (Di1 to Di6). The motor (M) is connected to the output of the IGBTs. The circuit includes various pins (V_UFB, V_UFS, V_P1, U_P, V_WFB, V_WFS, V_P1, W_P, V_OT, U_N, V_N, W_N, F_O, C_FO, V_N1, V_NC, C_IN, B, A, C, D, N1) and components like capacitors (C1, C2, C3, C4), resistors (R1, R2), and a shunt resistor. Annotations highlight potential issues: 'Long wiring here might cause SC level short circuit failure.' and 'Long wiring here might cause SC level fluctuation and malfunction.'

- (1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
- (2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.
- (3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.
- (4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is recommended generally.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
- (5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
- (6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals when it is used by one shunt operation. Low inductance SMD type with tight tolerance, temp-compensated type is recommended for shunt resistor.
- (7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
- (8) Input logic is High-active. There is a 3.3kΩ(min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the input wiring should be as short as possible. When using RC coupling, make the input signal level meet the turn-on and turn-off threshold voltage.
- (9) Fo output is open drain type. It should be pulled up to power supply of MCU (e.g. 5V,3.3V) by a resistor that makes I_{Fo} up to 1mA. (I_{Fo} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.) When using opto coupler, Fo also can be pulled up to 15V (control supply of DIPIPM) by the resistor.
- (10) Fo pulse width can be set by the capacitor connected to CFO terminal. $C_{Fo}(F) = 9.1 \times 10^{-6} \times t_{Fo}$ (Required Fo pulse width).
- (11) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet $dV/dt \leq \pm 1V/\mu s$, $V_{ripple} \leq 2V_p-p$.
- (12) For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIPIPM.

The diagram illustrates the DIPIM input stage circuit. It features an MCU connected to a 5V line through a 10kΩ resistor. The 5V line is also connected to the DIPIM's $U_P, V_P, W_P, U_N, V_N, W_N$ inputs. The MCU's output is connected to the DIPIM's F_o input through a 3.3kΩ resistor. The DIPIM's $V_{NC}(\text{Logic})$ input is connected to ground. The DIPIM's output is connected to an op-amp.

Fo output is open drain type. It should be pulled up to control power supply (e.g. 5V, 15V) with a resistor that makes Fo sink current I_{Fo} 1mA or less. In the case of pulled up to 5V supply, 10k Ω (5k Ω or more) is recommended.

DIPIPM

NU, NV, NW should be connected each other at near terminals.

Wiring Inductance should be less than 10nH.
 (Inductance of a copper pattern with length=17mm, width=3mm is about 10nH.)

NU
NV
NW

V_{NC}

Shunt resistor

N1

GND wiring from V_{NC} should be connected close to the terminal of shunt resistor.

DIPIPM

Each wiring Inductance should be less than 10nH.
 (Inductance of a copper pattern with length=17mm, width=3mm is about 10nH.)

NU
NV
NW

V_{NC}

Shunt resistors

N1

GND wiring from V_{NC} should be connected close to the terminal of shunt resistor.

- (1) It is necessary to set the time constant $R_f C_f$ of external comparator input so that IGBT stops within $2\mu s$ when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
- (2) It is recommended for the threshold voltage V_{ref} to set to the same rating of short circuit trip level ($V_{sc(ref)}$: typ. 0.48V).
- (3) Select the external shunt resistance so that SC trip-level is less than specified value (≈ 2.0 times of rating current).
- (4) To avoid malfunction, the wiring A, B, C should be as short as possible.
- (5) The point D at which the wiring to comparator is divided should be close to the terminal of shunt resistor.
- (6) OR output high level when protection works should be over 0.51V ($\approx$ maximum $V_{sc(ref)}$ rating).
- (7) GND of Comparator, GND of V_{ref} circuit and C_f should be not connected to power GND but to control GND wiring.

Fig. 10 (Reference Figure) PCB Through-hole Pattern

Recommended through-hole locations and diameter layout for PSS**S73F6

[Dimension: mm]

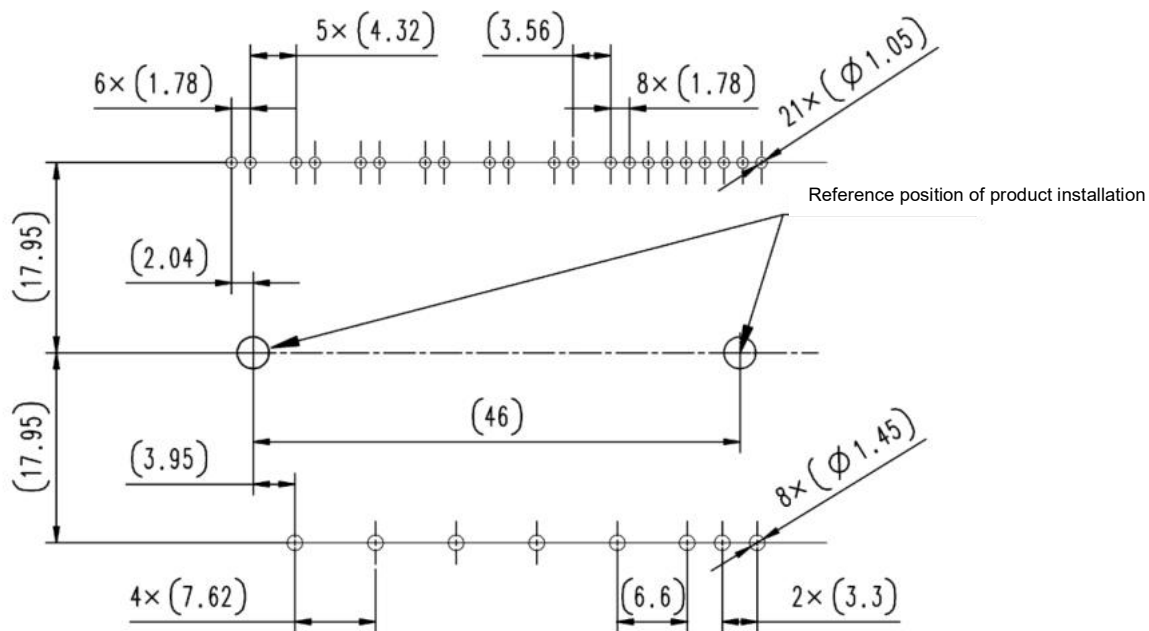
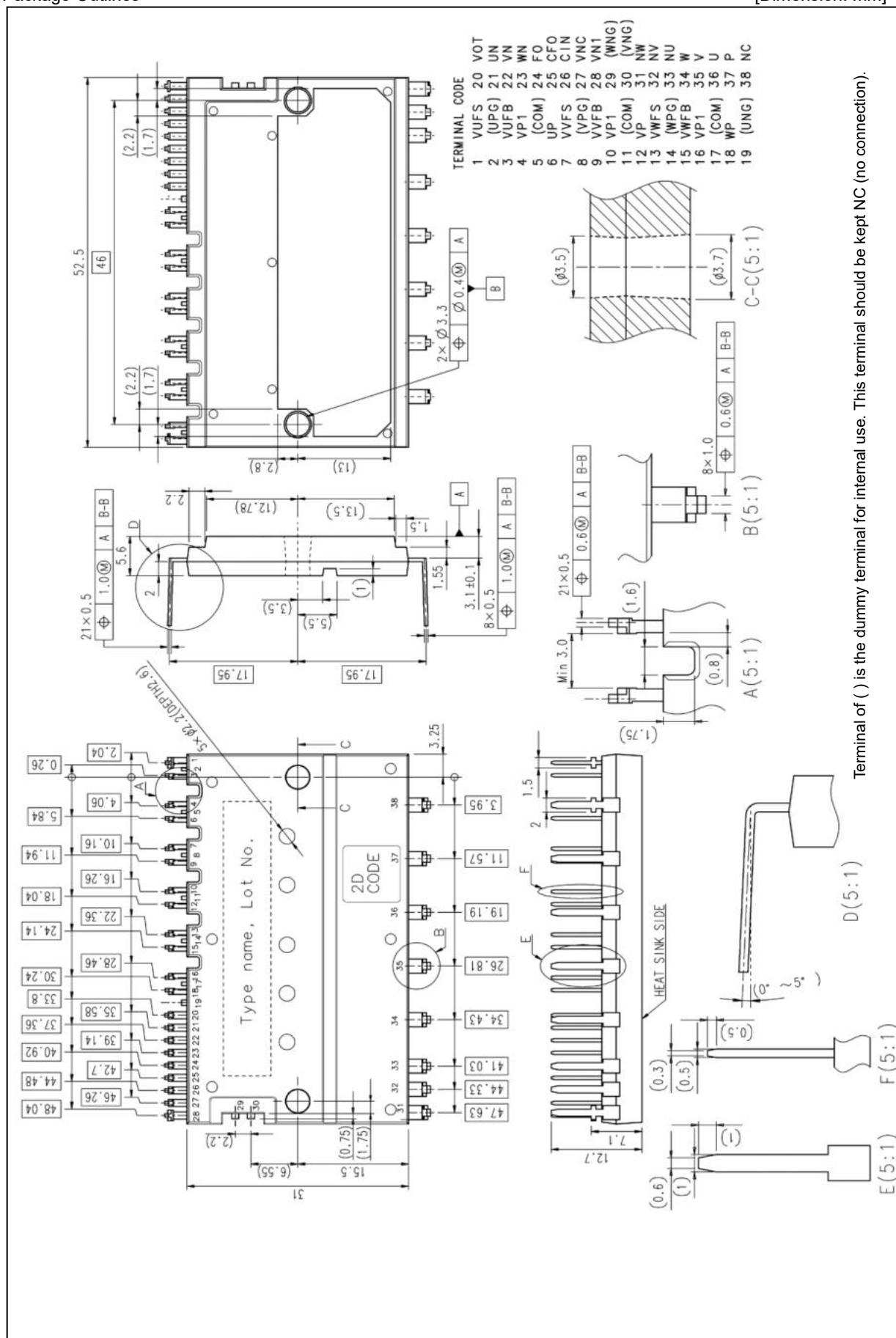


Fig. 11 Package Outlines

[Dimension: mm]



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sonal injury.

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e. As required, pay close attention to the safety design by installing appropriate fuse or circuit breaker between a power supply and semiconductor products to prevent secondary damage. Please also pay attention to the application note and the related technical information.

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