
# 2.7 inch
# E-paper Display Series

# WAA0270A2AAA7NXXX000

# Product Specifications

| | |
|---|---|
| **Customer** | **Standard** |
| **Description** | **2.7” E-PAPER DISPLAY** |
| **Model Name** | **WAA0270A2AAA7NXXX000** |
| **Date** | **2025/02/12** |
| **Revision** | **1.0** |

| | Design Engineering | | |
|---|---|---|---|
| | **Approval** | **Check** | **Design** |
| | | | |

# REVISION HISTORY

| Rev | Date | Item | Page | Remark |
|---|---|---|---|---|
| 1.0 | 02.12.2025 | New Creation | ALL | |

# CONTENTS

# 1. Over View

WAA0270A2AAA7NXXX000 is an Active Matrix Electrophoretic Display (AM EPD), with front light panel. The display is capable to display image at 1-bit white, black full display capabilities. The 2.7inch active area contains 264×176pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

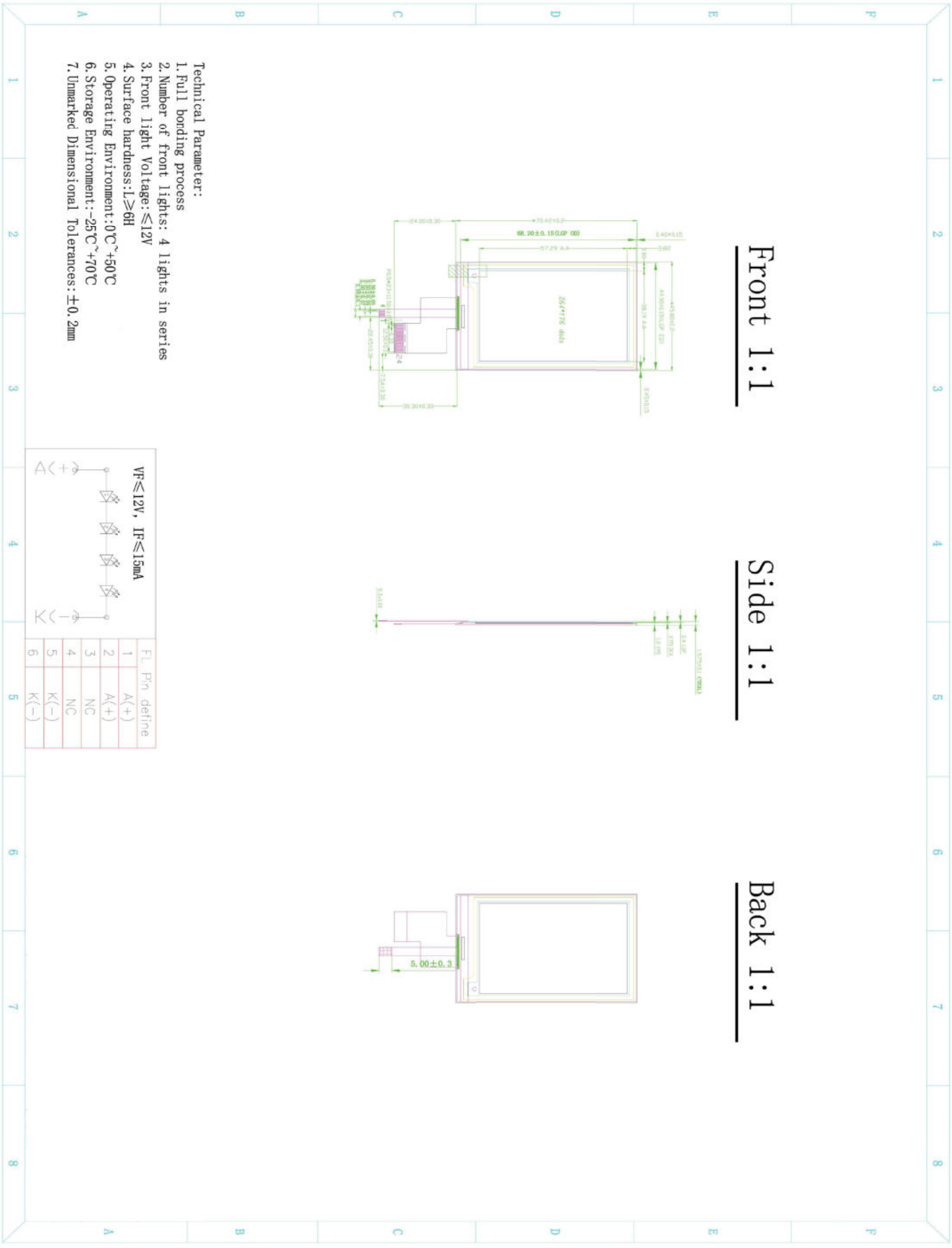
# 2.Features

264×176 pixels display
High contrast
High reflectance
Ultra wide viewing angle Ultra low power consumption Pure reflective mode
Bi-stable display
Commercial temperature range
Landscape portrait modes
Hard-coat antiglare display surface
Ultra Low current deep sleep mode
On chip display RAM
Waveform can stored in On-chip OTP or written by MCU
Serial peripheral interface available
On-chip oscillator
On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
I2C signal master interface to read external temperature sensor Built-in temperature sensor
With front light panel, 4 LEDs in serial, operating voltage: 12V

# 3.Mechanical Specifications

| Parameter | Specifications | Unit | Remark |
|---|---|---|---|
| Screen Size | 2.7 | Inch | |
| Display Resolution | 264(H)×176(V) | Pixel | Dpi:117 |
| Active Area | 38.19×57.29 | mm | |
| Pixel Pitch | 0.217×0.217 | mm | |
| Pixel Configuration | Rectangle | | |
| Outline Dimension | 45.8 (H)×70.42(V) ×1.58(D) | mm | |
| Weight | 8.84±0.5 | g | |

# 4. Mechanical Drawing of EPD module



## 5. Input /Output Pin Assignment

| No. | Name | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | NC | | Do not connect with other NC pins | Keep Open |
| 2 | GDR | O | N-Channel MOSFET Gate Drive Control | |
| 3 | RESE | I | Current Sense Input for the Control Loop | |
| 4 | NC | NC | Do not connect with other NC pins | Keep Open |
| 5 | VSH2 | C | Positive Source driving voltage(Red) | |
| 6 | TSCL | O | $I^2C$ Interface to digital temperature sensor Clock pin | |
| 7 | TSDA | I/O | $I^2C$ Interface to digital temperature sensor Data pin | |
| 8 | BS1 | I | Bus Interface selection pin | Note 5-5 |
| 9 | BUSY | O | Busy state output pin | Note 5-4 |
| 10 | RES# | I | Reset signal input. Active Low. | Note 5-3 |
| 11 | D/C# | I | Data /Command control pin | Note 5-2 |
| 12 | CS# | I | Chip select input pin | Note 5-1 |
| 13 | SCL | I | Serial Clock pin (SPI) | |
| 14 | SDA | I | Serial Data pin (SPI) | |
| 15 | VDDIO | P | Power Supply for interface logic pins It should be connected with VCI | |
| 16 | VCI | P | Power Supply for the chip | |
| 17 | VSS | P | Ground | |
| 18 | VDD | C | Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS | |
| 19 | VPP | P | FOR TEST | |
| 20 | VSH1 | C | Positive Source driving voltage | |
| 21 | VGH | C | Power Supply pin for Positive Gate driving voltage and VSH1 | |
| 22 | VSL | C | Negative Source driving voltage | |
| 23 | VGL | C | Power Supply pin for Negative Gate driving voltage VCOM and VSL | |
| 24 | VCOM | C | VCOM driving voltage | |

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

**Note 5-1:** This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.
**Note 5-2:** This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.
**Note 5-3:** This pin (RES#) is reset signal input. The Reset is active low.
**Note 5-4:** This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when –Outputting display waveform -Communicating with digital temperature sensor

**Note 5-5:** Bus interface selection pin

| BS1 State | MCU Interface |
|---|---|
| L | 4-lines serial peripheral interface(SPI) - 8 bits SPI |
| H | 3- lines serial peripheral interface(SPI) - 9 bits SPI |

# 6. Electrical Characteristics
## 6.1 Absolute Maximum Rating

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Logic supply voltage | VCI | -0.5 to +6.0 | V |
| Logic Input voltage | VIN | -0.5 to VCI +0.5 | V |
| Logic Output voltage | VOUT | -0.5 to VCI +0.5 | V |
| Operating Temp range | TOPR | 0 to +50 | °C |
| Storage Temp range | TSTG | -25 to+70 | °C |
| Optimal Storage Humidity | HSTGo | 55±10 | %RH |

**Note:**

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

## 6.2 Panel DC Characteristics

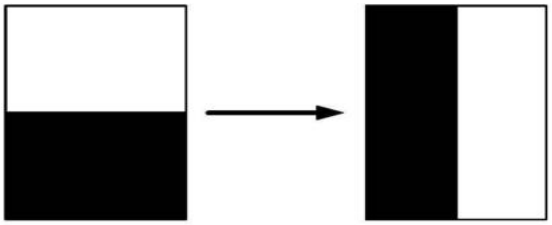
The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25ºC.

| Parameter | Symbol | Conditions | Applicable pin | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|---|
| Single ground | $V_{SS}$ | -- | | - | 0 | - | V |
| Logic supply voltage | $V_{CI}$ | | VCI | 2.2 | 3.0 | 3.7 | V |
| Core logic voltage | $V_{DD}$ | | VDD | 1.7 | 1.8 | 1.9 | V |
| High level input voltage | $V_{IH}$ | - | -- | 0.8 $V_{CI}$ | - | - | V |
| Low level input voltage | $V_{IL}$ | - | -- | - | - | 0.2 $V_{CI}$ | V |
| High level output voltage | $V_{OH}$ | IOH = - 100uA | -- | 0.9 VCI | - | - | V |
| Low level output voltage | $V_{OL}$ | IOL = 100uA | -- | -- | - | 0.1 $V_{CI}$ | V |
| Typical power | $P_{TYP}$ | $V_{CI}$ =3.0V | -- | -- | 9 | -- | mW |
| Deep sleep mode | $P_{STPY}$ | $V_{CI}$ =3.0V | | -- | 0.003 | -- | mW |
| Typical operating current | Iopr_$V_{CI}$ | $V_{CI}$ =3.0V | | - | 3 | -- | mA |
| Full update time | -- | 25 ℃ | | | 3 | | sec |
| Fast update time | - | 25 ℃ | | | 1.5 | | sec |
| Partial update time | | 25 ℃ | | | 0.42 | | sec |
| Sleep mode current | Islp_$V_{CI}$ | DC/ DC off<br>No clock<br>No input load<br>Ram data retain | - | - | 20 | | uA |
| Deep sleep mode current | Idslp_$V_{CI}$ | DC/ DC off<br>No clock<br>No input load<br>Ram data not retain | - | - | 1 | 5 | uA |

Notes:
1) Refresh time: the time it takes for the whole process from the screen change to the screen stabilization.
2) The difference between different refresh methods:
Full refresh: The screen will flicker several times during the refresh process;
Fast Refresh: The screen will flash once during the refresh process;
Partial refresh: The screen does not flicker during the refresh process.

During the fast refresh or partial refresh of the electronic paper, it is recommended to add a full-screen refresh after 5 consecutive operations to reduce the accumulation of afterimages on the screen.

1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.
2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by WINSTAR DISPLAY.



## 6.3 Panel AC Characteristics

### 6.3.1 MCU Interface Selection

MCU interface is pin selectable by BS1 shown in Table 6-1.

**Table 6-1 : Interface pins assignment under different MCU interface**

| | Pin Name | | | | | |
|---|---|---|---|---|---|---|
| MCU Interface | BS1 | RES# | CS# | D/C# | SCL | SDA |
| 4-wire serial peripheral interface (SPI) | L | RES# | CS# | DC# | SCL | SDA |
| 3-wire serial peripheral interface (SPI) – 9 bits SPI | H | RES# | CS# | L | SCL | SDA |

Note：(1) L is connected to VSS and H is connected to VDDIO

### 6.3.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure 4-wire SPI is shown in Table 6-2

**Table 6-2 : Control pins status of 4-wire SPI**

| Function | SCL pin | SDA pin | D/C# pin | CS# pin |
|---|---|---|---|---|
| Write command | ↑ | Command bit | L | L |
| Write data | ↑ | Data bit | H | L |

Note:(1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

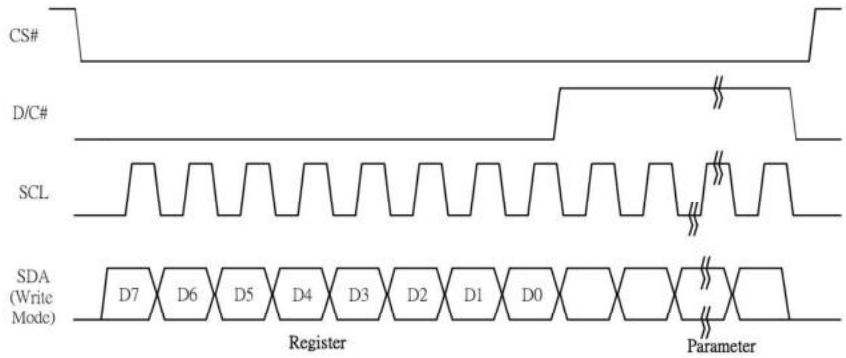



**Figure 6-1 : Write procedure in 4-wire SPI mode**

In the read operation (Command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). After CS # is pulled low, the first byte sent is command byte, D/C# is pulled low. After com mand byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pu lled high. An 8-bit data will be shifted out on every clock falling edge. The serial da ta SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

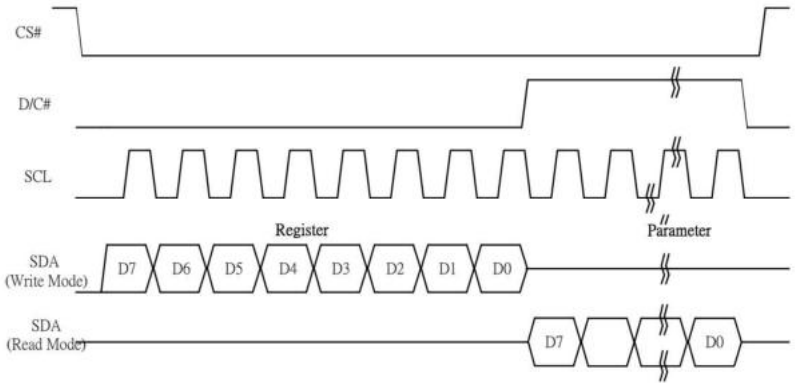



**Figure 6-2 : Read procedure in 4-wire SPI mode**

## 6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

**Table 6-3 : Control pins status of 3-wire SPI**

| Function | SCL pin | SDA pin | D/C# pin | CS# pin |
|---|---|---|---|---|
| Write command | ↑ | Command bit | Tie LOW | L |
| Write data | ↑ | Data bit | Tie LOW | L |

Note: (1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

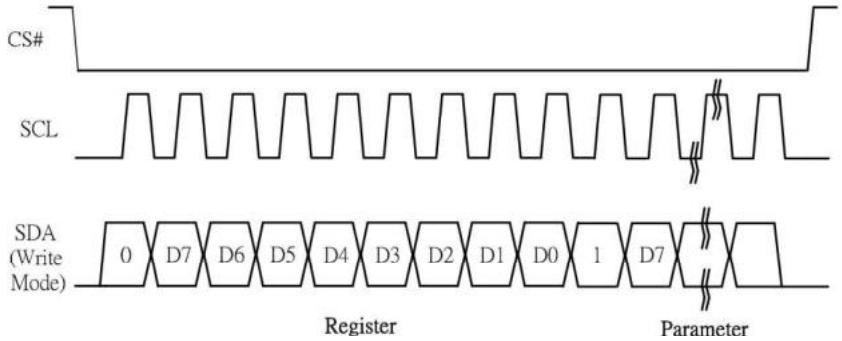



**Figure 6-3 : Write procedure in 3-wire SPI**

In the read operation (Register 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command by te, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1.After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-4 shows the read procedure in 3-wire SPI.

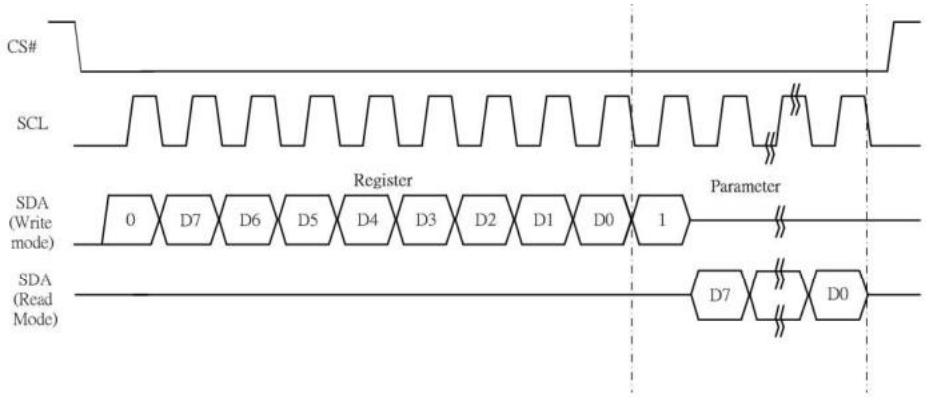



**Figure 6-4 : Read procedure in 3-wire SPI mode**

## 6.3.4 Interface Timing

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, CL=20pF

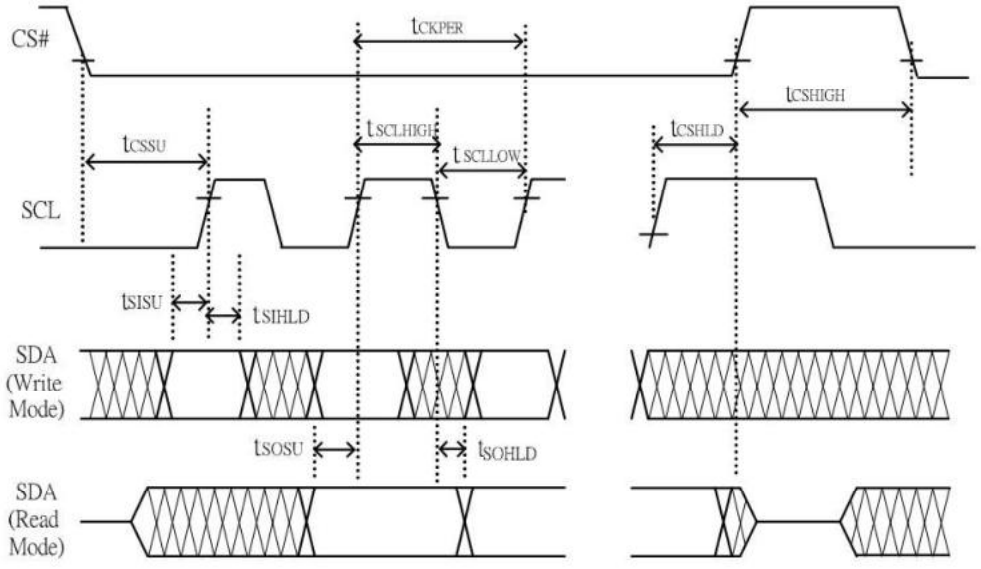
**Write mode**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL frequency (Write Mode) | - | - | 20 | MHz |
| $t_{CSSU}$ | Time CS# has to be low before the first rising edge of SCLK | 60 | - | - | ns |
| $t_{CSHLD}$ | Time CS# has to remain low after the last falling edge of SCLK | 65 | - | - | ns |
| $t_{CSHIGH}$ | Time CS# has to remain high between two transfers | 100 | - | - | ns |
| $t_{SCLHIGH}$ | Part of the clock period where SCL has to remain high | 25 | - | - | ns |
| $t_{SCLLOW}$ | Part of the clock period where SCL has to remain low | 25 | - | - | ns |
| $t_{SISU}$ | Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL | 10 | - | - | ns |
| $t_{SIHLD}$ | Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL | 40 | - | - | ns |

**Read mode**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL frequency (Read Mode) | - | - | 2.5 | MHz |
| $t_{CSSU}$ | Time CS# has to be low before the first rising edge of SCLK | 100 | - | - | ns |
| $t_{CSHLD}$ | Time CS# has to remain low after the last falling edge of SCLK | 50 | - | - | ns |
| $t_{CSHIGH}$ | Time CS# has to remain high between two transfers | 250 | - | - | ns |
| $t_{SCLHIGH}$ | Part of the clock period where SCL has to remain high | 180 | - | - | ns |
| $t_{SCLLOW}$ | Part of the clock period where SCL has to remain low | 180 | - | - | ns |
| $t_{SOSU}$ | Time SO(SDA Read Mode) will be stable before the next rising edge of SCL | - | 50 | - | ns |
| $t_{SOHLD}$ | Time SO (SDA Read Mode) will remain stable after the falling edge of SCL | - | 0 | - | ns |

Note: All timings are based on 20% to 80% of VDDIO-VSS



## 7. Command Table

<table>
<tr><th colspan="12">Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output control</td><td rowspan="4">Gate setting<br>A[8:0]= 127h [POR], 296 MUX<br>MUX Gate lines setting as (A[8:0] + 1).<br><br>B [2:0] = 000 [POR].<br>Gate scanning sequence and direction<br><br>B[2]: GD<br>Selects the 1st output Gate<br>GD=0 [POR],<br>G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, …<br>GD=1,<br>G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, …<br><br>B[1]: SM<br>Change scanning order of gate driver.<br>SM=0 [POR],<br>G0, G1, G2, G3…295 (left and right gate interlaced)<br>SM=1,<br>G0, G2, G4 …G294, G1, G3, …G295<br><br>B[0]: TB<br>TB = 0 [POR], scan from G0 to G295<br>TB = 1, scan from G295 to G0.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate Driving voltage Control</td><td rowspan="2">Set Gate driving voltage<br>A[4:0] = 00h [POR]<br>VGH setting from 10V to 20V<br>
<table>
<tr><th>A[4:0]</th><th>VGH</th><th>A[4:0]</th><th>VGH</th></tr>
<tr><td>00h</td><td>20</td><td>0Dh</td><td>15</td></tr>
<tr><td>03h</td><td>10</td><td>0Eh</td><td>15.5</td></tr>
<tr><td>04h</td><td>10.5</td><td>0Fh</td><td>16</td></tr>
<tr><td>05h</td><td>11</td><td>10h</td><td>16.5</td></tr>
<tr><td>06h</td><td>11.5</td><td>11h</td><td>17</td></tr>
<tr><td>07h</td><td>12</td><td>12h</td><td>17.5</td></tr>
<tr><td>08h</td><td>12.5</td><td>13h</td><td>18</td></tr>
<tr><td>07h</td><td>12</td><td>14h</td><td>18.5</td></tr>
<tr><td>08h</td><td>12.5</td><td>15h</td><td>19</td></tr>
<tr><td>09h</td><td>13</td><td>16h</td><td>19.5</td></tr>
<tr><td>0Ah</td><td>13.5</td><td>17h</td><td>20</td></tr>
<tr><td>0Bh</td><td>14</td><td>Other</td><td>NA</td></tr>
<tr><td>0Ch</td><td>14.5</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

**Command Table**

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 04 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Source Driving voltage Control | Set Source driving voltage<br>A[7:0] = 41h [POR], VSH1 at 15V<br>B [7:0] = A8h [POR], VSH2 at 5V.<br>C[7:0] = 32h [POR], VSL at -15V<br>Remark: VSH1>=VSH2 |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 1 | | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 0 | 1 | | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | | |

A[7]/B[7] = 1,
VSH1/VSH2 voltage setting from 2.4V to 8.8V

| A/B[7:0] | VSH1/VSH2 | A/B[7:0] | VSH1/VSH2 |
|---|---|---|---|
| 8Eh | 2.4 | AFh | 5.7 |
| 8Fh | 2.5 | B0h | 5.8 |
| 90h | 2.6 | B1h | 5.9 |
| 91h | 2.7 | B2h | 6 |
| 92h | 2.8 | B3h | 6.1 |
| 93h | 2.9 | B4h | 6.2 |
| 94h | 3 | B5h | 6.3 |
| 95h | 3.1 | B6h | 6.4 |
| 96h | 3.2 | B7h | 6.5 |
| 97h | 3.3 | B8h | 6.6 |
| 98h | 3.4 | B9h | 6.7 |
| 99h | 3.5 | BAh | 6.8 |
| 9Ah | 3.6 | BBh | 6.9 |
| 9Bh | 3.7 | BCh | 7 |
| 9Ch | 3.8 | BDh | 7.1 |
| 9Dh | 3.9 | BEh | 7.2 |
| 9Eh | 4 | BFh | 7.3 |
| 9Fh | 4.1 | C0h | 7.4 |
| A0h | 4.2 | C1h | 7.5 |
| A1h | 4.3 | C2h | 7.6 |
| A2h | 4.4 | C3h | 7.7 |
| A3h | 4.5 | C4h | 7.8 |
| A4h | 4.6 | C5h | 7.9 |
| A5h | 4.7 | C6h | 8 |
| A6h | 4.8 | C7h | 8.1 |
| A7h | 4.9 | C8h | 8.2 |
| A8h | 5 | C9h | 8.3 |
| A9h | 5.1 | CAh | 8.4 |
| AAh | 5.2 | CBh | 8.5 |
| ABh | 5.3 | CCh | 8.6 |
| ACh | 5.4 | CDh | 8.7 |
| ADh | 5.5 | CEh | 8.8 |
| AEh | 5.6 | Other | NA |

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

| A/B[7:0] | VSH1/VSH2 | A/B[7:0] | VSH1/VSH2 |
|---|---|---|---|
| 23h | 9 | 3Ch | 14 |
| 24h | 9.2 | 3Dh | 14.2 |
| 25h | 9.4 | 3Eh | 14.4 |
| 26h | 9.6 | 3Fh | 14.6 |
| 27h | 9.8 | 40h | 14.8 |
| 28h | 10 | 41h | 15 |
| 29h | 10.2 | 42h | 15.2 |
| 2Ah | 10.4 | 43h | 15.4 |
| 2Bh | 10.6 | 44h | 15.6 |
| 2Ch | 10.8 | 45h | 15.8 |
| 2Dh | 11 | 46h | 16 |
| 2Eh | 11.2 | 47h | 16.2 |
| 2Fh | 11.4 | 48h | 16.4 |
| 30h | 11.6 | 49h | 16.6 |
| 31h | 11.8 | 4Ah | 16.8 |
| 32h | 12 | 4Bh | 17 |
| 33h | 12.2 | Other | NA |
| 34h | 12.4 | | |
| 35h | 12.6 | | |
| 36h | 12.8 | | |
| 37h | 13 | | |
| 38h | 13.2 | | |
| 39h | 13.4 | | |
| 3Ah | 13.6 | | |
| 3Bh | 13.8 | | |

C[7] = 0,
VSL setting from -5V to -17V

| C[7:0] | VSL |
|---|---|
| 0Ah | -5 |
| 0Ch | -5.5 |
| 0Eh | -6 |
| 10h | -6.5 |
| 12h | -7 |
| 14h | -7.5 |
| 16h | -8 |
| 18h | -8.5 |
| 1Ah | -9 |
| 1Ch | -9.5 |
| 1Eh | -10 |
| 20h | -10.5 |
| 22h | -11 |
| 24h | -11.5 |
| 26h | -12 |
| 28h | -12.5 |
| 2Ah | -13 |
| 2Ch | -13.5 |
| 2Eh | -14 |
| 30h | -14.5 |
| 32h | -15 |
| 34h | -15.5 |
| 36h | -16 |
| 38h | -16.5 |
| 3Ah | -17 |
| Other | NA |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 08 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Initial Code Setting<br>OTP Program | Program Initial Code Setting<br><br>The command required CLKEN=1.<br>Refer to Register 0x22 for detail.<br>BUSY pad will output high during operation. |
| 0 | 0 | 09 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | Write Register for Initial Code Setting | Write Register for Initial Code Setting Selection<br>A[7:0] ~ D[7:0]: Reserved<br>Details refer to Application Notes of Initial Code Setting |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 1 | | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 0 | 1 | | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | | |
| 0 | 1 | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | | |
| 0 | 0 | 0A | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Read Register for Initial Code Setting | Read Register for Initial Code Setting |

**Command Table**

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0C | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Booster Soft start Control | Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. |
| 0 | 1 | | 1 | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] |
| 0 | 1 | | 1 | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] |
| 0 | 1 | | 1 | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | | C[7:0] -> Soft start setting for Phase3 = 96h [POR] |
| 0 | 1 | | 0 | 0 | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | | D[7:0] -> Duration setting = 0Fh [POR] |

Bit Description of each byte:
A[6:0] / B[6:0] / C[6:0]:

| Bit[6:4] | Driving Strength Selection |
|---|---|
| 000 | 1(Weakest) |
| 001 | 2 |
| 010 | 3 |
| 011 | 4 |
| 100 | 5 |
| 101 | 6 |
| 110 | 7 |
| 111 | 8(Strongest) |

| Bit[3:0] | Min Off Time Setting of GDR [ Time unit ] |
|---|---|
| 0000 ~ 0011 | NA |
| 0100 | 2.6 |
| 0101 | 3.2 |
| 0110 | 3.9 |
| 0111 | 4.6 |
| 1000 | 5.4 |
| 1001 | 6.3 |
| 1010 | 7.3 |
| 1011 | 8.4 |
| 1100 | 9.8 |
| 1101 | 11.5 |
| 1110 | 13.8 |
| 1111 | 16.5 |

D[5:0]: duration setting of phase
D[5:4]: duration setting of phase 3
D[3:2]: duration setting of phase 2
D[1:0]: duration setting of phase 1

| Bit[1:0] | Duration of Phase [Approximation] |
|---|---|
| 00 | 10ms |
| 01 | 20ms |
| 10 | 30ms |
| 11 | 40ms |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 10 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Deep Sleep mode | Deep Sleep mode Control: |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | $A_1$ | $A_0$ | | |

| A[1:0] : | Description |
|---|---|
| 00 | Normal Mode [POR] |
| 01 | Enter Deep Sleep Mode 1 |
| 11 | Enter Deep Sleep Mode 2 |

After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.
Remark:
To Exit Deep Sleep mode, User required to send HWRESET to the driver

**Command Table**

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 11 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Data Entry mode setting | Define data entry sequence<br>A[2:0] = 011 [POR]<br><br>A [1:0] = ID[1:0]<br>Address automatic increment / decrement setting<br>The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.<br>00 –Y decrement, X decrement,<br>01 –Y decrement, X increment,<br>10 –Y increment, X decrement,<br>11 –Y increment, X increment [POR]<br><br>A[2] = AM<br>Set the direction in which the address counter is updated automatically after data are written to the RAM.<br>AM= 0, the address counter is updated in the X direction. [POR]<br>AM = 1, the address counter is updated in the Y direction. |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | $A_2$ | $A_1$ | $A_0$ | | |
| | | | | | | | | | | | | |
| 0 | 0 | 12 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | SW RESET | It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode<br><br>During operation, BUSY pad will output high.<br><br>Note: RAM are unaffected by this command. |
| 0 | 0 | 14 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | HV Ready Detection | HV ready detection<br>A[7:0] = 00h [POR]<br>The command required CLKEN=1 and ANALOGEN=1.<br>Refer to Register 0x22 for detail.<br>After this command initiated, HV Ready detection starts.<br>BUSY pad will output high during detection.<br>The detection result can be read from the Status Bit Read (Command 0x2F). |
| 0 | 1 | | 0 | $A_6$ | $A_5$ | $A_4$ | 0 | $A_2$ | $A_1$ | $A_0$ | | A[6:4]=n for cool down duration:<br>10ms x (n+1)<br>A[2:0]=m for number of Cool Down Loop to detect.<br>The max HV ready duration is<br>10ms x (n+1) x (m)<br>HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready.<br>For 1 shot HV ready detection, A[7:0] can be set as 00h. |

**Command Table**

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 15 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | VCI Detection | VCI Detection<br>A[2:0] = 100 [POR] , Detect level at 2.3V<br>A[2:0] : VCI level Detect<br>A[2:0] VCI level<br>011 2.2V<br>100 2.3V<br>101 2.4V<br>110 2.5V<br>111 2.6V<br>Other NA<br>The command required CLKEN=1 and ANALOGEN=1<br>Refer to Register 0x22 for detail.<br>After this command initiated, VCI detection starts.<br>BUSY pad will output high during detection.<br>The detection result can be read from the Status Bit Read (Command 0x2F). |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 0 | 18 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | Temperature Sensor Control | Temperature Sensor Selection<br>A[7:0] = 48h [POR], external temperatrure sensor<br>A[7:0] = 80h Internal temperature sensor |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 0 | 1A | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | Temperature Sensor Control (Write to temperature register) | Write to temperature register.<br>A[7:0] = 7Fh [POR] |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 0 | 1B | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | Temperature Sensor Control (Read from temperature register) | Read from temperature register. |
| 1 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 0 | 1C | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | Temperature Sensor Control (Write Command to External temperature sensor) | Write Command to External temperature sensor.<br>A[7:0] = 00h [POR],<br>B[7:0] = 00h [POR],<br>C[7:0] = 00h [POR],<br>A[7:6]<br>A[7:6] Select no of byte to be sent<br>00 Address + pointer<br>01 Address + pointer + 1st parameter<br>10 Address + pointer + 1st parameter + 2nd pointer<br>11 Address<br>A[5:0] – Pointer Setting<br>B[7:0] – 1st parameter<br>C[7:0] – 2nd parameter<br>The command required CLKEN=1.<br>Refer to Register 0x22 for detail.<br>After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation. |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 1 | | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 0 | 1 | | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | | |
| 0 | 0 | 1F | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | IC revision Read | Read IC revision [POR 0x0D] |
| 1 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |

**Command Table**

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 20 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Master Activation | Activate Display Update Sequence<br><br>The Display Update Sequence Option is located at R22h.<br><br>BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images. |
| | | | | | | | | | | | | |
| 0 | 0 | 21 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Display Update Control 1 | RAM content option for Display Update<br>A[7:0] = 00h [POR]<br>B[7:0] = 00h [POR]<br><br>A[7:4] Red RAM option<br>0000 Normal<br>0100 Bypass RAM content as 0<br>1000 Inverse RAM content<br><br>A[3:0] BW RAM option<br>0000 Normal<br>0100 Bypass RAM content as 0<br>1000 Inverse RAM content<br><br>B[7] Source Output Mode<br>0 Available Source from S0 to S175<br>1 Available Source from S8 to S167 |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 1 | | $B_7$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 0 | 0 | 24 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | Write RAM (Black White) / RAM 0x24 | After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly<br><br>For Write pixel:<br>Content of Write RAM(BW) = 1<br>For Black pixel:<br>Content of Write RAM(BW) = 0 |

**Command Table**

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 22 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | Display Update Control 2 | Display Update Sequence Option:<br>Enable the stage for Master Activation<br>A[7:0]= FFh (POR) |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |

| Operating sequence | Parameter (in Hex) |
|---|---|
| Enable clock signal | 80 |
| Disable clock signal | 01 |
| | |
| Enable clock signal<br>→ Enable Analog | C0 |
| Disable Analog<br>→ Disable clock signal | 03 |
| | |
| Enable clock signal<br>→ Load LUT with DISPLAY Mode 1<br>→ Disable clock signal | 91 |
| Enable clock signal<br>→ Load LUT with DISPLAY Mode 2<br>→ Disable clock signal | 99 |
| | |
| Enable clock signal<br>→ Load temperature value<br>→ Load LUT with DISPLAY Mode 1<br>→ Disable clock signal | B1 |
| Enable clock signal<br>→ Load temperature value<br>→ Load LUT with DISPLAY Mode 2<br>→ Disable clock signal | B9 |
| | |
| Enable clock signal<br>→ Enable Analog<br>→ Display with DISPLAY Mode 1<br>→ Disable Analog<br>→ Disable OSC | C7 |
| Enable clock signal<br>→ Enable Analog<br>→ Display with DISPLAY Mode 2<br>→ Disable Analog<br>→Disable OSC | CF |
| | |
| Enable clock signal<br>→Enable Analog<br>→ Load temperature value<br>→ DISPLAY with DISPLAY Mode 1<br>→ Disable Analog<br>→ Disable OSC | F7 |
| Enable clock signal<br>→Enable Analog<br>→ Load temperature value<br>→ DISPLAY with DISPLAY Mode 2<br>→ Disable Analog<br>→ Disable OSC | FF |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 26 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | Write RAM (RED) / RAM 0x26 | After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly.<br><br>For Red pixel:<br>Content of Write RAM(RED) = 1<br>For non-Red pixel [Black or White]:<br>Content of Write RAM(RED) = 0 |
| | | | | | | | | | | | | |
| 0 | 0 | 27 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | Read RAM | After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly.<br><br>The 1st byte of data read is dummy data. |

**Command Table**

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 28 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | VCOM Sense | Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value.<br>The sensed VCOM voltage is stored in register<br>The command required CLKEN=1 and ANALOGEN=1<br>Refer to Register 0x22 for detail.<br><br>BUSY pad will output high during operation. |
| | | | | | | | | | | | | |
| 0 | 0 | 29 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | VCOM Sense Duration | Stabling time between entering VCOM sensing mode and reading acquired.<br><br>A[3:0] = 9h, duration = 10s.<br>VCOM sense duration = (A[3:0]+1) sec |
| 0 | 1 | | 0 | 1 | 0 | 0 | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| | | | | | | | | | | | | |
| 0 | 0 | 2A | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Program VCOM OTP | Program VCOM register into OTP<br><br>The command required CLKEN=1.<br>Refer to Register 0x22 for detail.<br><br>BUSY pad will output high during operation. |
| 0 | 0 | 2C | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Write VCOM register | Write VCOM register from MCU interface<br>A[7:0] = 00h [POR] |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |

| A[7:0] | VCOM | A[7:0] | VCOM |
|---|---|---|---|
| 08h | -0.2 | 44h | -1.7 |
| 0Ch | -0.3 | 48h | -1.8 |
| 10h | -0.4 | 4Ch | -1.9 |
| 14h | -0.5 | 50h | -2 |
| 18h | -0.6 | 54h | -2.1 |
| 1Ch | -0.7 | 58h | -2.2 |
| 20h | -0.8 | 5Ch | -2.3 |
| 24h | -0.9 | 60h | -2.4 |
| 28h | -1 | 64h | -2.5 |
| 2Ch | -1.1 | 68h | -2.6 |
| 30h | -1.2 | 6Ch | -2.7 |
| 34h | -1.3 | 70h | -2.8 |
| 38h | -1.4 | 74h | -2.9 |
| 3Ch | -1.5 | 78h | -3 |
| 40h | -1.6 | Other | NA |

| Command Table | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
| 0 | 0 | 2D | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | OTP Register Read for Display Option | Read Register for Display Option:<br><br>A[7:0]: VCOM OTP Selection (Command 0x37, Byte A)<br><br>B[7:0]: VCOM Register (Command 0x2C)<br><br>C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes]<br><br>H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes] |
| 1 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 1 | 1 | | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 1 | 1 | | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | | |
| 1 | 1 | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | | |
| 1 | 1 | | $E_7$ | $E_6$ | $E_5$ | $E_4$ | $E_3$ | $E_2$ | $E_1$ | $E_0$ | | |
| 1 | 1 | | $F_7$ | $F_6$ | $F_5$ | $F_4$ | $F_3$ | $F_2$ | $F_1$ | $F_0$ | | |
| 1 | 1 | | $G_7$ | $G_6$ | $G_5$ | $G_4$ | $G_3$ | $G_2$ | $G_1$ | $G_0$ | | |
| 1 | 1 | | $H_7$ | $H_6$ | $H_5$ | $H_4$ | $H_3$ | $H_2$ | $H_1$ | $H_0$ | | |
| 1 | 1 | | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | | |
| 1 | 1 | | $J_7$ | $J_6$ | $J_5$ | $J_4$ | $J_3$ | $J_2$ | $J_1$ | $J_0$ | | |
| 1 | 1 | | $K_7$ | $K_6$ | $K_5$ | $K_4$ | $K_3$ | $K_2$ | $K_1$ | $K_0$ | | |
| | | | | | | | | | | | | |
| 0 | 0 | 2E | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | User ID Read | Read 10 Byte User ID stored in OTP: A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes] |
| 1 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 1 | 1 | | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 1 | 1 | | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | | |
| 1 | 1 | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | | |
| 1 | 1 | | $E_7$ | $E_6$ | $E_5$ | $E_4$ | $E_3$ | $E_2$ | $E_1$ | $E_0$ | | |
| 1 | 1 | | $F_7$ | $F_6$ | $F_5$ | $F_4$ | $F_3$ | $F_2$ | $F_1$ | $F_0$ | | |
| 1 | 1 | | $G_7$ | $G_6$ | $G_5$ | $G_4$ | $G_3$ | $G_2$ | $G_1$ | $G_0$ | | |
| 1 | 1 | | $H_7$ | $H_6$ | $H_5$ | $H_4$ | $H_3$ | $H_2$ | $H_1$ | $H_0$ | | |
| 1 | 1 | | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | | |
| 1 | 1 | | $J_7$ | $J_6$ | $J_5$ | $J_4$ | $J_3$ | $J_2$ | $J_1$ | $J_0$ | | |
| 0 | 0 | 2F | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | Status Bit Read | Read IC status Bit [POR 0x01]<br>A[5]: HV Ready Detection flag [POR=0]<br>0: Ready<br>1: Not Ready<br>A[4]: VCI Detection flag [POR=0]<br>0: Normal<br>1: VCI lower than the Detect level<br>A[3]: [POR=0]<br>A[2]: Busy flag [POR=0]<br>0: Normal<br>1: BUSY<br>A[1:0]: Chip ID [POR=01]<br><br>Remark:<br>A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively. |
| 1 | 1 | | 0 | 0 | $A_5$ | $A_4$ | 0 | 0 | $A_1$ | $A_0$ | | |
| | | | | | | | | | | | | |
| 0 | 0 | 30 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Program WS OTP | Program OTP of Waveform Setting<br>The contents should be written into RAM before sending this command.<br><br>The command required CLKEN=1.<br>Refer to Register 0x22 for detail.<br>BUSY pad will output high during operation. |

| Command Table | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
| 0 | 0 | 31 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | Load WS OTP | Load OTP of Waveform Setting<br><br>The command required CLKEN=1.<br>Refer to Register 0x22 for detail.<br><br>BUSY pad will output high during operation. |
| | | | | | | | | | | | | |
| 0 | 0 | 32 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | Write LUT register | Write LUT register from MCU interface [227 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR and XON[nXY]<br>Refer to Session 6.7 WAVEFORM SETTING |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 1 | | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 0 | 1 | | : | : | : | : | : | : | : | : | | |
| 0 | 1 | | . | .. | . | . | . | . | . | . | | |
| | | | | | | | | | | | | |
| 0 | 0 | 34 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | CRC calculation | CRC calculation command<br>For details, please refer to SSD1680A application note.<br><br>BUSY pad will output high during operation. |
| | | | | | | | | | | | | |
| 0 | 0 | 35 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | CRC Status Read | CRC Status Read<br>A[15:0] is the CRC read out value |
| 1 | 1 | | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ | | |
| 1 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 0 | 36 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Program OTP selection | Program OTP Selection according to the OTP Selection Control [R37h and R38h]<br><br>The command required CLKEN=1.<br>Refer to Register 0x22 for detail.<br>BUSY pad will output high during operation. |
| | | | | | | | | | | | | |
| 0 | 0 | 37 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Write Register for Display Option | Write Register for Display Option<br>A[7] Spare VCOM OTP selection<br>0: Default [POR]<br>1: Spare<br><br>B[7:0] Display Mode for WS[7:0]<br>C[7:0] Display Mode for WS[15:8]<br>D[7:0] Display Mode for WS[23:16]<br>0: Display Mode 1<br>1: Display Mode 2<br><br>F[6]: Ping-Pong for Display Mode 2<br>0: RAM Ping-Pong disable [POR]<br>1: RAM Ping-Pong enable<br><br>G[7:0]~J[7:0] module ID /waveform version.<br><br>Remarks:<br>1) A[7:0]~J[7:0] can be stored in OTP<br>2) RAM Ping-Pong function is not support for Display Mode 1 |
| 0 | 1 | | $A_7$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 0 | 1 | | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 0 | 1 | | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | | |
| 0 | 1 | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | | |
| 0 | 1 | | $E_7$ | $E_6$ | $E_5$ | $E_4$ | $E_3$ | $E_2$ | $E_1$ | $E_0$ | | |
| 0 | 1 | | 0 | $F_6$ | 0 | 0 | $F_3$ | $F_2$ | $F_1$ | $F_0$ | | |
| 0 | 1 | | $G_7$ | $G_6$ | $G_5$ | $G_4$ | $G_3$ | $G_2$ | $G_1$ | $G_0$ | | |
| 0 | 1 | | $H_7$ | $H_6$ | $H_5$ | $H_4$ | $H_3$ | $H_2$ | $H_1$ | $H_0$ | | |
| 0 | 1 | | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | | |
| 0 | 1 | | $J_7$ | $J_6$ | $J_5$ | $J_4$ | $J_3$ | $J_2$ | $J_1$ | $J_0$ | | |

**Command Table**

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 38 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | Write Register for User ID | Write Register for User ID<br>A[7:0]]~J[7:0]: UserID [10 bytes]<br><br>Remarks: A[7:0]~J[7:0] can be stored in OTP |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 1 | | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 0 | 1 | | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | | |
| 0 | 1 | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | | |
| 0 | 1 | | $E_7$ | $E_6$ | $E_5$ | $E_4$ | $E_3$ | $E_2$ | $E_1$ | $E_0$ | | |
| 0 | 1 | | $F_7$ | $F_6$ | $F_5$ | $F_4$ | $F_3$ | $F_2$ | $F_1$ | $F_0$ | | |
| 0 | 1 | | $G_7$ | $G_6$ | $G_5$ | $G_4$ | $G_3$ | $G_2$ | $G_1$ | $G_0$ | | |
| 0 | 1 | | $H_7$ | $H_6$ | $H_5$ | $H_4$ | $H_3$ | $H_2$ | $H_1$ | $H_0$ | | |
| 0 | 1 | | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | | |
| 0 | 1 | | $J_7$ | $J_6$ | $J_5$ | $J_4$ | $J_3$ | $J_2$ | $J_1$ | $J_0$ | | |
| 0 | 0 | 39 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | OTP program mode | OTP program mode<br>A[1:0] = 00: Normal Mode [POR]<br>A[1:0] = 11: Internal generated OTP programming voltage<br><br>: User is required to EXACTLY follow the reference code sequences |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | $A_1$ | $A_0$ | | |
| 0 | 0 | 3C | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | Border Waveform Control | Select border waveform for VBD<br>A[7:0] = C0h [POR], set VBD as HIZ.<br>A [7:6] :Select VBD option |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | 0 | 0 | $A_1$ | $A_0$ | | |

| A[7:6] | Select VBD as |
|---|---|
| 00 | GS Transition, Defined in A[2] and A[1:0] |
| 01 | Fix Level, Defined in A[5:4] |
| 10 | VCOM |
| 11[POR] | HiZ |

A [5:4] Fix Level Setting for VBD

| A[5:4] | VBD level |
|---|---|
| 00 | VSS |
| 01 | VSH1 |
| 10 | VSL |
| 11 | VSH2 |

A [1:0] GS Transition setting for VBD
VBD Level Selection:
00b: VCOM ; 01b: VSH1;
10b: VSL; 11b: VSH2

| A[1:0] | VBD Transition |
|---|---|
| 00 | LUT0 |
| 01 | LUT1 |
| 10 | LUT2 |
| 11 | LUT3 |

| 0 | 0 | 3F | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | End Option (EOPT) | Option for LUT end<br>Data bytes should be set for this command or programmed into Waveform setting. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |

| | |
|---|---|
| 22h | Normal. |
| 07h | Source output level keep previous output before power off |

| Command Table | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
| 0 | 0 | 41 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | Read RAM Option | Read RAM Option<br>A[0]= 0 [POR]<br>0 : Read RAM corresponding to RAM0x24<br>1 : Read RAM corresponding to RAM0x26 |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $A_0$ | | |
| | | | | | | | | | | | | |
| 0 | 0 | 44 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Set RAM X - address Start / End position | Specify the start/end positions of the window address in the X direction by an address unit for RAM<br><br>A[5:0]: XSA[5:0], XStart, POR = 00h<br>B[5:0]: XEA[5:0], XEnd, POR = 15h |
| 0 | 1 | | 0 | 0 | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 1 | | 0 | 0 | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| | | | | | | | | | | | | |
| 0 | 0 | 45 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Set Ram Y- address Start / End position | Specify the start/end positions of the window address in the Y direction by an address unit for RAM<br><br>A[8:0]: YSA[8:0], YStart, POR = 000h<br>B[8:0]: YEA[8:0], YEnd, POR = 127h |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $A_8$ | | |
| 0 | 1 | | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $B_8$ | | |
| | | | | | | | | | | | | |
| 0 | 0 | 46 | 0 | 1 | 0 | 0 | 0 | 1 | | 0 | Auto Write RED RAM for Regular Pattern | Auto Write RED RAM for Regular Pattern<br>A[7:0] = 00h [POR]<br><br>A[7]: The 1st step value, POR = 0<br>A[6:4]: Step Height, POR= 000<br>Step of alter RAM in Y-direction according to Gate<br>A[6:4] Height A[6:4] Height<br>000 8 100 128<br>001 16 101 256<br>010 32 110 296<br>011 64 111 NA<br><br>A[2:0]: Step Width, POR= 000<br>Step of alter RAM in X-direction according to Source<br>A[2:0] Width A[2:0] Width<br>000 8 100 128<br>001 16 101 176<br>010 32 110 NA<br>011 64 111 NA<br><br>BUSY pad will output high during operation. |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | 0 | $A_2$ | $A_1$ | $A_0$ | | |

**Command Table**

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 47 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | Auto Write B/W RAM for Regular Pattern | Auto Write B/W RAM for Regular Pattern<br>A[7:0] = 00h [POR]<br><br>A[7]: The 1st step value, POR = 0<br>A[6:4]: Step Height, POR= 000<br>Step of alter RAM in Y-direction according to Gate<br>A[6:4] Height A[6:4] Height<br>000 8 100 128<br>001 16 101 256<br>010 32 110 296<br>011 64 111 NA<br><br>A[2:0]: Step Width, POR= 000<br>Step of alter RAM in X-direction according to Source<br>A[2:0] Width A[2:0] Width<br>000 8 100 128<br>001 16 101 176<br>010 32 110 NA<br>011 64 111 NA<br><br>During operation, BUSY pad will output high. |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | 0 | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 0 | 4E | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | Set RAM X address counter | Make initial settings for the RAM X address in the address counter (AC)<br>A[5:0]: 00h [POR]. |
| 0 | 1 | | 0 | 0 | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 0 | 4F | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | Set RAM Y address counter | Make initial settings for the RAM Y address in the address counter (AC)<br>A[8:0]: 000h [POR]. |
| 0 | 1 | | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $A_8$ | | |
| 0 | 0 | 7F | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | NOP | This command is an empty command; it does not have any effect on the display module.<br>However it can be used to terminate Frame Memory Write or Read Commands. |

## 8.Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ. | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| R | White Reflectivity | White | 30 | 35 | - | % | 8-1 |
| CR | Contrast Ratio | Indoor | 8:1 | | - | | 8-2 |
| GN | 2Grey Level | - | | DS+(WS-DS)*n(m-1) | | | 8-3 |
| T update | Image update time | at 25 °C | | 3 | - | sec | |
| Life | | Topr | | 1000000times or 5years | | | |

**Notes:**

8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3 WS: White state, DS: Dark state

## 9. Handling, Safety and Environment Requirements

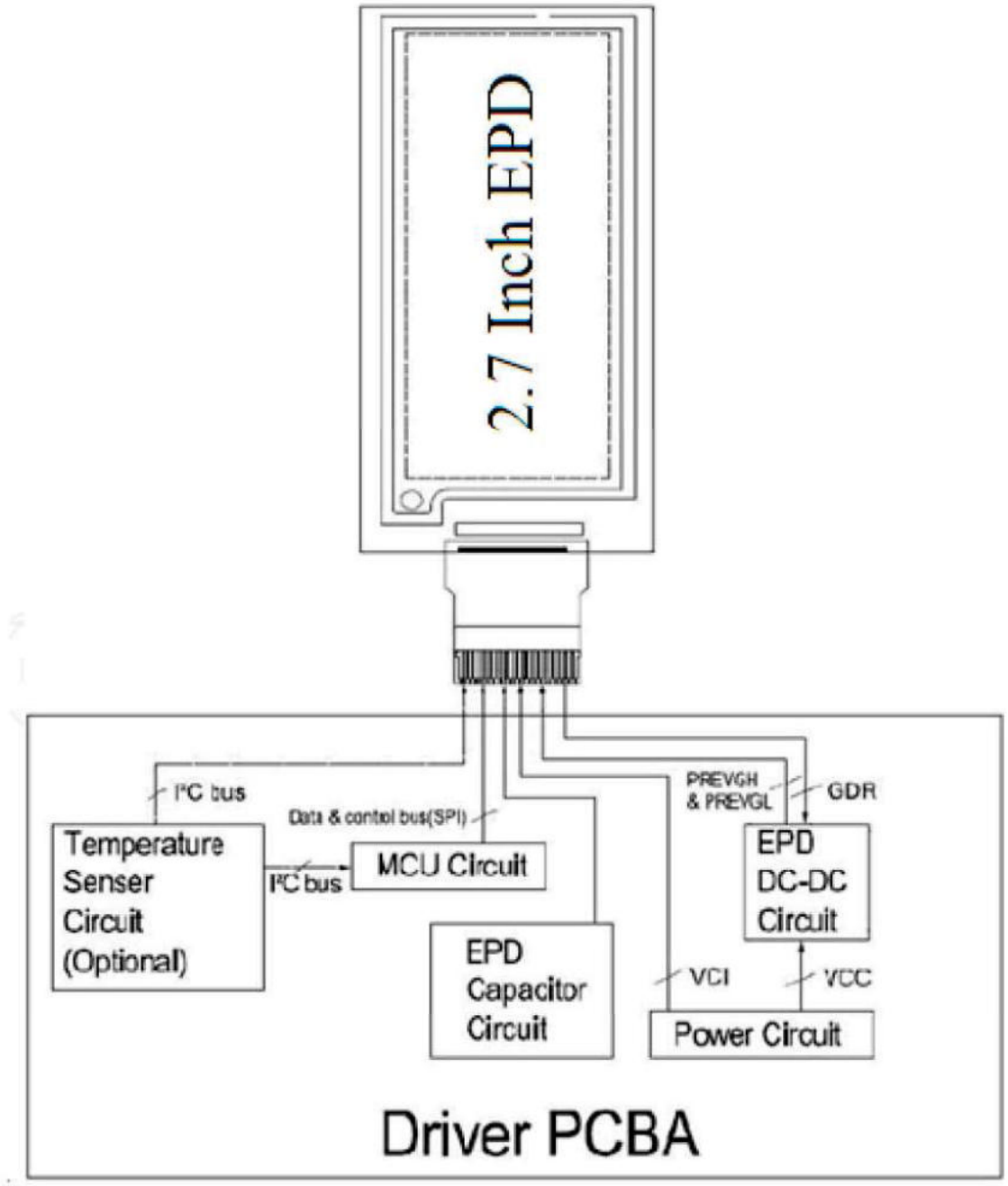
| Warning |
|---|
| The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap. |
| **Caution** |
| The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.<br>Disassembling the display module can cause permanent damage and invalidates the warranty agreements.<br>Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions. |
| **Data sheet status** |
| Product specification — This data sheet contains final product specifications. |
| **Limiting values** |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |
| **Application information** |
| Where application information is given, it is advisory and does not form part of the specification. |

## 10.Reliability test

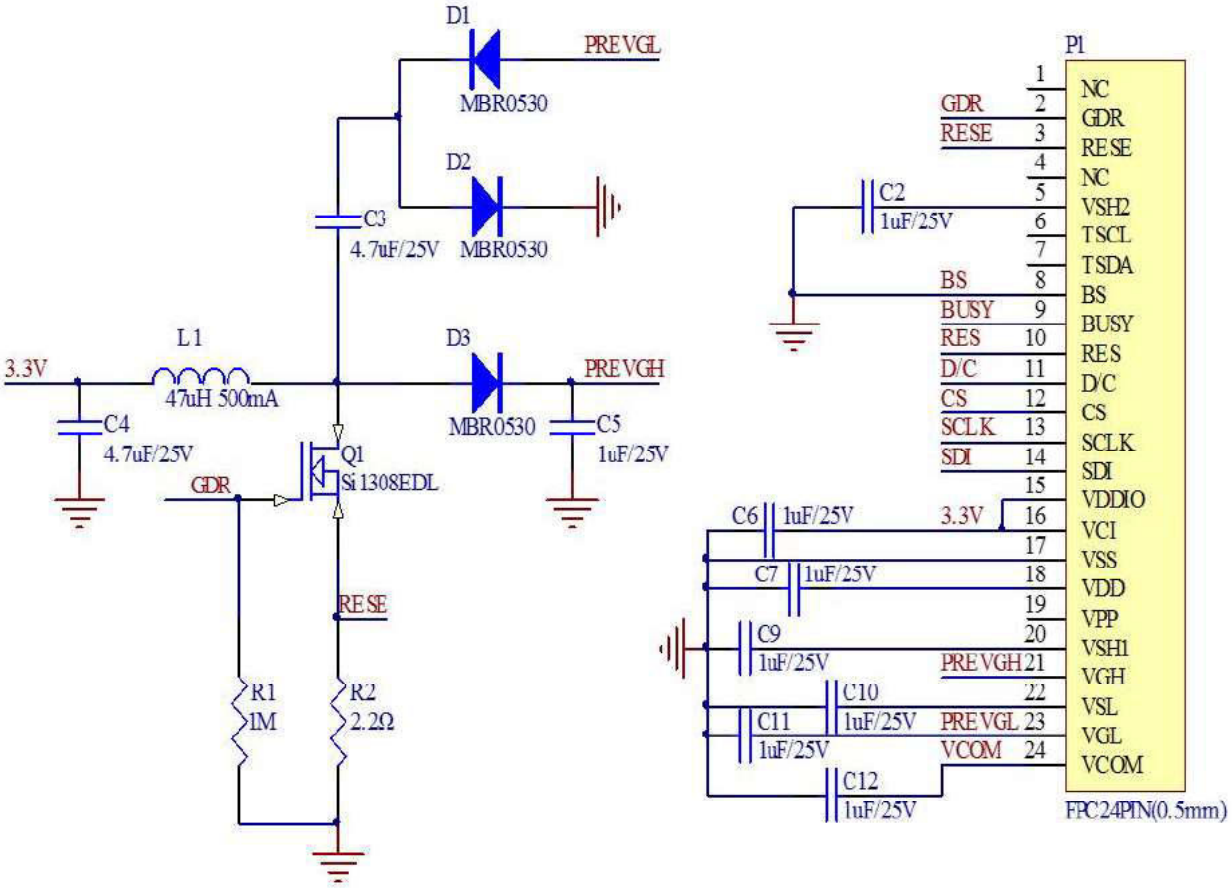
| NO | Test items | Test condition |
|---|---|---|
| 1 | Low-Temperature Storage | T = -25°C, 240 h<br>Test in white pattern |
| 2 | High-Temperature Storage | T=70° C，RH=40%，240h<br>Test in white pattern |
| 3 | High-Temperature Operation | T=50° C，RH=35%，240h |
| 4 | Low-Temperature Operation | 0° C，240h |
| 5 | High-Temperature, High-Humidity Operation | T=40° C，RH=80%，240h |
| 6 | High Temperature, High Humidity Storage | T=50° C，RH=80%, 240h<br>Test in white pattern |
| 7 | Temperature Cycle | 1 cycle:[-25° C 30min]→[+70 ° C 30 min] : 50 cycles<br>Test in white pattern |
| 8 | UV exposure Resistance | 765W/m² for 168hrs,40 °C<br>Test in white pattern |
| 9 | ESD Gun | Air+/-15KV;Contact+/-8KV<br>(Test finished product shell, not display only)<br>Air+/-8KV;Contact+/-6KV<br>(Naked EPD display, no including IC and FPC area)<br>Air+/-4KV;Contact+/-2KV<br>(Naked EPD display, including IC and FPC area) |

**Note:**
Put in normal temperature for 1hour after test finished, display performance is ok.

## 11. Block Diagram



## 12. Reference Circuit



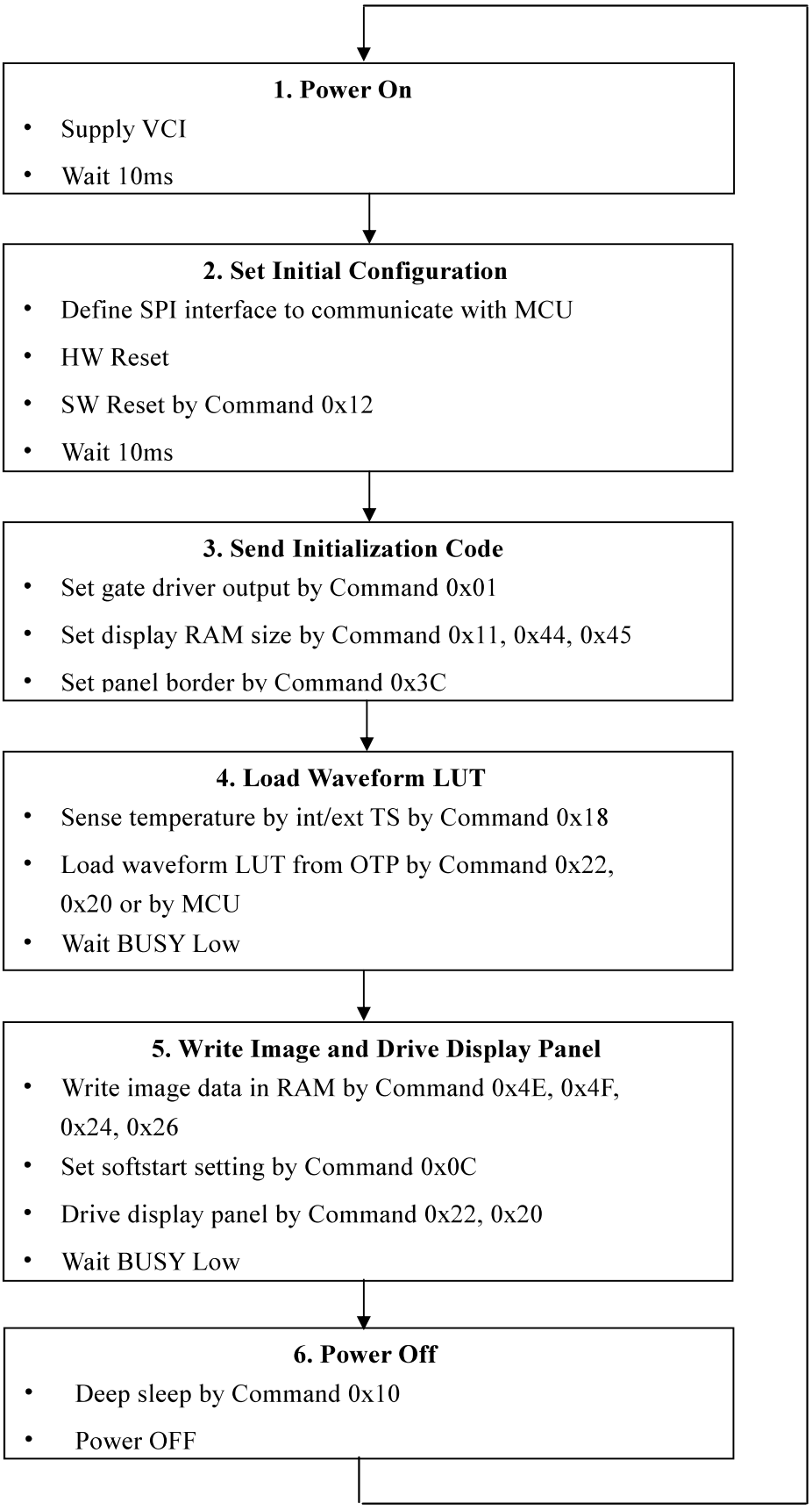

| Part Name | Requirements for spare part |
|---|---|
| C1—C12 | 0603/0805; X5R/X7R;Voltage Rating:≥25V |
| R1、R2 | 0603/0805;1% variation,≥0.05W |
| D1—D3 | MBR0530: 1)Reverse DC Voltage≥30V 2)Io≥500mA 3)Forward voltage ≤430mV |
| Q1 | Si1308EDL:1)Drain-Source breakdown voltage≥30V 2)Vgs(th)≤1.5V 3)Rds(on)≤400mΩ |
| L1 | refer to NR3015: Io=500mA(max) |
| P1 | 24pins,0.5mm pitch |

## 13. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) WINSTAR Display 's E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.
DESPI Development Kit consists of the development board and the pinboard.

# 14.Typical Operating Sequence

## 14.1 Normal Operation Flow



# 15.Inspection condition

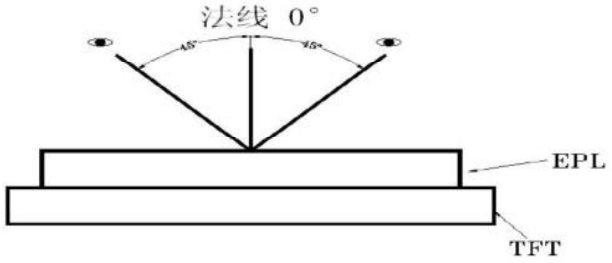
## 15.1 Environment

Temperature： 25±3℃
Humidity： 55±10%RH

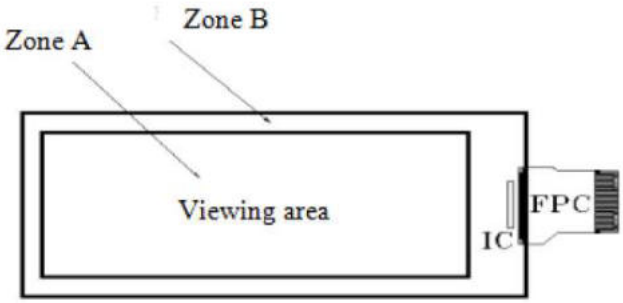
## 15.2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 30°surround.

## 15.3 Inspection method

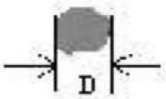
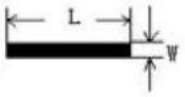



## 15.4 Display area

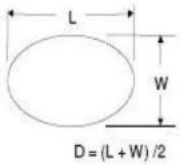
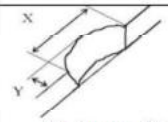
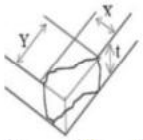
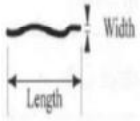


## 15.5 Inspection standard

### 15.5.1 Electric inspection standard

| NO. | Item | Standard | Defect level | Method | Scope |
|---|---|---|---|---|---|
| 1 | Display | Display complete<br>Display uniform | MA | Visual inspection | Zone A |
| 2 | Black/White spots |  <br>D≤0.25mm，Allowed<br>0.25mm＜D≤0.4mm。N≤3，and Distance≥5mm<br>0.4mm＜D Not Allow | MI | | |
| 3 | Black/White spots<br>(No switch) |  <br>L≤0.6mm，W≤0.2mm，N≤1<br>L≤2.0mm,W＞0.2mm，Not Allow<br>L＞0.6mm，Not Allow | | Visual/ Inspection card | |
| 4 | Ghost image | Allowed in switching process | MI | Visual inspection | |
| 5 | Flash spots/ Larger FPL size | Flash spots in switching, Allowed<br>FPL size larger than viewing area, Allowed | MI | Visual/ Inspection card | Zone A<br>Zone B |
| 6 | Display wrong/Missing | All appointed displays are showed correct | MA | Visual inspection | Zone A |
| 7 | Short circuit/ Circuit break/ Display abnormal | Not Allow | | | |

## 15.5.2 Appearance inspection standard

| NO. | Item | Standard | Defect level | Method | Scope |
|---|---|---|---|---|---|
| 1 | B/W spots /Bubble/ Foreign bodies/ Dents |  D≤0.25mm，Allowed<br>0.25mm＜D≤0.4mm，N≤3<br>D＞0.4mm，Not Allow | MI | Visual inspection | Zone A |
| 2 | Glass crack | Not Allow | MA | Visual / Microscope | Zone A<br>Zone B |
| 3 | Dirty | Allowed if can be removed | MI | | Zone A<br>Zone B |
| 4 | Chips/Scratch/ Edge crown |  X≤3mm,Y≤0.5mmAnd without affecting the electrode is permissible<br>  2mm≤X or 2mm≤Y Not Allow<br>  W≤0.1mm,L≤5mm, No harm to the electrodes and N≤2 allow | MI | Visual / Microscope | Zone A<br>Zone B |
| 5 | TFT Cracks |  Not Allow | MA | Visual / Microscope | Zone A<br>Zone B |
| 6 | Dirty/ foreign body | Allowed if can be removed/ allow | MI | Visual / Microscope | Zone A / Zone B |
| 7 | FPC broken/ Goldfingers ›xidation/ scratch |   Not Allow | MA | Visual / Microscope | Zone B |

| | | | | | |
|---|---|---|---|---|---|
| 8 | TFT edge bulge /TFT chromatic aberration | TFT edge bulge:<br>X≤3mm，Y≤0.3mm Allowed<br>TFT chromatic aberration :Allowed | MI | Visual / Microscope | Zone A<br>Zone B |
| 9 | PCB damaged/ Poor welding/ Curl | PCB（Circuit area）damaged Not Allow<br>PCB Poor welding Not Allow<br>PCB Curl≤1% | MI | Visual / Ruler | Zone B |
| 10 | Edge glue height/ Edge glue bubble | Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding<br>Edge adhesives bubble: bubble Width<br>≤1/2 Margin width; Length<br>≤0.5mm。n≤5 | | | |
| 11 | Protect film | Surface scratch but not effect protect function, Allowed | | Visual Inspection | |
| 12 | Silicon glue | Thickness≤PS surface(With protect film):<br>Full cover the IC;<br>Shape:<br>The width on the FPC ≤ 0.5mm (Front)<br>The width on the FPC≤1.0mm (Back)<br>smooth surface,No obvious raised. | MI | Visual Inspection | |
| 13 | Warp degree (TFT substrate) | t≤2.0mm | MI | Ruler | |
| 14 | Color difference in COM area (Silver point area) | Allowed | | Visual Inspection | |

## 16. Packing

TBD

## 17. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.