WINSTAR Display

OLED SPECIFICATION

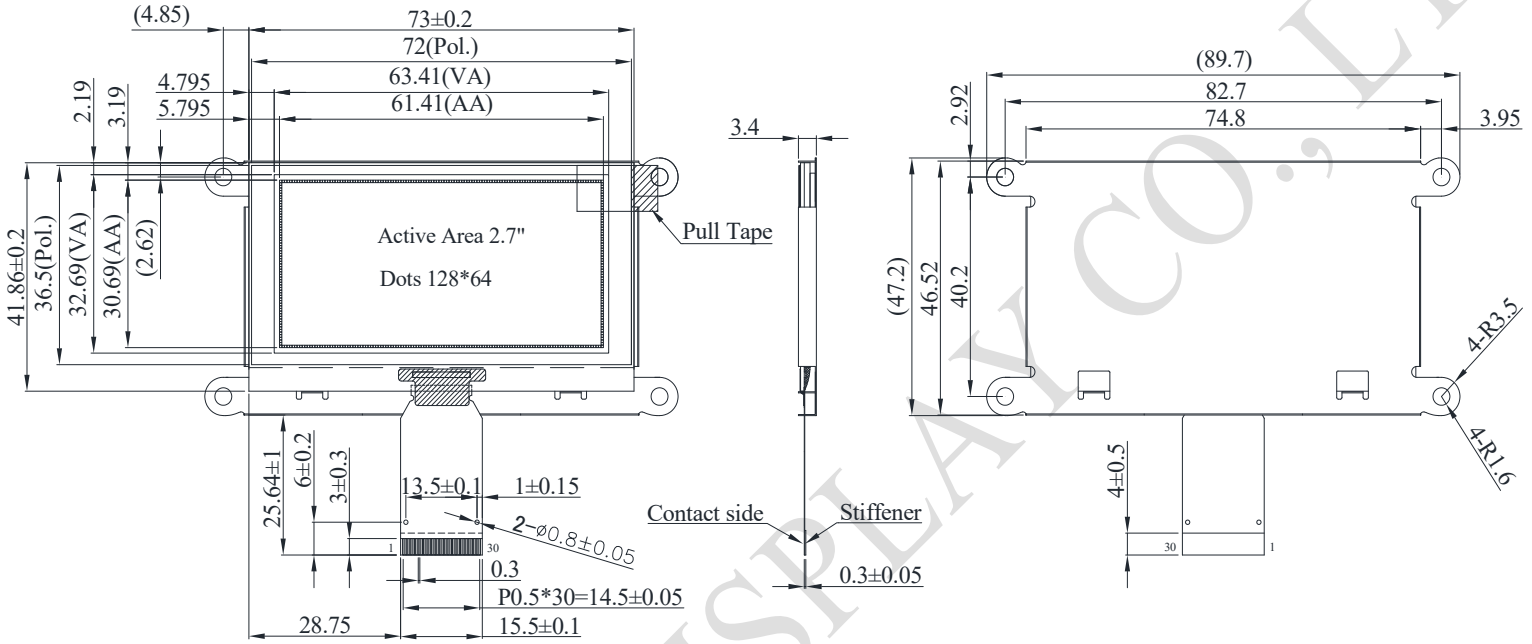
Model No:

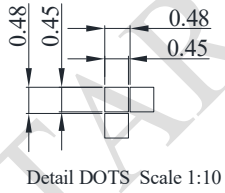
WEF012864U

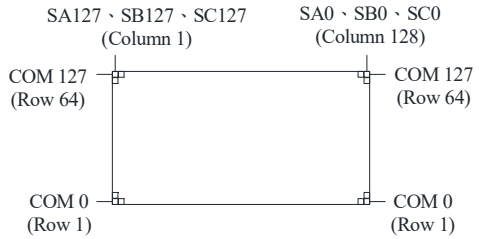
General Specification

Item	Dimension	Unit
Dot Matrix	128 x 64 Dots	—
Module dimension	89.7 x 47.2 x 3.4	mm
Active Area	61.41 × 30.69	mm
Pixel Size	0.45 × 0.45	mm
Pixel Pitch	0.48 × 0.48	mm
Display Mode	Passive Matrix	
Display Color	Monochrome	
Drive Duty	1/64 Duty	
Gray Scale	4 bits	
IC	SSD1357	
Interface	8-bits 6800 and 8080 parallel, 4-line SPI, I2C	
Size	2.7 inch	

Contour Drawing & Block Diagram







PIN No.	SYMBOL
1	NC(GND)
2	VSS
3	VCC
4	VCOMH
5	VLSS
6	D7
7	D6
8	D5
9	D4
10	D3
11	D2
12	D1
13	D0
14	E/RD#
15	R/W#
16	BS1
17	BS2
18	DC#
19	CS#
20	RES#
21	FR
22	IREF
23	NC
24	VDD
25	VP
26	VDD
27	VSL
28	VLSS
29	VCC
30	NC(GND)

The non-specified tolerance of dimension is ±0.3 mm .

Interface Pin Function

No.	Symbol	Function
1	NC(GND)	No connection.
2	VSS	Ground of Logic Circuit. This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
3	VCC	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
4	VCOMH	Voltage Output High Level for COM Signal. This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
5	VLSS	Ground of Analog Circuit These are the analog ground pins. They should be connected to VSS externally.
6~13	D7~D0	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
14	E/RD#	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.
15	R/W#	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.

<table>
<tr><td>16
17</td><td>BS1
BS2</td><td>Communicating Protocol Select.
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS1</td><td>BS2</td></tr>
<tr><td>I2C</td><td>1</td><td>0</td></tr>
<tr><td>4-wire Serial</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 8080 Parallel</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 6800 Parallel</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>18</td><td>D/C#</td><td>This pin is Data/Command control pin connecting to the MCU.
When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.
When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.
In I2C mode, this pin acts as SA0 for slave address selection.
When 3-wire serial interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>19</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only
when CS# is pulled low.</td></tr>
<tr><td>20</td><td>RES#</td><td>This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>21</td><td>FR</td><td>Frame Frequency Triggering Signal
This pin will send out a signal that could be used to identify the driver status.
Nothing should be connected to this pin. It should be left open individually.</td></tr>
<tr><td>22</td><td>IREF</td><td>This pin is the segment output current reference pin.
IREF is supplied externally.</td></tr>
<tr><td>23</td><td>N.C.</td><td>Reserved Pin
The N.C. pin between function pins is reserved for compatible and flexible design.</td></tr>
<tr><td>24</td><td>VDD</td><td>Power Supply for I/O Pin.
This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.</td></tr>
<tr><td>25</td><td>VP</td><td>Power Supply for Core Logic Circuit
This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.</td></tr>
<tr><td>26</td><td>VDD</td><td>Power Supply for Operation.
This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.</td></tr>
<tr><td>27</td><td>VSL</td><td>Voltage Output Low Level for SEG Signal
This is segment voltage (output low level) reference pin.
This pin has to connect with resistor and diode to ground (details depends on application).</td></tr>
</table>

28	VLSS	Ground of Analog Circuit These are the analog ground pins. They should be connected to VSS externally.
29	VCC	Power Supply for OEL Panel These are the most positive voltage supply pin of the chip. They must be connected to external source.
30	NC(GND)	No connection

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	VDD	-0.3	4.0	V	1, 2
Supply Voltage for Display	VCC	0	15.0	V	1, 2
Operating Temperature	TOP	-40	+80	°C	-
Storage Temperature	TSTG	-40	+85	°C	-

Electrical Characteristics

DC Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD	—	1.65	3.0	3.3	V
Supply Voltage for Display	VCC	—	8.0	9.0	9.5	V
High Level Input	VIH	—	0.8×VDD	—	VDD	V
Low Level Input	VIL	—	—	—	0.2×VDD	V
High Level Output	VOH	—	0.9×VDD	—	VDD	V
Low Level Output	VOL	—	—	—	0.1×VDD	V
Display 50% Pixel on	ICC	VCC =9V	—	31.5	47.5	mA