

MOSFET

CoolSiC™ Automotive Power Device 750 V G1

The 750 V CoolSiC™ is built over the solid silicon carbide technology developed in Infineon in more than 20 years. Leveraging the wide bandgap SiC material characteristics, the 750V CoolSiC™ MOSFET offers a unique combination of performance, reliability and ease of use. Suitable for high temperature and harsh operations, it enables the simplified and cost effective deployment of the highest system efficiency.

Features

- Highly robust 750V technology, 100% avalanche tested
- Best-in-class $R_{DS(on)} \times Q_{fr}$
- Excellent $R_{DS(on)} \times Q_{oss}$ and $R_{DS(on)} \times Q_g$
- Unique combination of low C_{rss}/C_{iss} and high $V_{GS(th)}$
- Infineon proprietary die attach technology
- Driver source pin available

Benefits

- Enhanced robustness and reliability for bus voltages beyond 500 V
- Superior efficiency in hard switching
- Higher switching frequency in soft switching topologies
- Robustness against parasitic turn on for unipolar gate driving
- Reduced switching losses through improved gate control

Potential applications

Uni- and bidirectional On Board Chargers and HV-LV DCDC converters:

- hard switching half bridges
- soft switching topologies

Product validation

Qualified according to AEC Q101

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.

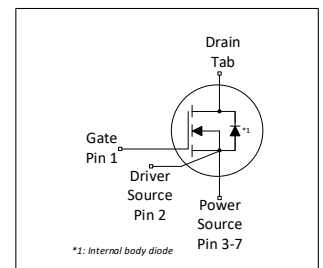
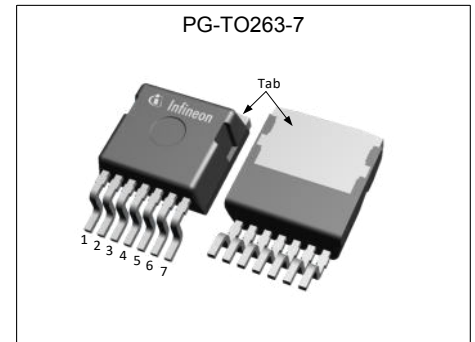


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DSS} over full $T_{j,range}$	750	V
$R_{DS(on),typ}$	90	mΩ
$R_{DS(on),max}$	117	mΩ
$Q_{G,typ}$	15	nC
$I_{DM,max}$	60	A
$Q_{oss,typ} @ 500 V$	39	nC
$E_{oss,typ} @ 500 V$	6.9	μJ

Type / Ordering Code	Package	Marking	Related Links
AIMBG75R090M1H	PG-TO263-7	75A090M1	see Appendix A

Table of Contents

Description 1

Maximum ratings 3

Thermal characteristics 4

Operating range 4

Electrical characteristics 5

Electrical characteristics diagrams 7

Test Circuits 12

Package Outlines 13

Appendix A 14

Revision History 15

Trademarks 15

Disclaimer 15

1 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous DC drain current ¹⁾	I_{DDC}	-	-	24 17	A	$T_C = 25\text{ °C}$ $T_C = 100\text{ °C}$
Peak drain current ²⁾	I_{DM}	-	-	60	A	$T_C = 25\text{ °C}$, $V_{GS} = 18\text{ V}$
Avalanche energy, single pulse	E_{AS}	-	-	75	mJ	$I_D = 2.8\text{ A}$, $V_{DD} = 50\text{ V}$; see table 11
Avalanche current, single pulse	I_{AS}	-	-	2.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	200	V/ns	$V_{DS} = 0...500\text{ V}$
Gate source voltage (static)	V_{GS}	-5	-	23	V	-
Gate source voltage (transient)	V_{GS}	-10	-	25	V	$t_{pulse} \leq 500\text{ ns}$, duty cycle $\leq 1\%$
Power dissipation	P_{tot}	-	-	128	W	$T_C = 25\text{ °C}$
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	175	°C	-
Mounting torque	-	-	-	n. a.	Ncm	M3 and M3.5 screws
Continuous reverse drain current ¹⁾	I_{SDC}	-	-	24 15	A	$V_{GS} = 18\text{ V}$, $T_C = 25\text{ °C}$ $V_{GS} = 0\text{ V}$, $T_C = 25\text{ °C}$
Peak reverse drain current ²⁾	I_{SM}	-	-	60 19	A	$T_C = 25\text{ °C}$, $t_p \leq 250\text{ ns}$ $T_C = 25\text{ °C}$
Insulation withstand voltage	V_{ISO}	-	-	n. a.	V	V_{rms} , $T_C = 25\text{ °C}$, $t = 1\text{ min}$

¹⁾ Limited by $T_{j,max}$

²⁾ Pulse width t_p limited by $T_{j,max}$

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	-	1.17	°C/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, reflow soldering allowed	T_{solder}	-	-	260	°C	reflow MSL1

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate-source voltage operating range including undershoots ¹⁾	V_{GS}	-2	-	20	V	-
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-	V	-

¹⁾ **Important notice:** If the gate source voltage of the device in application exceeds the operating range (Table 4), the device $R_{DS(on)}$ and $V_{GS(th)}$ might exceed the maximum value stated in the datasheet at the end of the lifetime of the device. In order to ensure sound operation of the device over the planned lifetime, the maximum ratings (Table 2) and the application note AN2018-09 must be considered.

4 Electrical characteristics

at $T_j = 25\text{ °C}$, unless otherwise specified

Table 5 Static characteristics

For applications with applied blocking voltage > 525 V, it is required that the customer evaluates the impact of cosmic radiation effect in early design phase and contacts the Infineon sales office for the necessary technical support.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source voltage ¹⁾	V_{DS}	750	-	-	V	$V_{GS} = 0\text{ V}$, $I_D = 0.26\text{ mA}$, $T_j = -55\text{ °C}$ to 175 °C
Gate threshold voltage ²⁾	$V_{GS(th)}$	3.5	4.3	5.6	V	$V_{DS} = V_{GS}$, $I_D = 2.6\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	1 10	75 -	μA	$V_{DS} = 750\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 25\text{ °C}$ $V_{DS} = 750\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 175\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	111 90 83 162	- 117 -	$\text{m}\Omega$	$V_{GS} = 15\text{ V}$, $I_D = 7.4\text{ A}$, $T_j = 25\text{ °C}$ $V_{GS} = 18\text{ V}$, $I_D = 7.4\text{ A}$, $T_j = 25\text{ °C}$ $V_{GS} = 20\text{ V}$, $I_D = 7.4\text{ A}$, $T_j = 25\text{ °C}$ $V_{GS} = 18\text{ V}$, $I_D = 7.4\text{ A}$, $T_j = 175\text{ °C}$
Internal gate resistance	$R_{G,int}$	-	8	-	Ω	$f = 1\text{ MHz}$

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	542	-	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $f = 250\text{ kHz}$
Reverse transfer capacitance	C_{rss}	-	3.2	-	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $f = 250\text{ kHz}$
Output capacitance ³⁾	C_{oss}	-	43	56	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $f = 250\text{ kHz}$
Output charge ³⁾	Q_{oss}	-	39	50	nC	calculation based on C_{oss}
Effective output capacitance, energy related ⁴⁾	$C_{o(er)}$	-	56	-	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{...}500\text{ V}$
Effective output capacitance, time related ⁵⁾	$C_{o(tr)}$	-	78	-	pF	$I_D = \text{constant}$, $V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{...}500\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	$V_{DD} = 500\text{ V}$, $V_{GS} = 18\text{ V}$, $I_D = 7.4\text{ A}$, $R_G = 1.8\text{ }\Omega$; see table 10
Rise time	t_r	-	7	-	ns	$V_{DD} = 500\text{ V}$, $V_{GS} = 18\text{ V}$, $I_D = 7.4\text{ A}$, $R_G = 1.8\text{ }\Omega$; see table 10
Turn-off delay time	$t_{d(off)}$	-	13	-	ns	$V_{DD} = 500\text{ V}$, $V_{GS} = 18\text{ V}$, $I_D = 7.4\text{ A}$, $R_G = 1.8\text{ }\Omega$; see table 10
Fall time	t_f	-	10	-	ns	$V_{DD} = 500\text{ V}$, $V_{GS} = 18\text{ V}$, $I_D = 7.4\text{ A}$, $R_G = 1.8\text{ }\Omega$; see table 10

¹⁾ Tested at $T_j = 25\text{ °C}$, minimum V_{DSS} verified by design over full junction temperature range.

²⁾ Tested after 1 ms pulse at $V_{GS} = +20\text{ V}$. "Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.

³⁾ Maximum specification is defined by calculated six sigma upper confidence bound

⁴⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 500 V.

⁵⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 500 V.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	4.3	-	nC	$V_{DD} = 500\text{ V}$, $I_D = 7.4\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$
Gate to drain charge	Q_{GD}	-	3.7	-	nC	$V_{DD} = 500\text{ V}$, $I_D = 7.4\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$
Total gate charge	Q_G	-	15	-	nC	$V_{DD} = 500\text{ V}$, $I_D = 7.4\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	V_{SD}	-	3.9	5.3	V	$V_{GS} = 0\text{ V}$, $I_S = 7.4\text{ A}$, $T_j = 25\text{ °C}$
MOSFET forward recovery time	t_{fr}	- -	15 8	- -	ns	$V_{DD} = 500\text{ V}$, $I_S = 7.4\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$; see table 9 $V_{DD} = 500\text{ V}$, $I_S = 7.4\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9
MOSFET forward recovery charge ¹⁾	Q_{fr}	- -	46 78	- -	nC	$V_{DD} = 500\text{ V}$, $I_S = 7.4\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$; see table 9 $V_{DD} = 500\text{ V}$, $I_S = 7.4\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9
MOSFET peak forward recovery current	I_{frm}	- -	6 19	- -	A	$V_{DD} = 500\text{ V}$, $I_S = 7.4\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$; see table 9 $V_{DD} = 500\text{ V}$, $I_S = 7.4\text{ A}$, $di_S/dt = 4000\text{ A}/\mu\text{s}$; see table 9

¹⁾ Q_{fr} includes Q_{oss}

5 Electrical characteristics diagrams

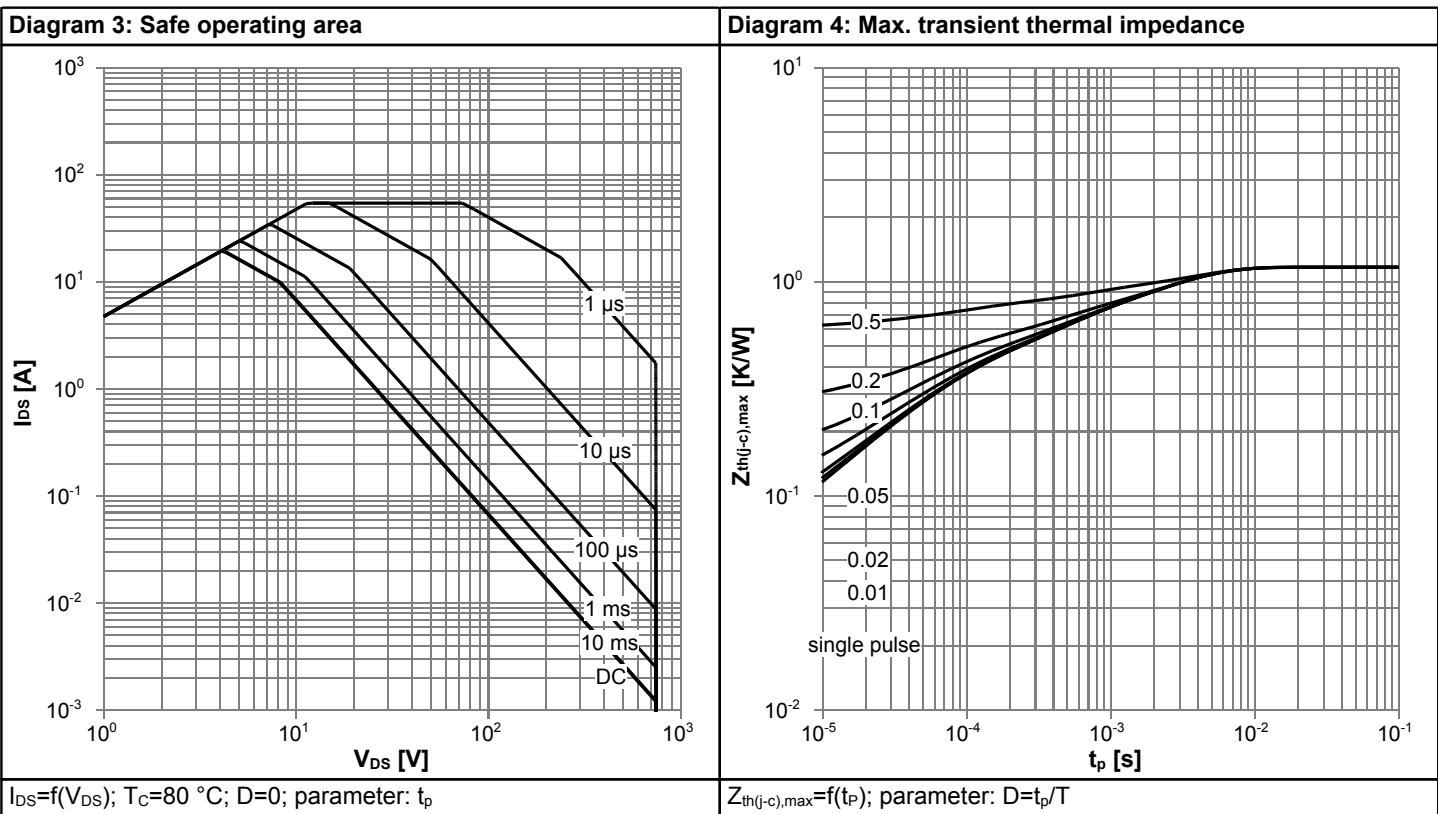
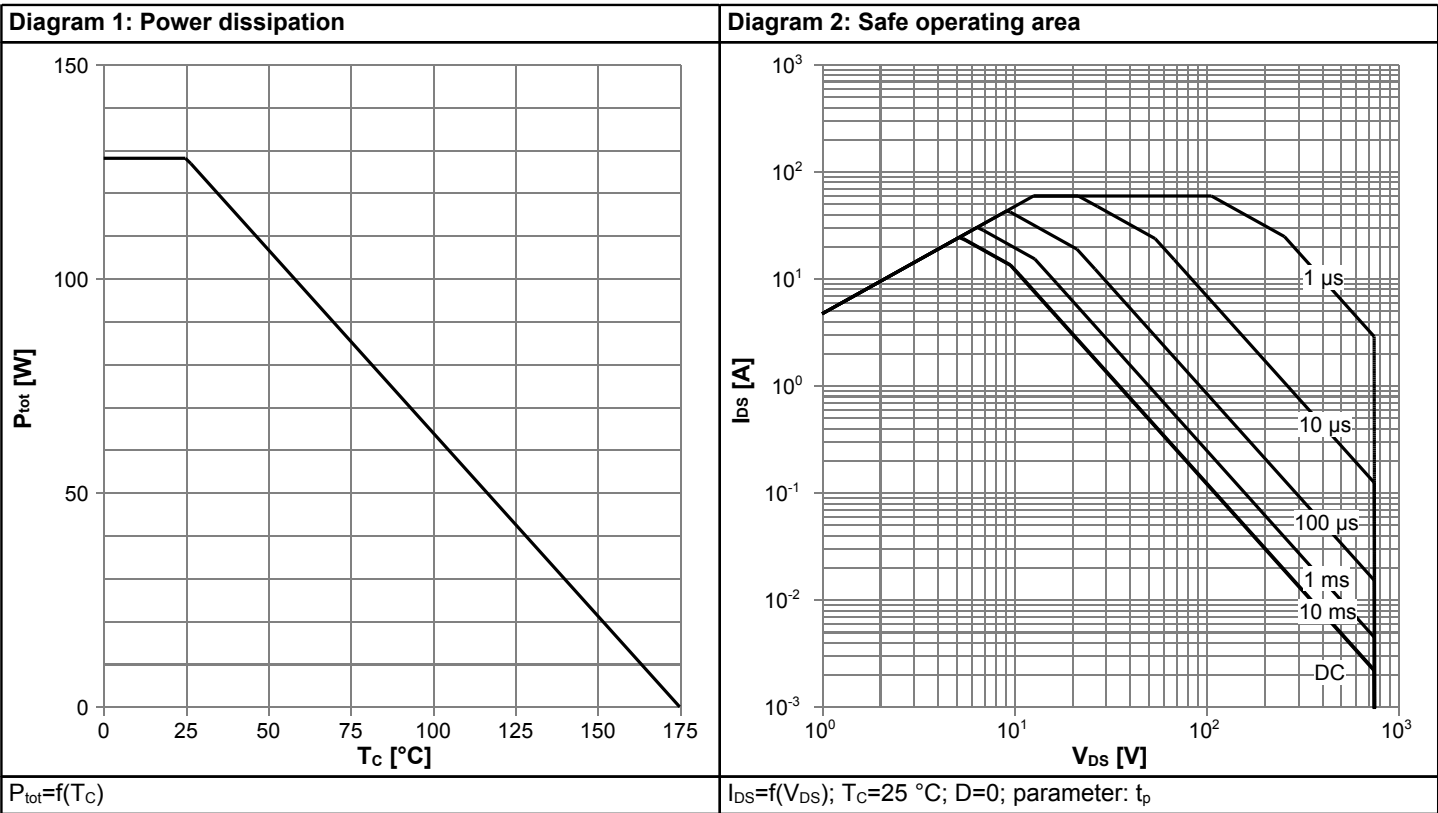
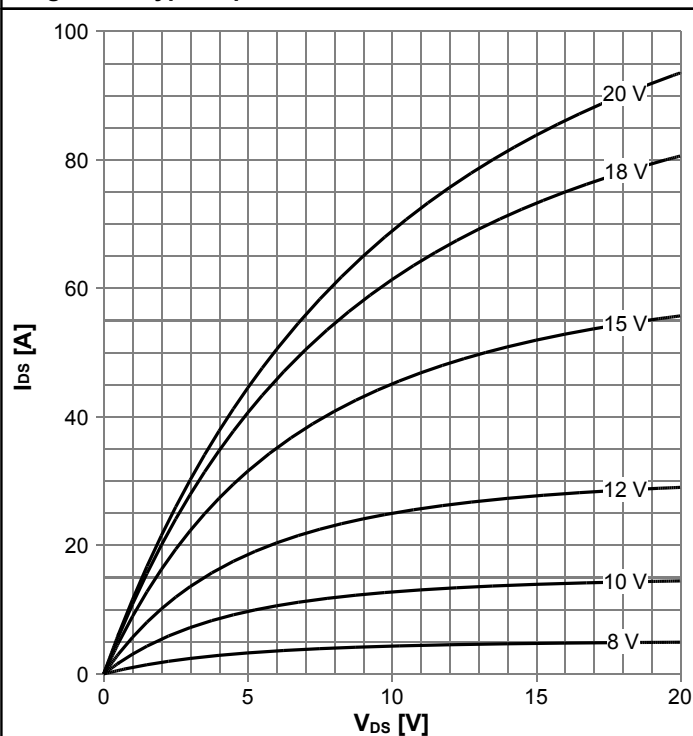
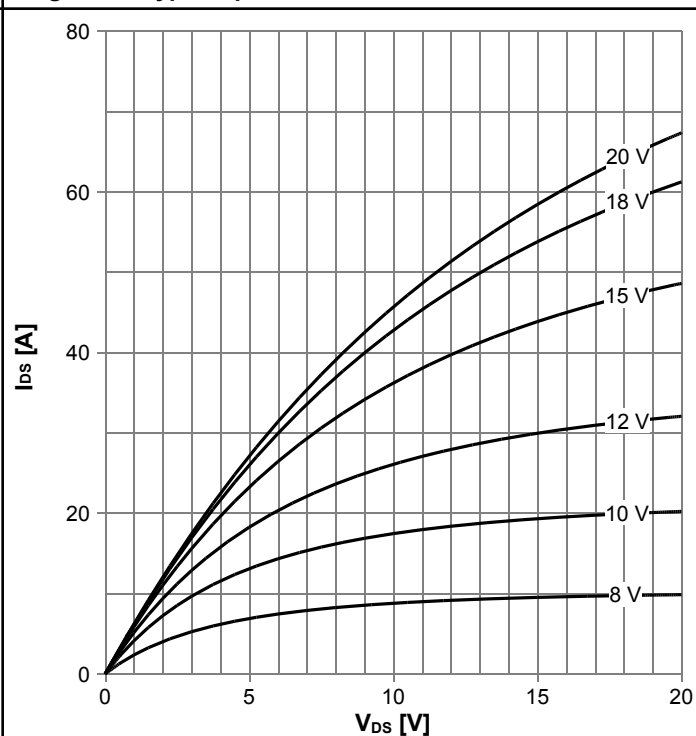


Diagram 5: Typ. output characteristics



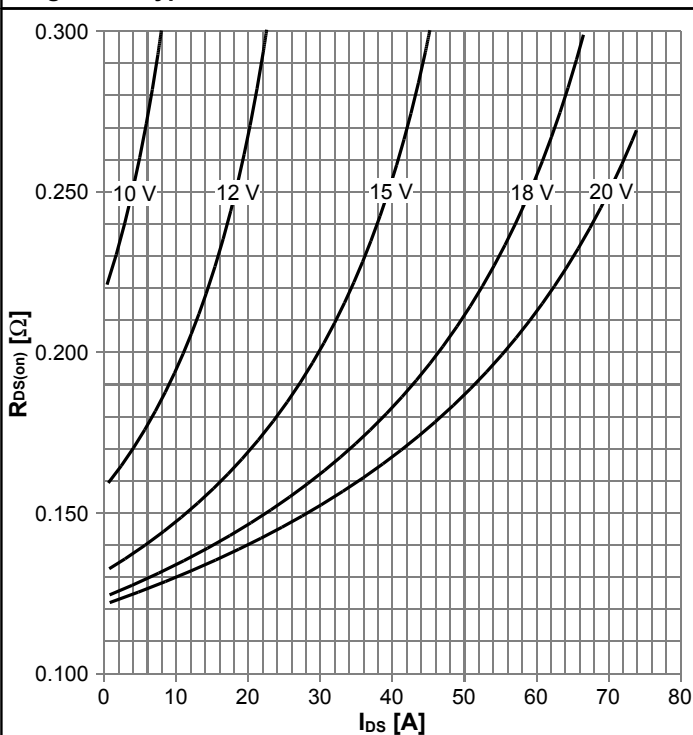
$I_{DS}=f(V_{DS})$; $T_J=25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



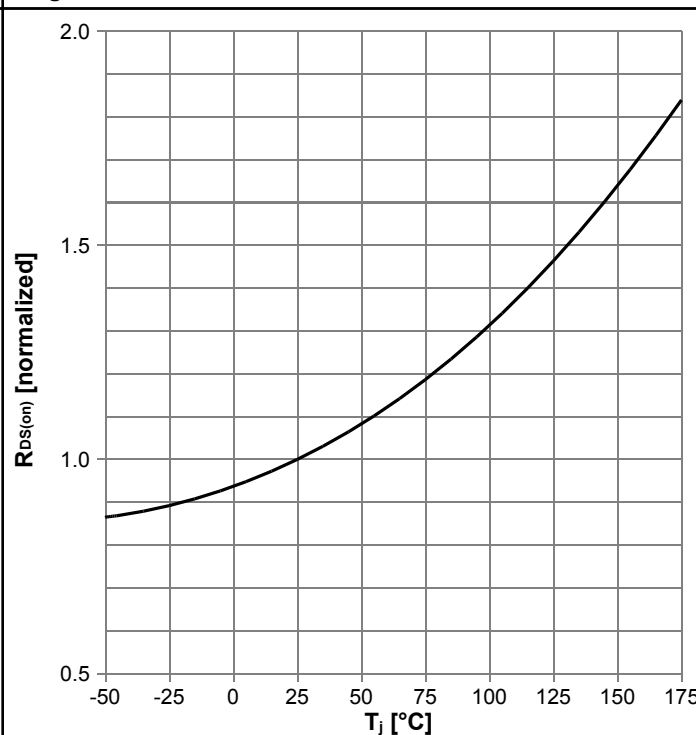
$I_{DS}=f(V_{DS})$; $T_J=175\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_{DS})$; $T_J=125\text{ °C}$; parameter: V_{GS}

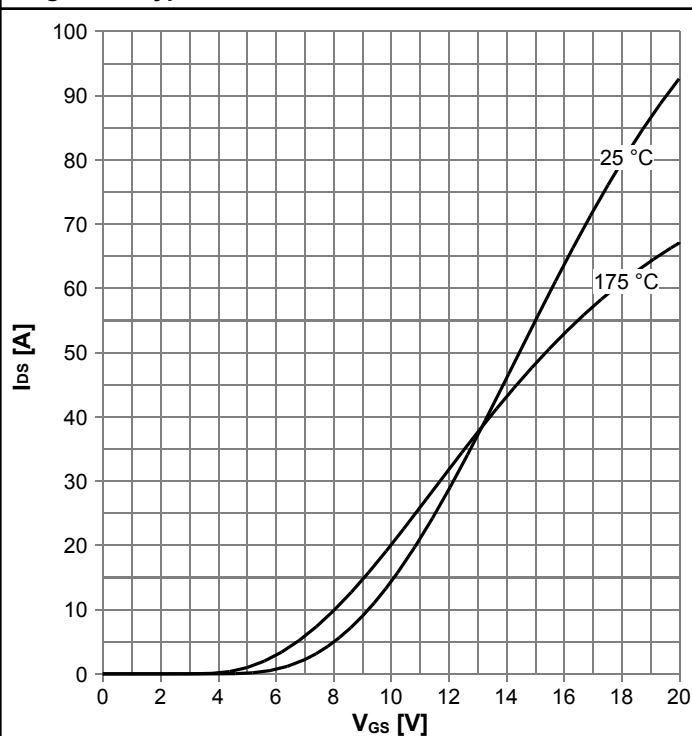
Diagram 8: Drain-source on-state resistance



$R_{DS(on)}=f(T_J)$; $I_D=7.4\text{ A}$; $V_{GS}=18\text{ V}$

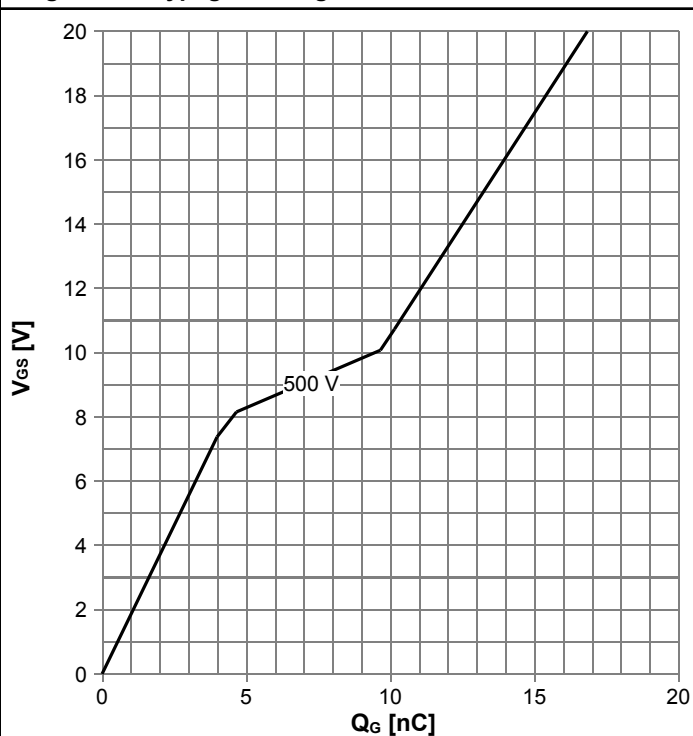
CoolSiC™ Automotive Power Device 750 V G1
AIMBG75R090M1H

Diagram 9: Typ. transfer characteristics



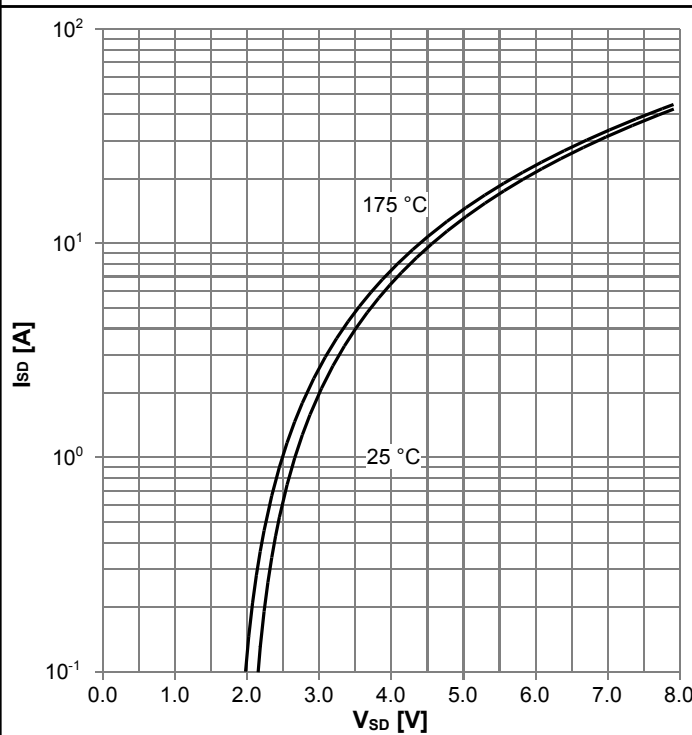
$I_{DS}=f(V_{GS})$; $V_{DS}=20\text{ V}$; parameter: T_j

Diagram 10: Typ. gate charge



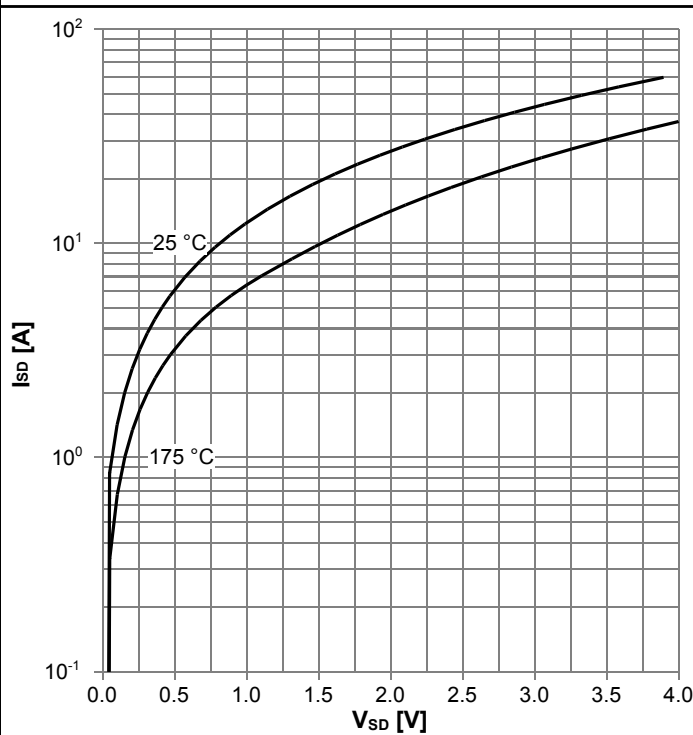
$V_{GS}=f(Q_G)$; $I_D=7.4\text{ A}$ pulsed; parameter: V_{DD}

Diagram 11: Typ. reverse drain current characteristics

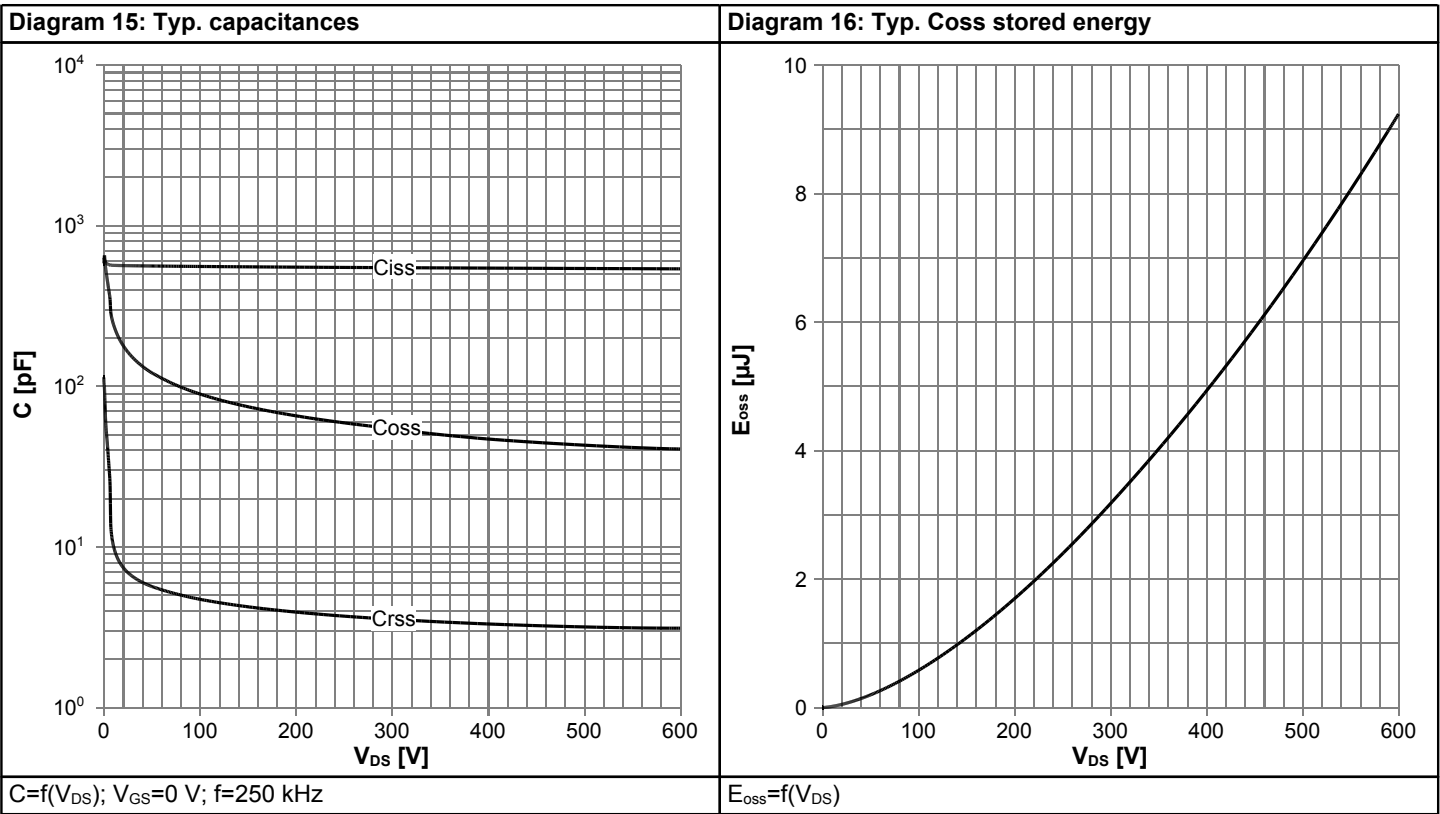
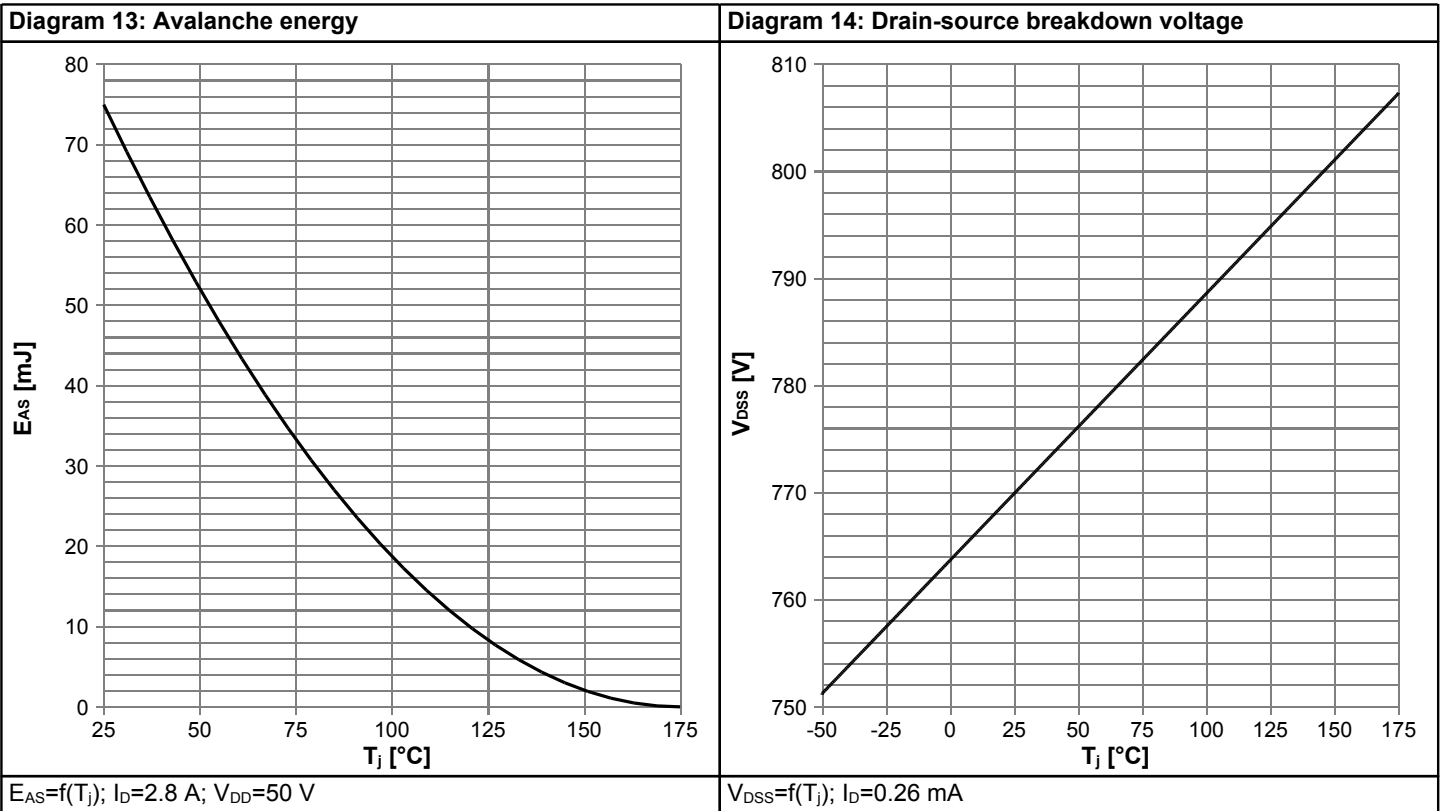


$I_{SD}=f(V_{SD})$; $V_{GS}=0\text{ V}$; parameter: T_j

Diagram 12: Typ. reverse drain current characteristics

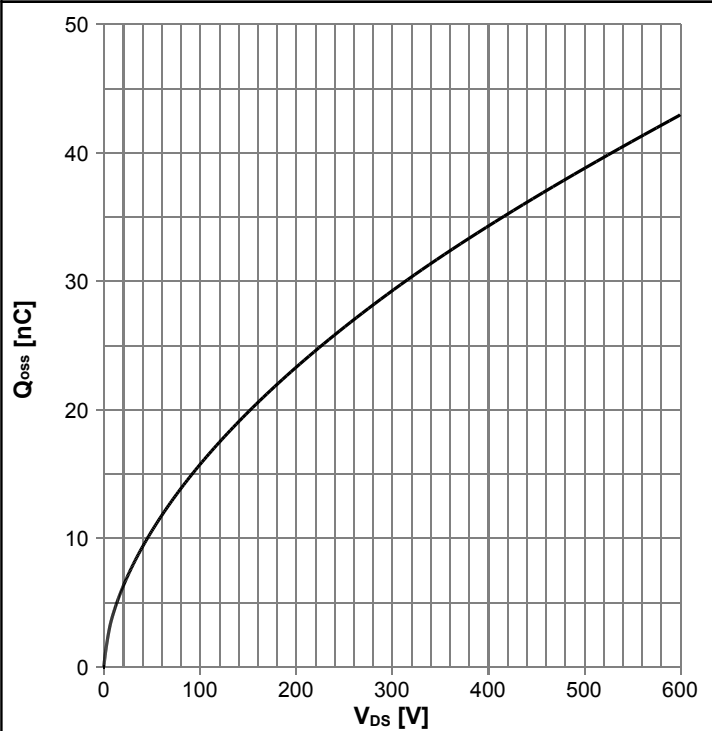


$I_{SD}=f(V_{SD})$; $V_{GS}=18\text{ V}$; parameter: T_j



CoolSiC™ Automotive Power Device 750 V G1
AIMBG75R090M1H

Diagram 17: Typ. Qoss output charge



$Q_{oss}=f(V_{DS})$

6 Test Circuits

Table 9 Body diode characteristics

Test circuit for body diode characteristics	Body diode recovery waveform

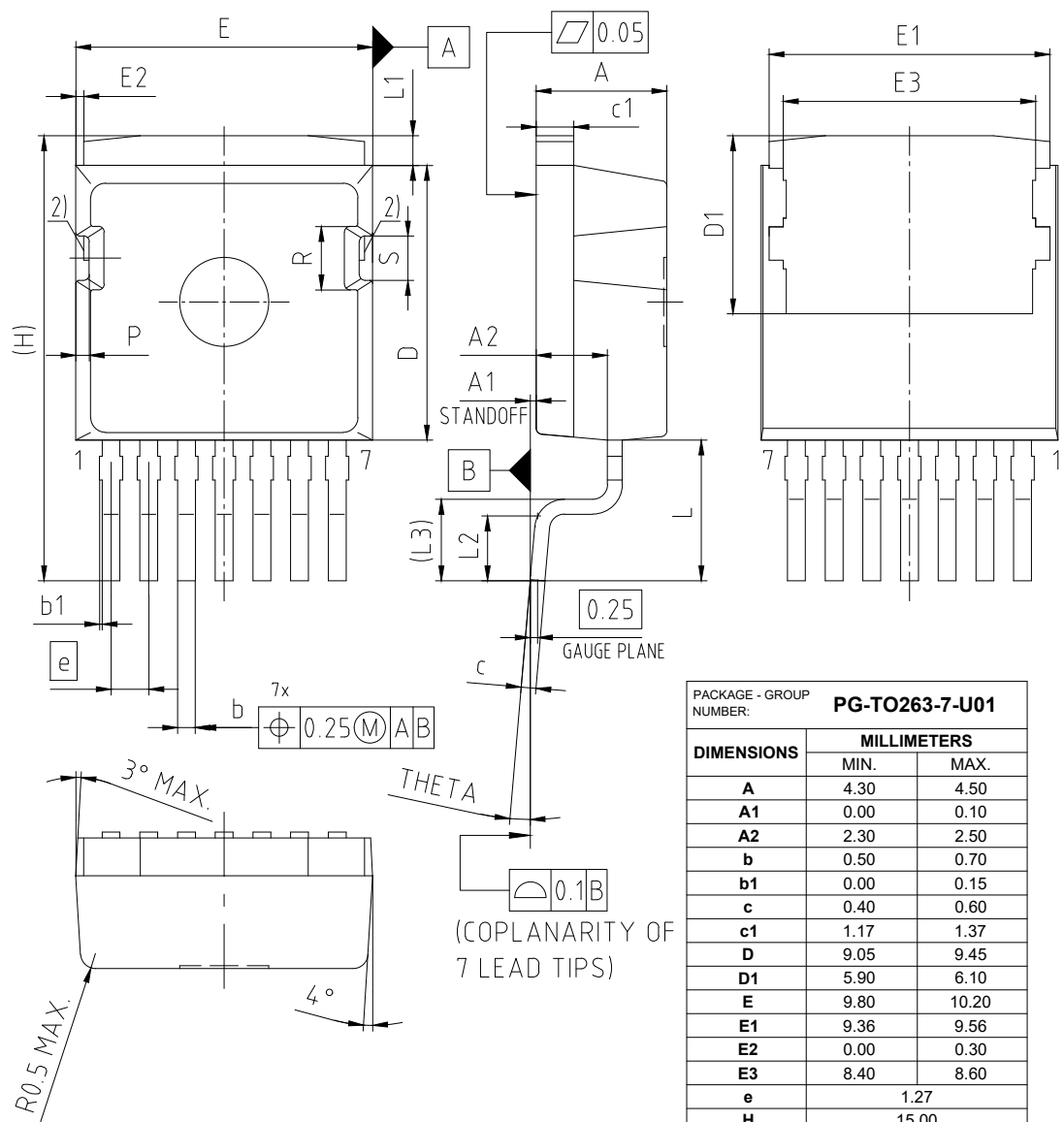
Table 10 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

7 Package Outlines



NOTES:
1) ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT
2) MOLD FILLING IS ACCEPTABLE AT THIS AREA

Figure 1 Outline PG-TO263-7, dimensions in mm

8 Appendix A

Table 12 Related Links

- IFX CoolSiC™ Automotive Power Device 750 V G1 Webpage: www.infineon.com
- IFX CoolSiC™ Automotive Power Device 750 V G1 application note: www.infineon.com
- IFX CoolSiC™ Automotive Power Device 750 V G1 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

AIMBG75R090M1H

Revision: 2024-03-11, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-03-11	Release of final version

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Disclaimer

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

erratum@infineon.com

Published by

Infineon Technologies AG

81726 München, Germany

© 2023 Infineon Technologies AG

All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life.

If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.