

Final datasheet

CoolSiC™ 1200 V SiC Trench MOSFET

Features

- $V_{DS} = 1200\text{ V}$ at $T_{vj} = -55...175^\circ\text{C}$
- $I_{DC} = 55\text{ A}$ at $T_C = 25^\circ\text{C}$
- $R_{DS(on)} = 40\text{ m}\Omega$ at $V_{GS} = 20\text{ V}$, $T_{vj} = 25^\circ\text{C}$
- New performance-optimized chip technology (Gen1p) with improved $R_{DS(on)}$ * A FOM
- Increased recommended turn-on voltage ($V_{GS(on)} = 20\text{ V}$) for lower $R_{DS(on)}$
- Best in class switching energy for lower switching losses and reduced cooling efforts
- Lowest device capacitances for higher switching speeds and higher power density
- A combination of low C_{rss}/C_{iss} ratio and high $V_{GS(th)}$ to avoid parasitic turn-on and enable unipolar gate driving
- Reduced total gate charge Q_{Gtot} for lower driving power and losses
- .XT die attach technology for best in class thermal performance
- Sense pin for optimized switching performance
- Suitable for HV creepage requirements

Potential applications

- On-board charger
- DC/DC converter
- Auxiliary drives

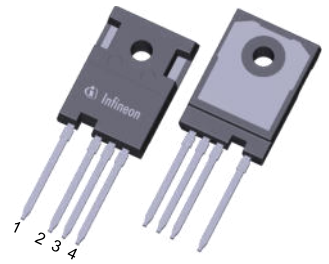
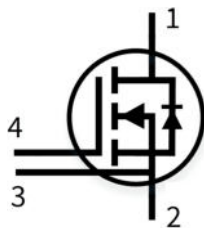
Product validation

- Qualified for Automotive Applications. Product Validation according to AEC-Q100/101

Description

Pin definition:

- 1 – drain
- 2 – source
- 3 – Kelvin sense contact
- 4 – gate



Type	Package	Marking
AIMZHN120R040M1T	PG-TO247-4-STD-NN6.7	A12M1N040



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1 Package

1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}				260	°C
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			0.43	0.56	K/W

Note: Not subject to production test. Parameter verified by design/characterization.

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} = -55...175\text{ °C}$		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 20\text{ V}$	$T_c = 25\text{ °C}$	55	A
			$T_c = 100\text{ °C}$	39	
Peak drain current, t_p limited by $T_{vj(max)}$	I_{DM}	$V_{GS} = 20\text{ V}$		140	A
Gate-source voltage, max. transient voltage ¹⁾	V_{GS}	$t_p \leq 0.5\text{ }\mu\text{s}$, $D < 0.01$		-10...25	V
Gate-source voltage, max. static voltage	V_{GS}			-5...23	V
Avalanche energy, single pulse	E_{AS}	$I_D = 15\text{ A}$, $V_{DD} = 50\text{ V}$, $L = 2.41\text{ mH}$		269	mJ
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25\text{ °C}$	268	W
			$T_c = 100\text{ °C}$	134	

1) **Important note:** The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		20	V
Recommended turn-off gate voltage	$V_{GS(off)}$		0	V

Table 4 **Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	$I_D = 20 \text{ A}$	$T_{vj} = 25 \text{ °C}$, $V_{GS(on)} = 20 \text{ V}$		40	50	mΩ
			$T_{vj} = 100 \text{ °C}$, $V_{GS(on)} = 20 \text{ V}$		56		
			$T_{vj} = 175 \text{ °C}$, $V_{GS(on)} = 20 \text{ V}$		80		
			$T_{vj} = 25 \text{ °C}$, $V_{GS(on)} = 18 \text{ V}$		44		
Gate-source threshold voltage	$V_{GS(th)}$	$I_D = 6.4 \text{ mA}$, $V_{DS} = V_{GS}$ (tested after 1 ms pulse at $V_{GS} = 20 \text{ V}$)	$T_{vj} = 25 \text{ °C}$	3.5	4.3	5.1	V
			$T_{vj} = 175 \text{ °C}$		3.8		
Zero gate-voltage drain current	I_{DSS}	$V_{DS} = 1200 \text{ V}$, $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ °C}$		0.3	19	μA
			$T_{vj} = 175 \text{ °C}$		50		
Gate leakage current	I_{GSS}	$V_{DS} = 0 \text{ V}$	$V_{GS} = 25 \text{ V}$			100	nA
			$V_{GS} = -10 \text{ V}$			-100	
Forward transconductance	g_{fs}	$I_D = 20 \text{ A}$, $V_{DS} = 20 \text{ V}$			12		S
Short-circuit withstand time ¹⁾	t_{SC}	$V_{DD} \leq 800 \text{ V}$, $V_{DS,peak} \leq 1200 \text{ V}$, $T_{vj(start)} = 25 \text{ °C}$, $R_{G,ext} = 2 \text{ } \Omega$	$V_{GS(on)} = 20 \text{ V}$		1.5		μs
			$V_{GS(on)} = 18 \text{ V}$		2		
			$V_{GS(on)} = 15 \text{ V}$		2.5		
Internal gate resistance	$R_{G,int}$	$f = 1 \text{ MHz}$, $V_{AC} = 25 \text{ mV}$			3.7		Ω
Input capacitance	C_{iss}	$V_{DD} = 800 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 100 \text{ kHz}$, $V_{AC} = 25 \text{ mV}$			1264		pF
Output capacitance	C_{oss}	$V_{DD} = 800 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 100 \text{ kHz}$, $V_{AC} = 25 \text{ mV}$			63		pF
Reverse transfer capacitance	C_{rss}	$V_{DD} = 800 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 100 \text{ kHz}$, $V_{AC} = 25 \text{ mV}$			3.6		pF
C_{oss} stored energy	E_{oss}	$V_{DD} = 800 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 100 \text{ kHz}$, $V_{AC} = 25 \text{ mV}$			40		μJ
Total gate charge	Q_G	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, turn-on pulse			43		nC
Plateau gate charge	$Q_{GS(pl)}$	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, turn-on pulse			12		nC
Gate-to-drain charge	Q_{GD}	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, turn-on pulse			7		nC
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, $R_{GS(on)} = 2 \text{ } \Omega$, $R_{GS(off)} = 2 \text{ } \Omega$, $L_\sigma = 15 \text{ nH}$	$T_{vj} = 25 \text{ °C}$		10		ns
			$T_{vj} = 175 \text{ °C}$		10		

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Rise time	t_r	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, $R_{GS(on)} = 2 \Omega$, $R_{GS(off)} = 2 \Omega$, $L_\sigma = 15 \text{ nH}$	$T_{vj} = 25 \text{ }^\circ\text{C}$	7		ns
			$T_{vj} = 175 \text{ }^\circ\text{C}$	10		
Turn-off delay time	$t_{d(off)}$	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, $R_{GS(on)} = 2 \Omega$, $R_{GS(off)} = 2 \Omega$, $L_\sigma = 15 \text{ nH}$	$T_{vj} = 25 \text{ }^\circ\text{C}$	20		ns
			$T_{vj} = 175 \text{ }^\circ\text{C}$	22		
Fall time	t_f	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, $R_{GS(on)} = 2 \Omega$, $R_{GS(off)} = 2 \Omega$, $L_\sigma = 15 \text{ nH}$	$T_{vj} = 25 \text{ }^\circ\text{C}$	8		ns
			$T_{vj} = 175 \text{ }^\circ\text{C}$	8		
Turn-on energy	E_{on}	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, $R_{GS(on)} = 2 \Omega$, $R_{GS(off)} = 2 \Omega$, $L_\sigma = 15 \text{ nH}$	$T_{vj} = 25 \text{ }^\circ\text{C}$	112		μJ
			$T_{vj} = 175 \text{ }^\circ\text{C}$	181		
Turn-off energy	E_{off}	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, $R_{GS(on)} = 2 \Omega$, $R_{GS(off)} = 2 \Omega$, $L_\sigma = 15 \text{ nH}$	$T_{vj} = 25 \text{ }^\circ\text{C}$	56		μJ
			$T_{vj} = 175 \text{ }^\circ\text{C}$	64		
Total switching energy	E_{tot}	$V_{DD} = 800 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 0/20 \text{ V}$, $R_{GS(on)} = 2 \Omega$, $R_{GS(off)} = 2 \Omega$, $L_\sigma = 15 \text{ nH}$	$T_{vj} = 25 \text{ }^\circ\text{C}$	168		μJ
			$T_{vj} = 175 \text{ }^\circ\text{C}$	245		
Virtual junction temperature	T_{vj}		-55		175	$^\circ\text{C}$

1) verified by the design/characterization

Note: Dynamic test circuit see Fig. F.

3 Body diode (MOSFET)

Table 5 Maximum rated values

Parameter	Symbol	Note or test condition	Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} = -55...175 \text{ }^\circ\text{C}$	1200	V
Continuous reverse drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{SDC}	$V_{GS} = 0 \text{ V}$	$T_c = 25 \text{ }^\circ\text{C}$	A
			$T_c = 100 \text{ }^\circ\text{C}$	
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	$V_{GS} = 0 \text{ V}$	45	A

Table 6 **Characteristic values**

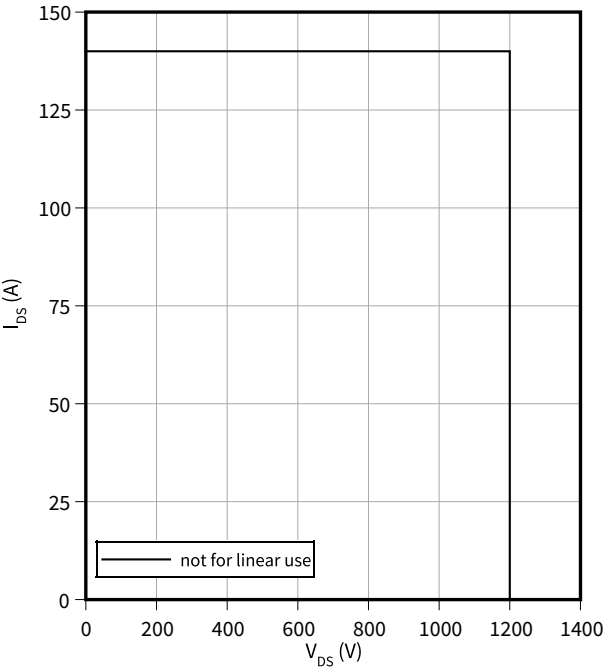
Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	$I_{SD} = 20 \text{ A}$, $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ °C}$		3.9	5	V
			$T_{vj} = 100 \text{ °C}$		3.8		
			$T_{vj} = 175 \text{ °C}$		3.7		
MOSFET forward recovery charge	Q_{fr}	$V_{DD} = 800 \text{ V}$, $I_{SD} = 20 \text{ A}$, $V_{GS} = 0 \text{ V}$, $di_{SD}/dt = 3000 \text{ A}/\mu\text{s}$, Q_{fr} includes also Q_C	$T_{vj} = 25 \text{ °C}$		135		nC
			$T_{vj} = 175 \text{ °C}$		350		
MOSFET peak forward recovery current	I_{frm}	$V_{DD} = 800 \text{ V}$, $I_{SD} = 20 \text{ A}$, $V_{GS} = 0 \text{ V}$, $di_{SD}/dt = 3000 \text{ A}/\mu\text{s}$, Q_{fr} includes also Q_C	$T_{vj} = 25 \text{ °C}$		9		A
			$T_{vj} = 175 \text{ °C}$		17		
Virtual junction temperature	T_{vj}			-55		175	°C

4 Characteristics diagrams

4 Characteristics diagrams

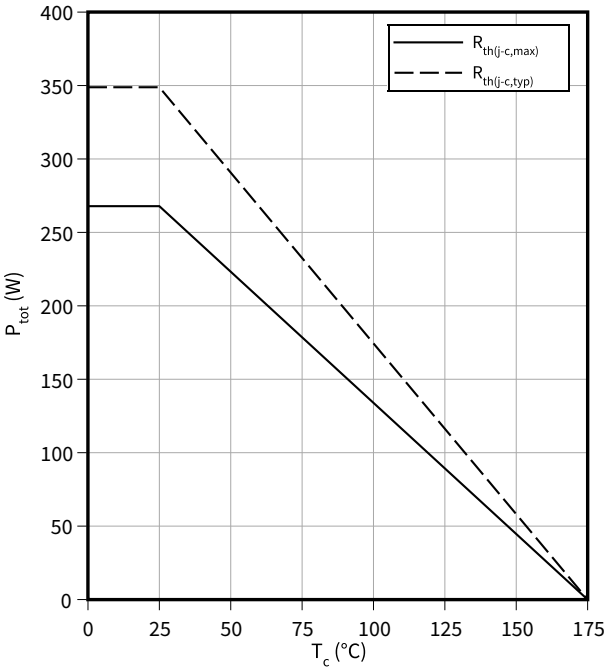
Reverse bias safe operating area (RBSOA)

$I_{DS} = f(V_{DS})$
 $T_{vj} \leq 175\text{ °C}, V_{GS} = 0/20\text{ V}, T_c = 25\text{ °C}$



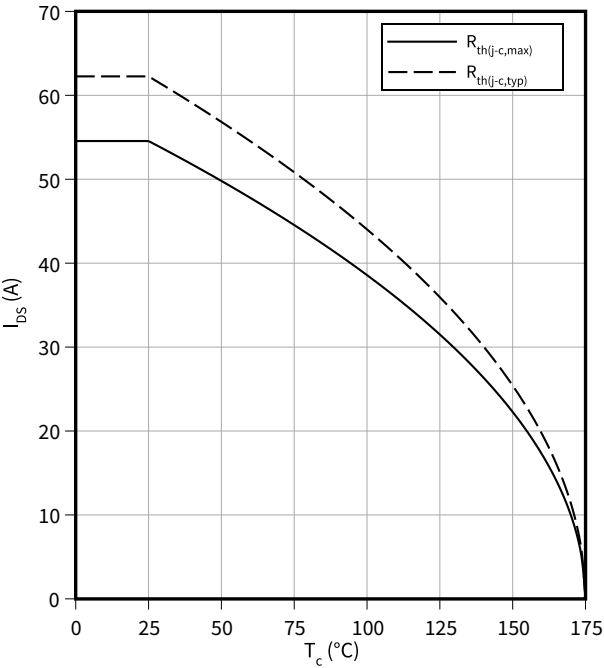
Power dissipation as a function of case temperature

$P_{tot} = f(T_c)$



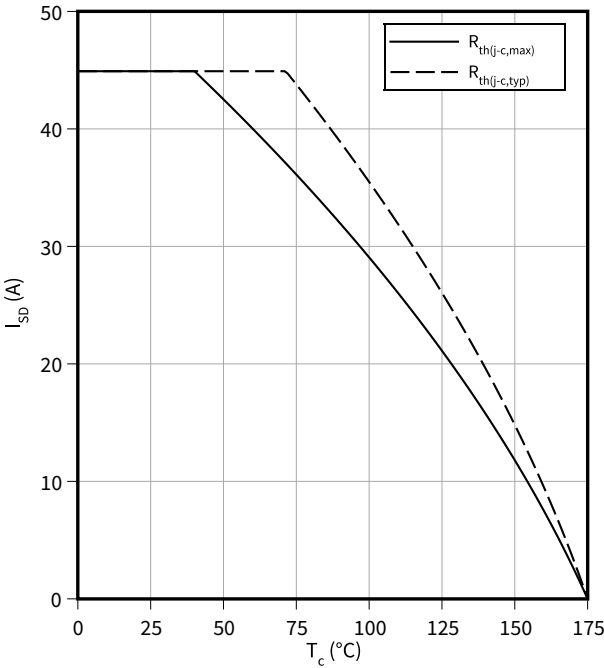
Maximum DC drain to source current as a function of case temperature

$I_{DS} = f(T_c)$



Maximum source to drain current as a function of case temperature

$I_{SD} = f(T_c)$
 $V_{GS} = 0\text{ V}$

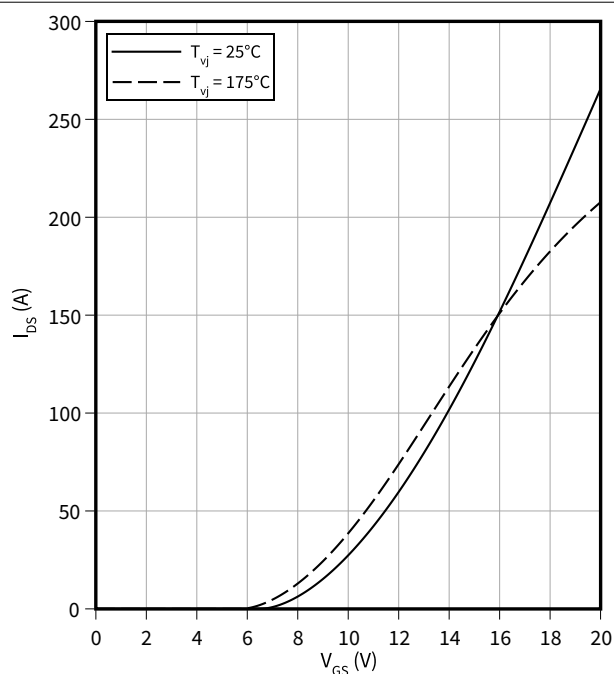


4 Characteristics diagrams

Typical transfer characteristic

$$I_{DS} = f(V_{GS})$$

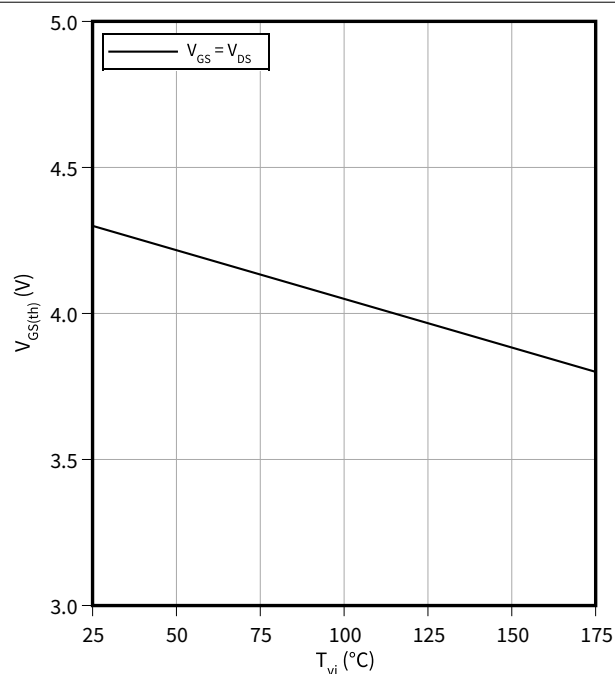
$$V_{DS} = 20 \text{ V}$$



Typical gate-source threshold voltage as a function of junction temperature

$$V_{GS(th)} = f(T_{vj})$$

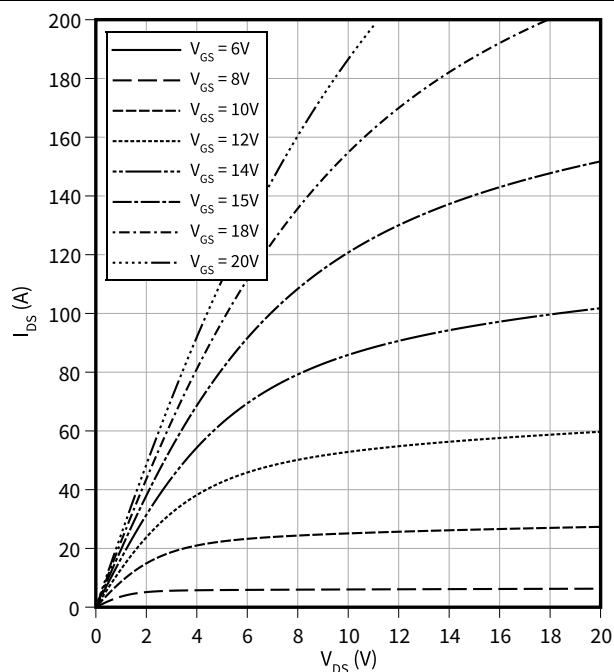
$$I_D = 6.4 \text{ mA}$$



Typical output characteristic, V_{GS} as parameter

$$I_{DS} = f(V_{DS})$$

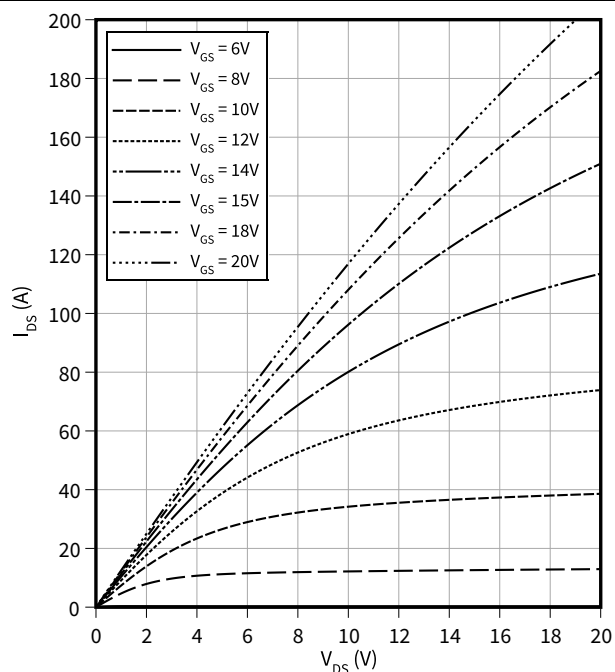
$$T_{vj} = 25^\circ\text{C}$$



Typical output characteristic, V_{GS} as parameter

$$I_{DS} = f(V_{DS})$$

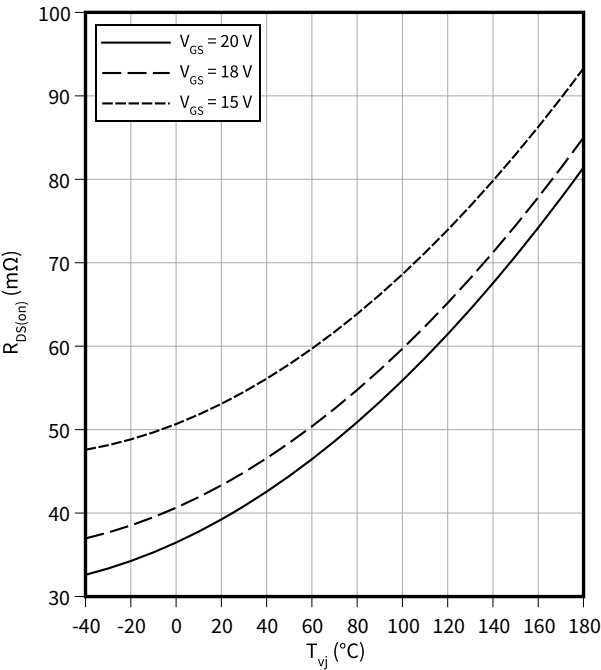
$$T_{vj} = 175^\circ\text{C}$$



4 Characteristics diagrams

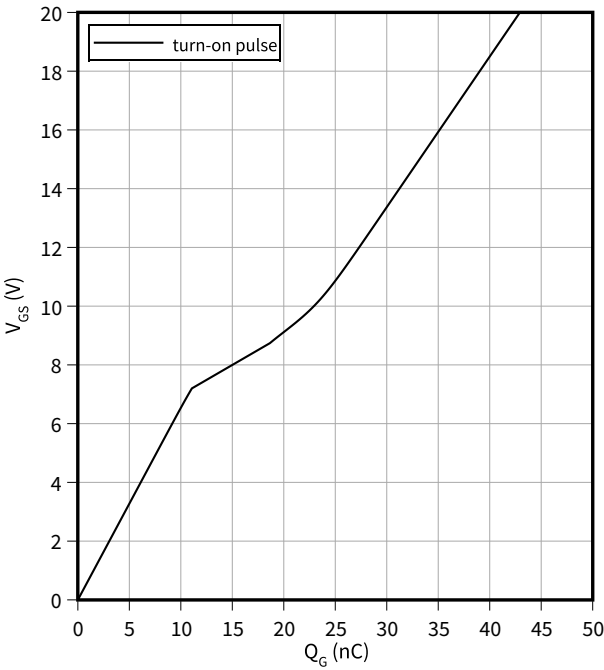
Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$
 $I_D = 20\text{ A}$



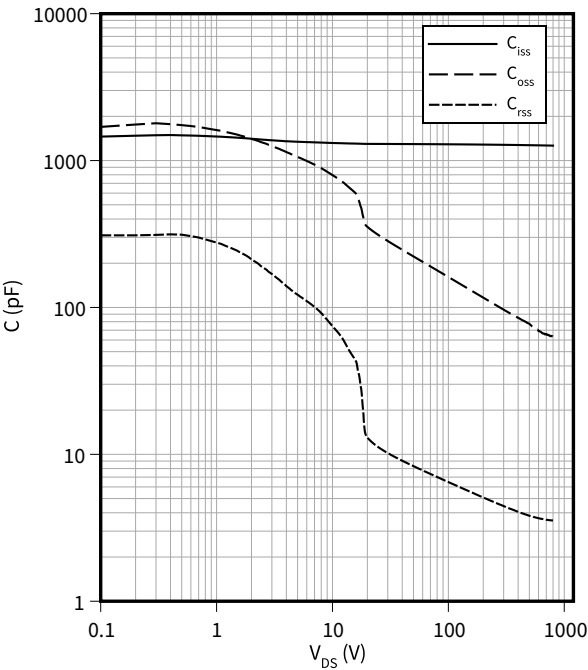
Typical gate charge

$V_{GS} = f(Q_G)$
 $I_D = 20\text{ A}, V_{DS} = 800\text{ V}$



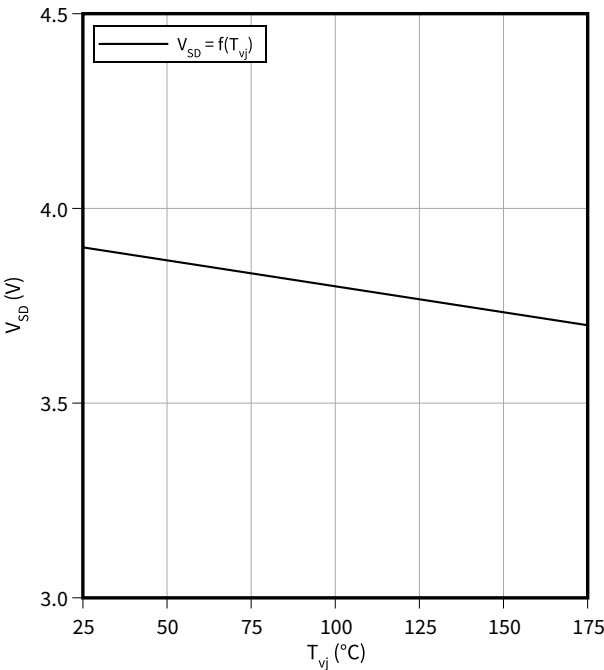
Typical capacitance as a function of drain-source voltage

$C = f(V_{DS})$
 $f = 100\text{ kHz}, V_{GS} = 0\text{ V}$



Typical reverse drain voltage as function of junction temperature

$V_{SD} = f(T_{vj})$
 $I_{SD} = 20\text{ A}, V_{GS} = 0\text{ V}$

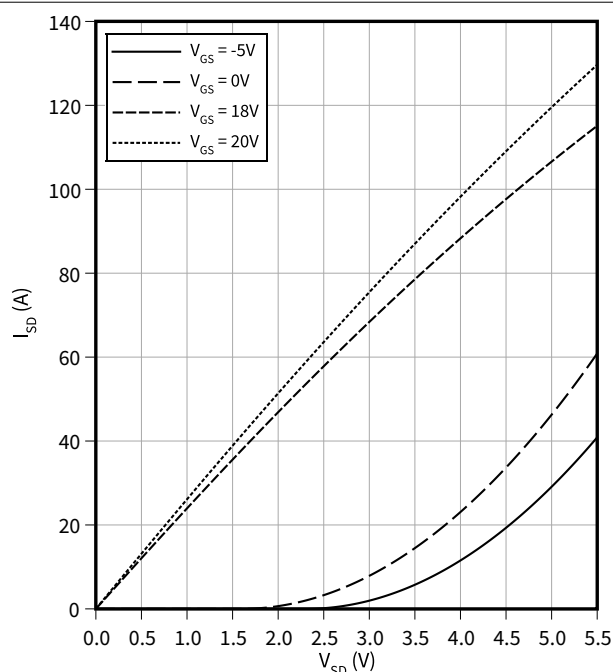


4 Characteristics diagrams

Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$$I_{SD} = f(V_{SD})$$

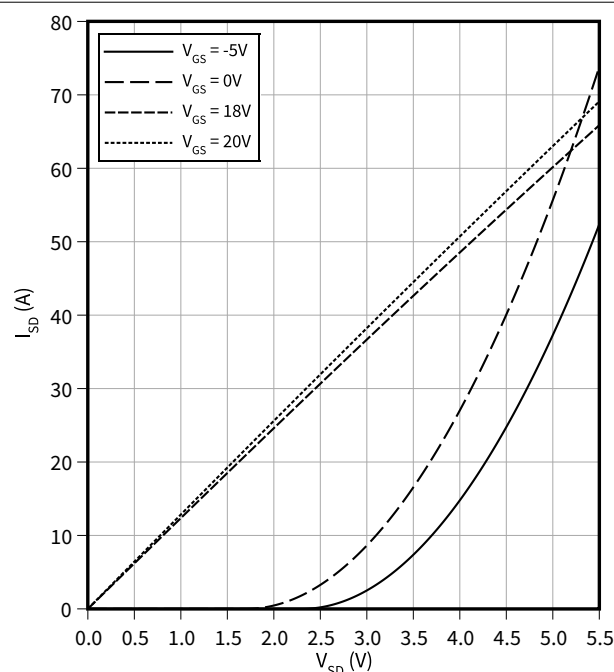
$$T_{vj} = 25\text{ °C}$$



Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$$I_{SD} = f(V_{SD})$$

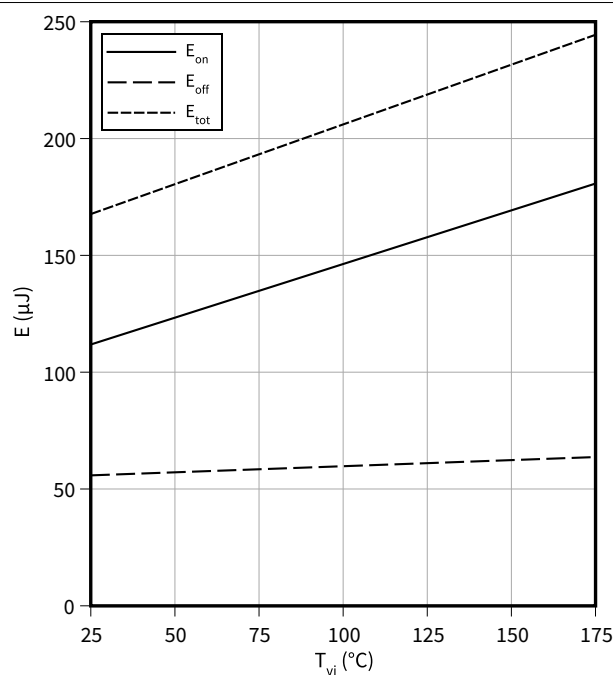
$$T_{vj} = 175\text{ °C}$$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\text{ V}$

$$E = f(T_{vj})$$

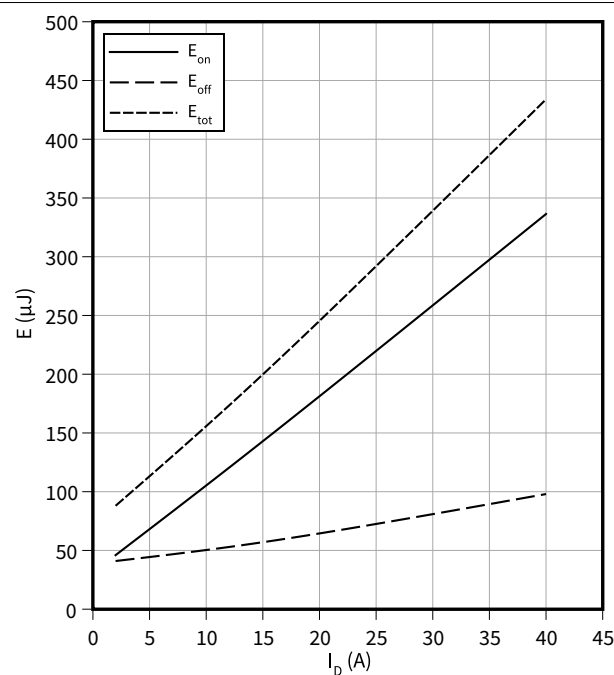
$$V_{GS} = 0/20\text{ V}, I_D = 20\text{ A}, R_{G,ext} = 2\text{ }\Omega, V_{DD} = 800\text{ V}$$



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\text{ V}$

$$E = f(I_D)$$

$$V_{GS} = 0/20\text{ V}, T_{vj} = 175\text{ °C}, R_{G,ext} = 2\text{ }\Omega, V_{DD} = 800\text{ V}$$

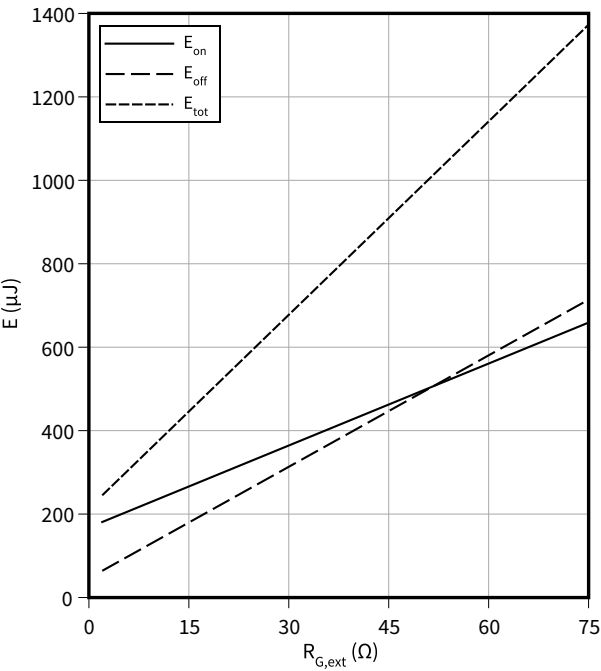


4 Characteristics diagrams

Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\text{ V}$

$E = f(R_{G,ext})$

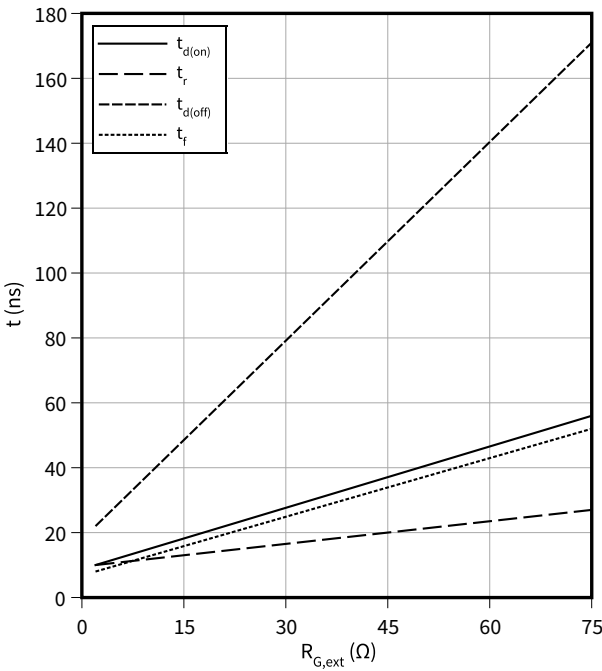
$V_{GS} = 0/20\text{ V}$, $I_D = 20\text{ A}$, $T_{vj} = 175\text{ °C}$, $V_{DD} = 800\text{ V}$



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\text{ V}$

$t = f(R_{G,ext})$

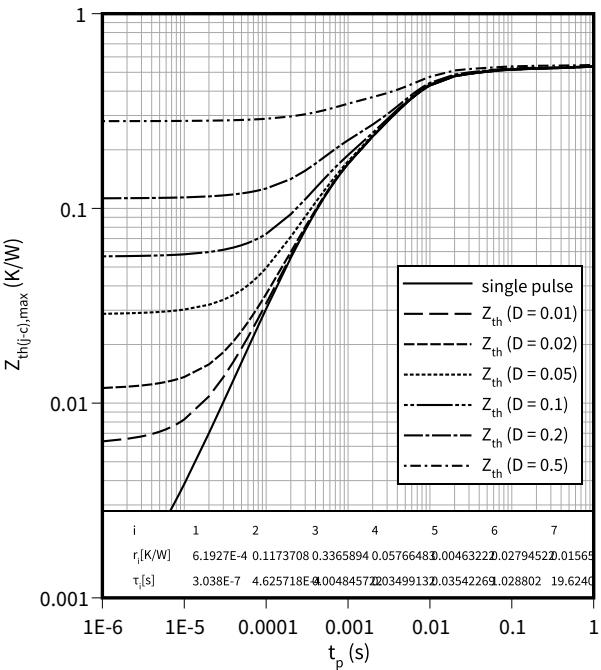
$V_{GS} = 0/20\text{ V}$, $I_D = 20\text{ A}$, $T_{vj} = 175\text{ °C}$, $V_{DD} = 800\text{ V}$



Max. transient thermal impedance (MOSFET/diode)

$Z_{th(j-c),max} = f(t_p)$

$D = t_p/T$



5 Package outlines

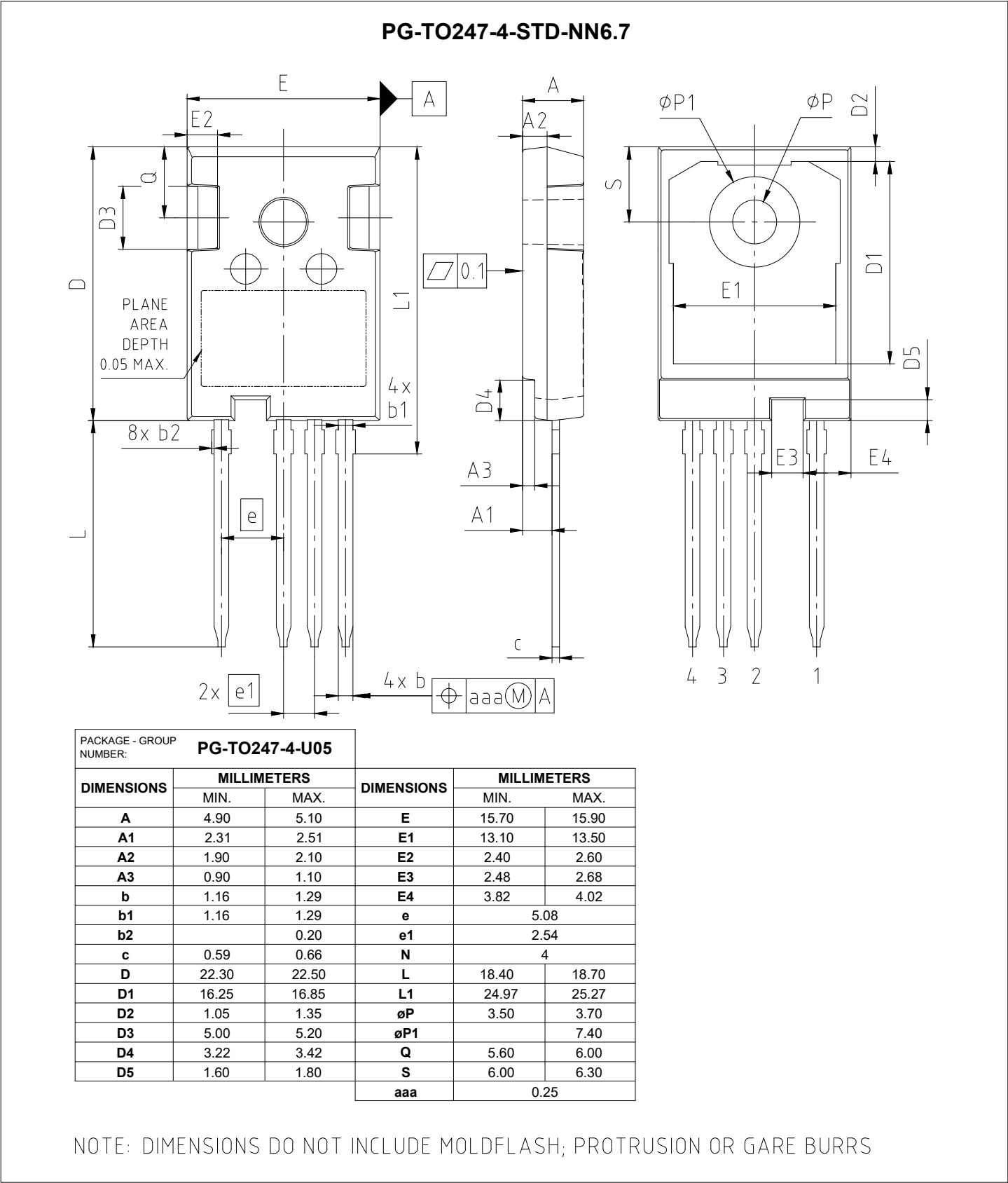


Figure 1

6 Testing conditions

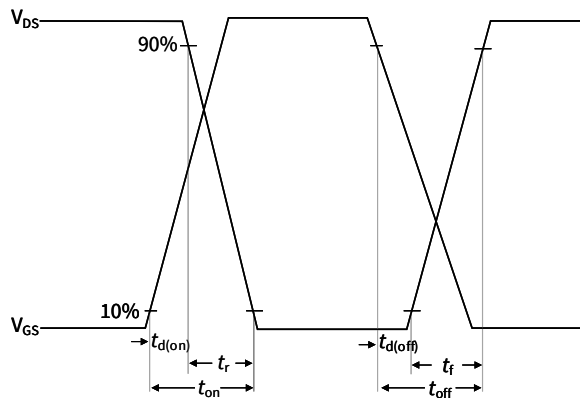


Figure A. Definition of switching times

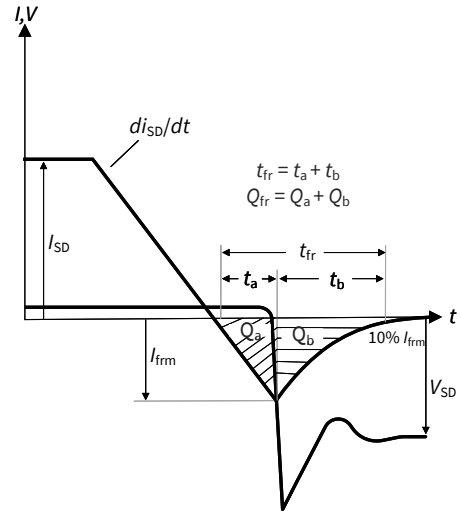


Figure B. Definition of body diode switching characteristics

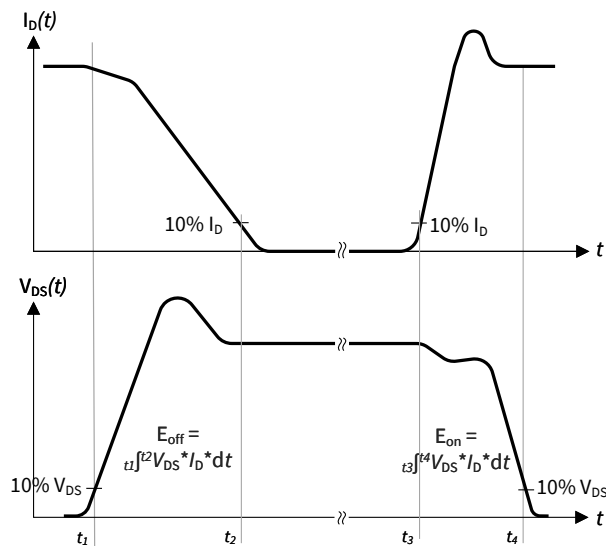


Figure C. Definition of switching losses

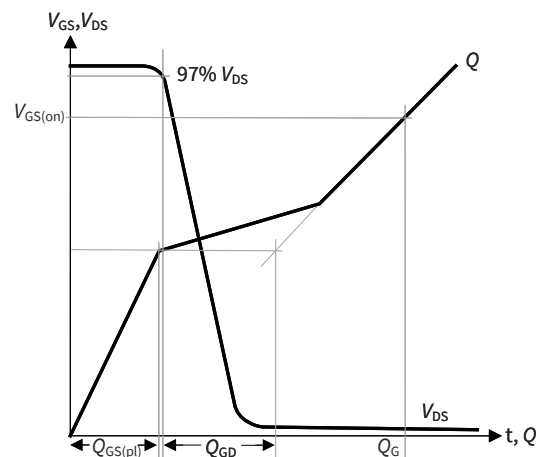


Figure D. Definition of Q_{GD}

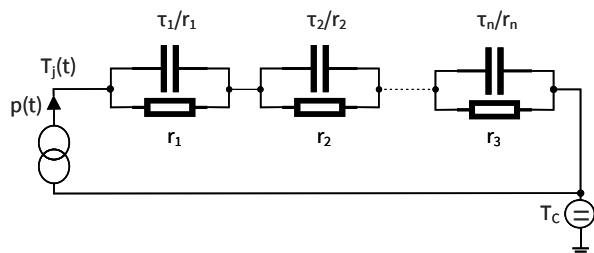


Figure E. Thermal equivalent circuit

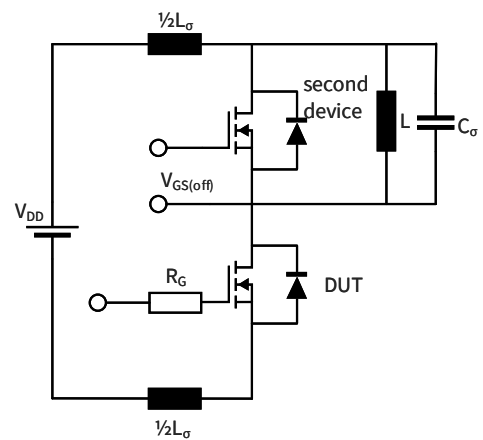


Figure F. Dynamic test circuit

Parasitic inductance L_{σ} ,
Parasitic capacitor C_{σ} ,

Revision history

Document revision	Date of release	Description of changes
0.10	2022-04-19	Target datasheet
0.20	2023-08-03	Preliminary datasheet
1.00	2023-11-30	Final datasheet

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