

MOSFET
OptiMOS™ 5 Power-Transistor, 25 V

Features

- Optimized for OR-ing application
- Very low on-resistance R_DS(on) @ V_GS=4.5 V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Table with 3 columns: Parameter, Value, Unit. Rows include V_DS (25 V), R_DS(on),max (0.45 mΩ), I_D (479 A), Q_oss (70 nC), and Q_G(0V..4.5V) (135 nC).

Table with 4 columns: Type / Ordering code, Package, Marking, Related links. Row 1: BSC004NE2LS5, PG-TDSON-8, 04NE2LS5, -

PG-TDSON-8

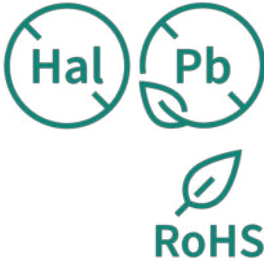
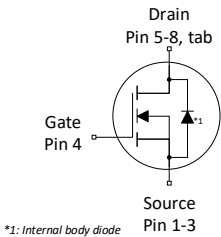
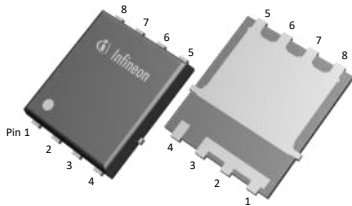




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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	479 338 40	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1914	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	400	mJ	$I_D=20\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	188 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	0.8	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	
Device on PCB, 6 cm ² cooling area	R_{thJA}	-	-	50	°C/W	

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.0	1.5	2.0	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1.0 100	μA	$V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=16\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.40 0.54	0.45 0.85	m Ω	$V_{GS}=10\text{ V}$, $I_D=30\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=30\text{ A}$
Gate resistance	R_G	-	0.7	-	Ω	-
Transconductance	g_{fs}	-	230	-	S	$ V_{DS} \geq 2 I_D $, $R_{DS(on)max}$, $I_D=30\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	11000	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=12.5\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	3600	-	pF	
Reverse transfer capacitance	C_{rss}	-	3100	-	pF	
Turn-on delay time	$t_{d(on)}$	-	28	-	ns	$V_{DD}=12.5\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	88	-	ns	
Turn-off delay time	$t_{d(off)}$	-	68	-	ns	
Fall time	t_f	-	93	-	ns	

Table 6 Gate charge characteristics ⁵⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	24	-	nC	$V_{DD}=12.5\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	15	-	nC	
Gate to drain charge	Q_{gd}	-	69	-	nC	
Switching charge	Q_{sw}	-	78	-	nC	
Gate charge total	Q_g	-	135	-	nC	
Gate plateau voltage	$V_{plateau}$	-	2.2	-	V	$V_{DD}=12.5\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	238	-	nC	
Output charge	Q_{oss}	-	70	-	nC	

⁵⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	188	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1914	A	
Diode forward voltage	V_{SD}	-	0.77	1.0	V	$V_{GS}=0\text{ V}$, $I_F=30\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	55	-	ns	$V_R=12.5\text{ V}$, $I_F=I_S$, $di_F/dt=400\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	250	-	nC	

4 Electrical characteristics diagrams

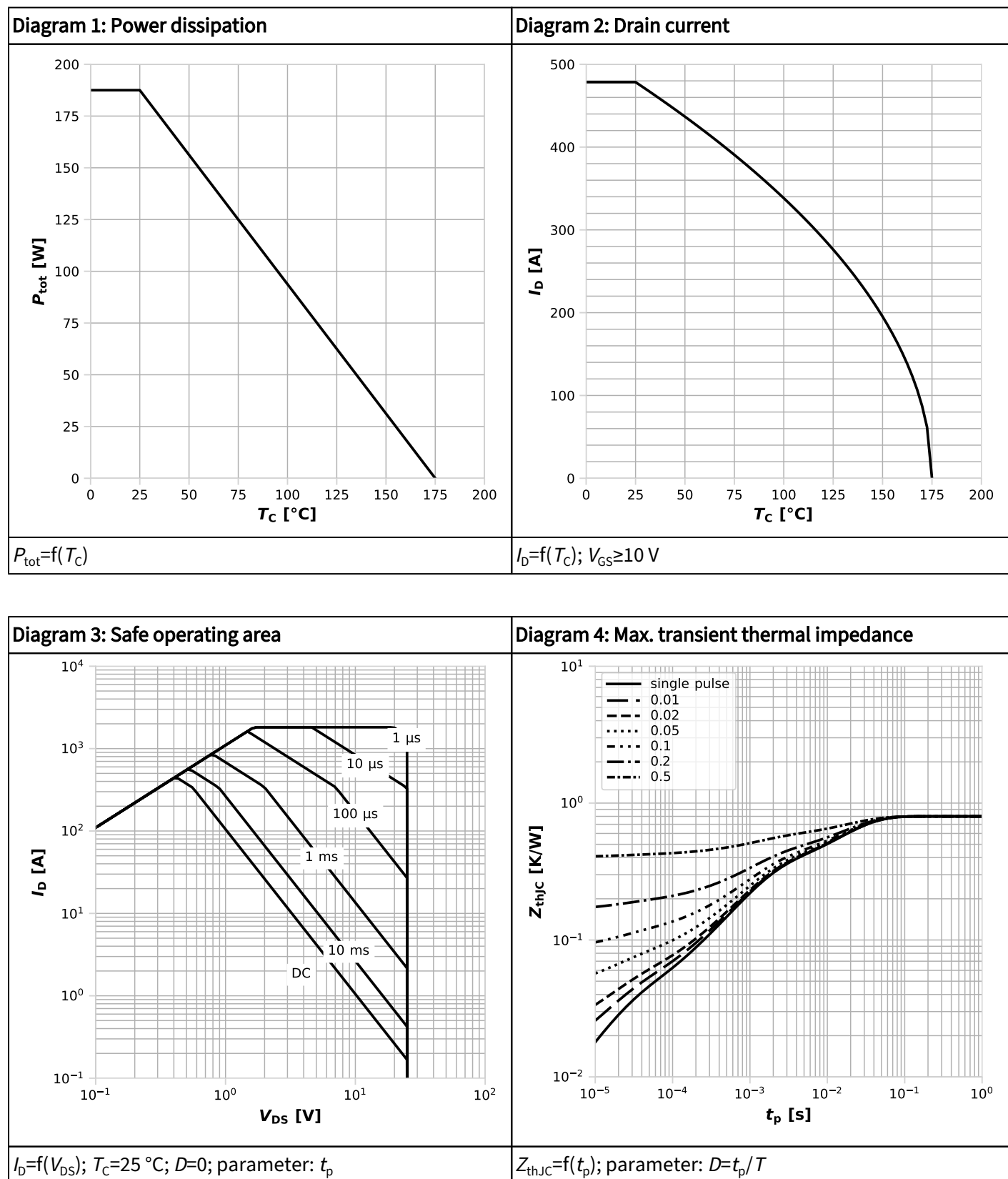
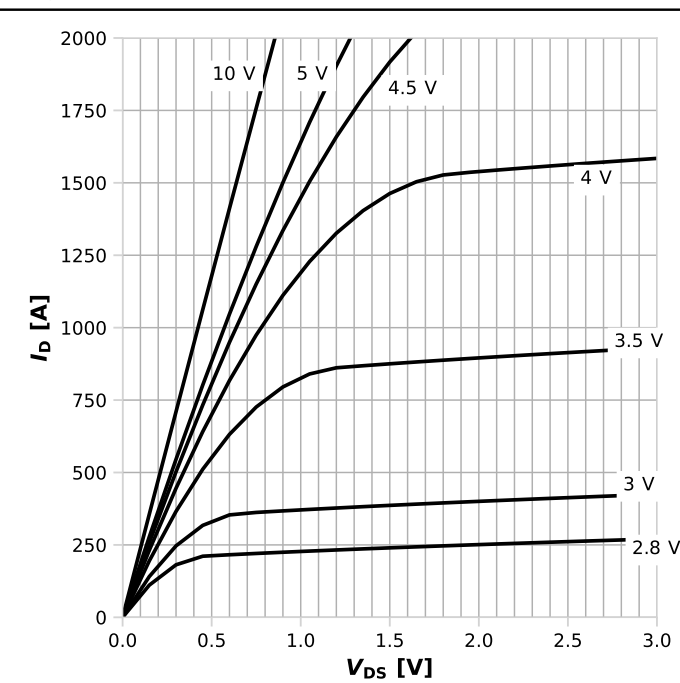
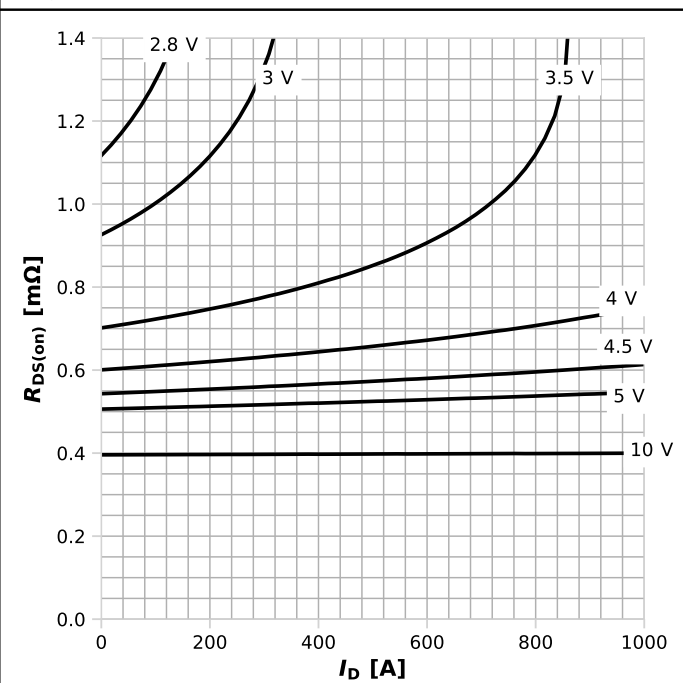


Diagram 5: Typ. output characteristics



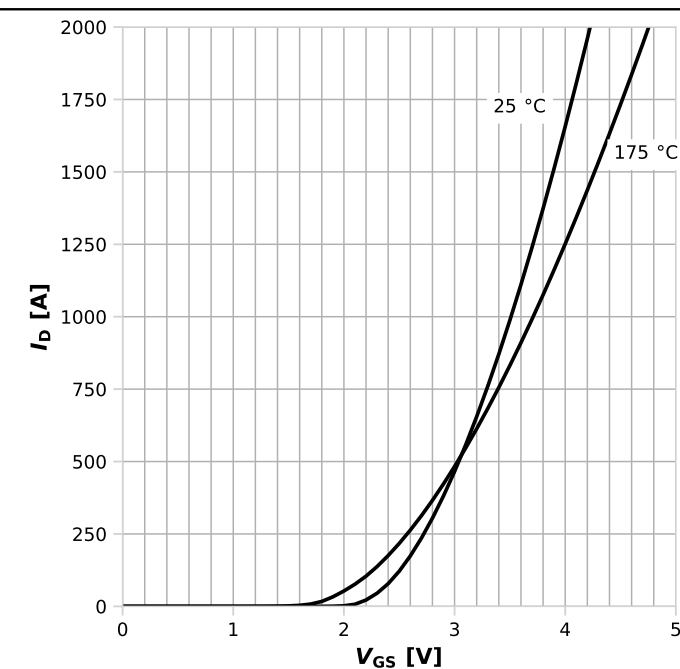
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



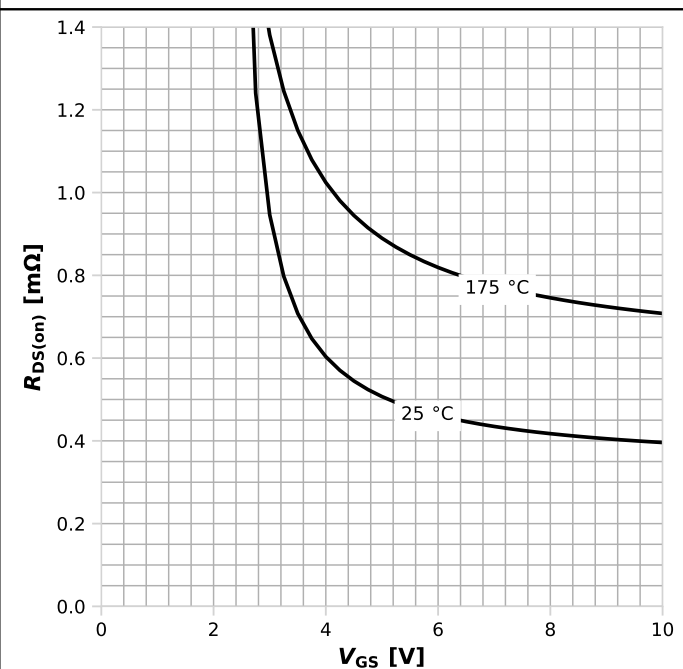
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



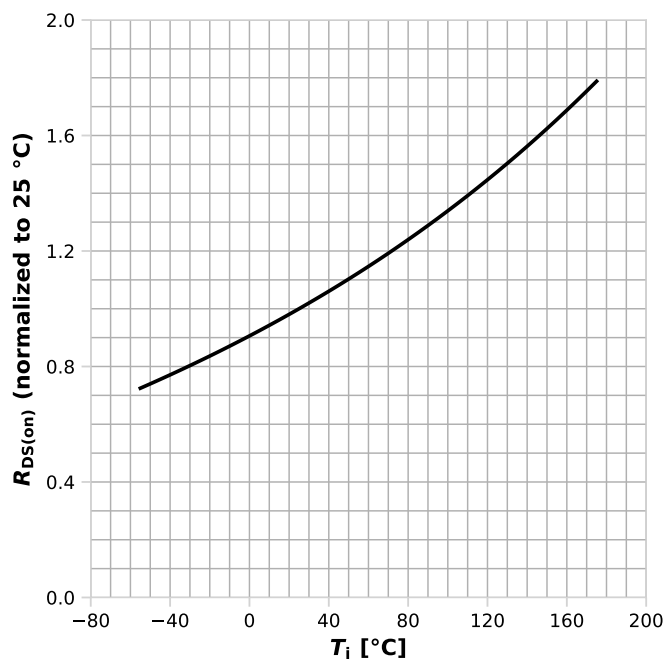
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)\max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



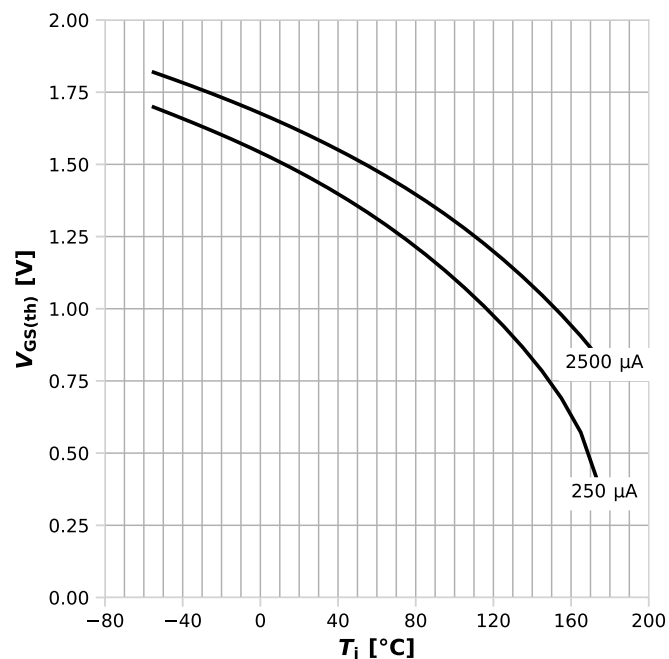
$R_{DS(on)} = f(V_{GS})$, $I_D = 30\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



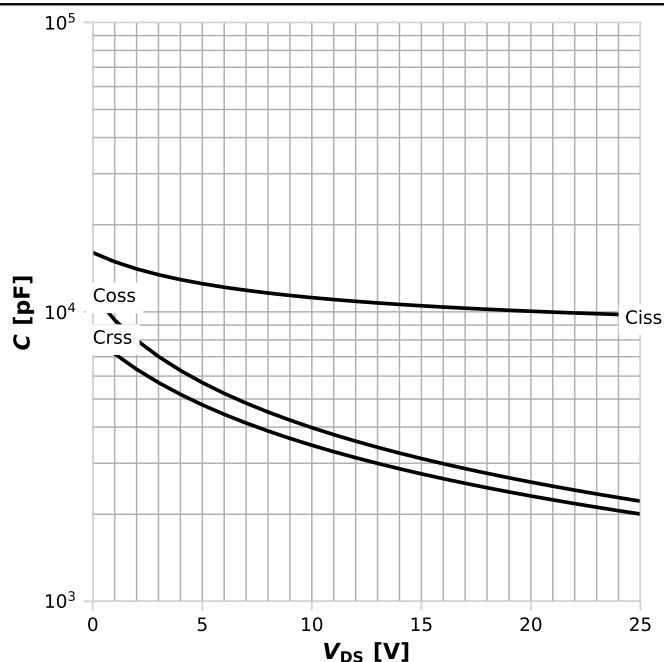
$$R_{DS(on)} = f(T_j), I_D = 30 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



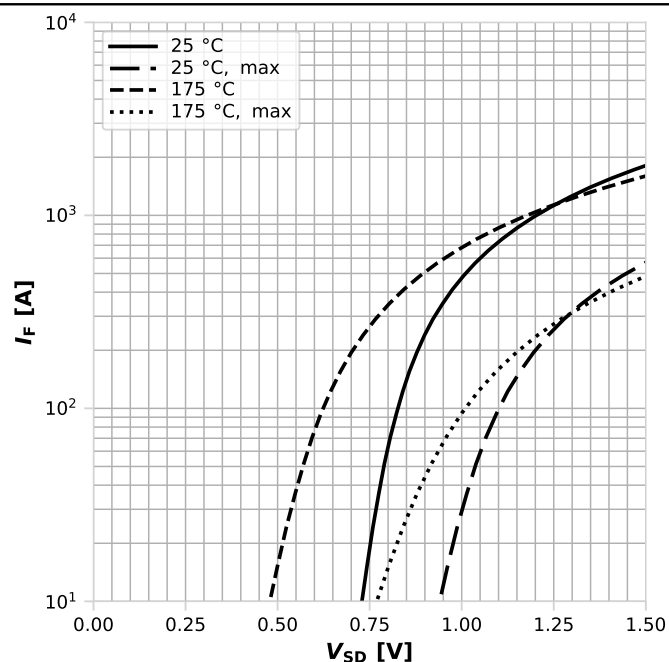
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



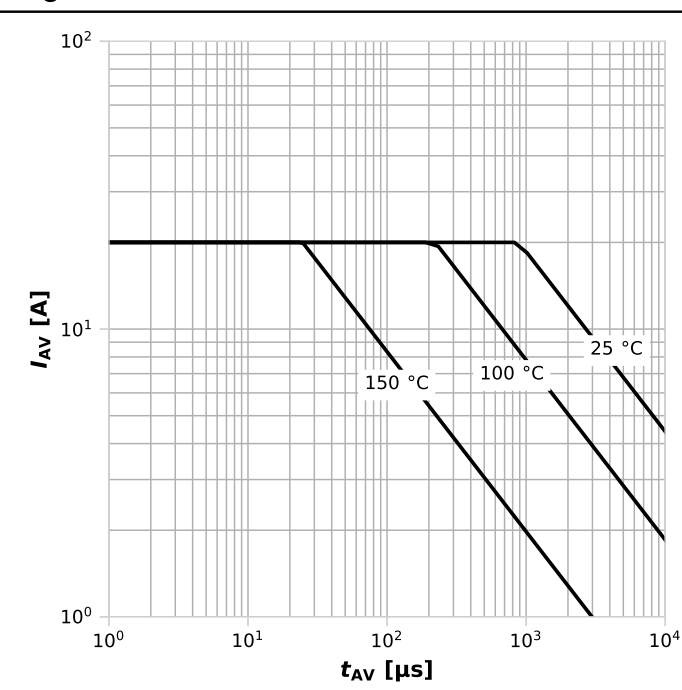
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



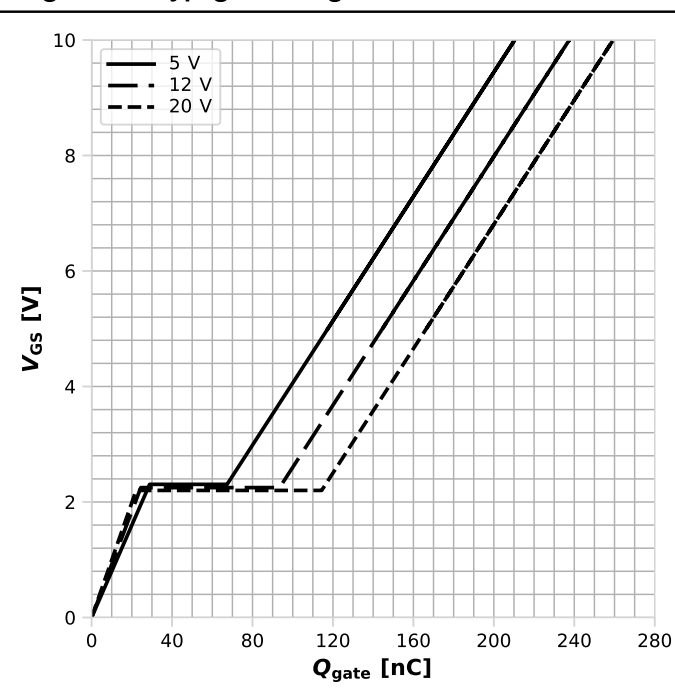
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



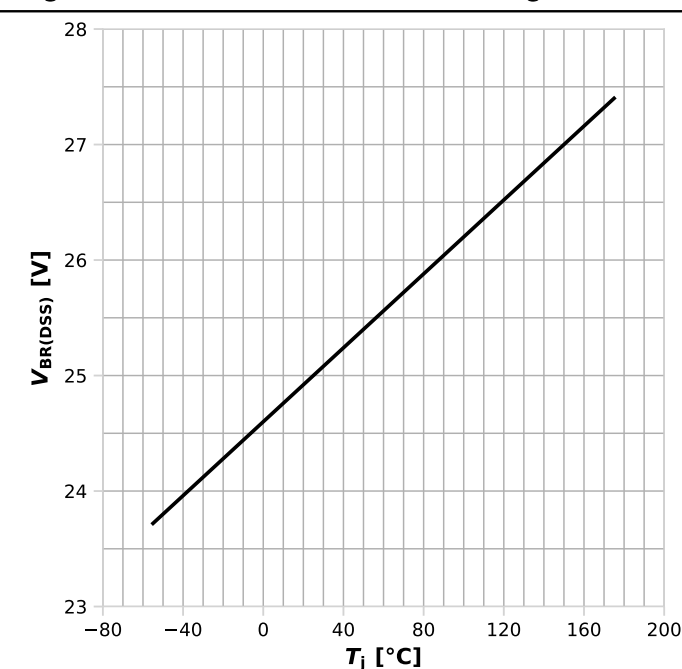
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



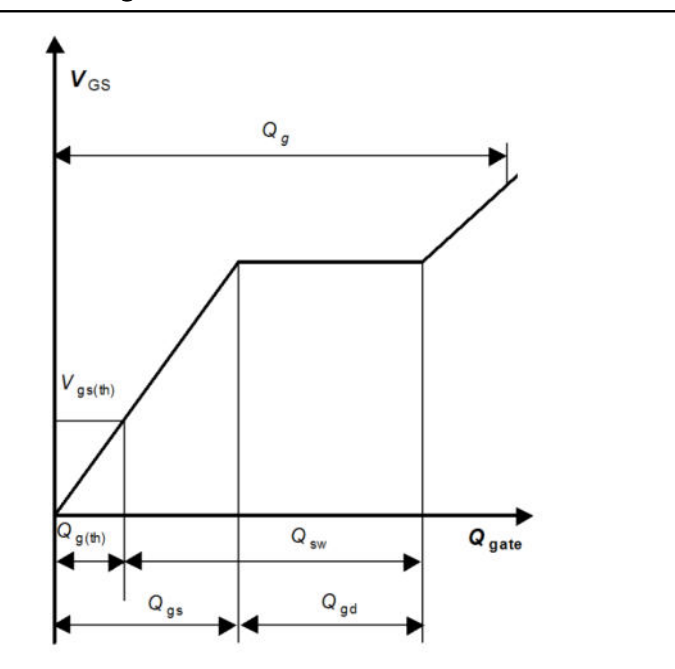
$V_{GS}=f(Q_{gate})$, $I_D=30\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



5 Package outlines

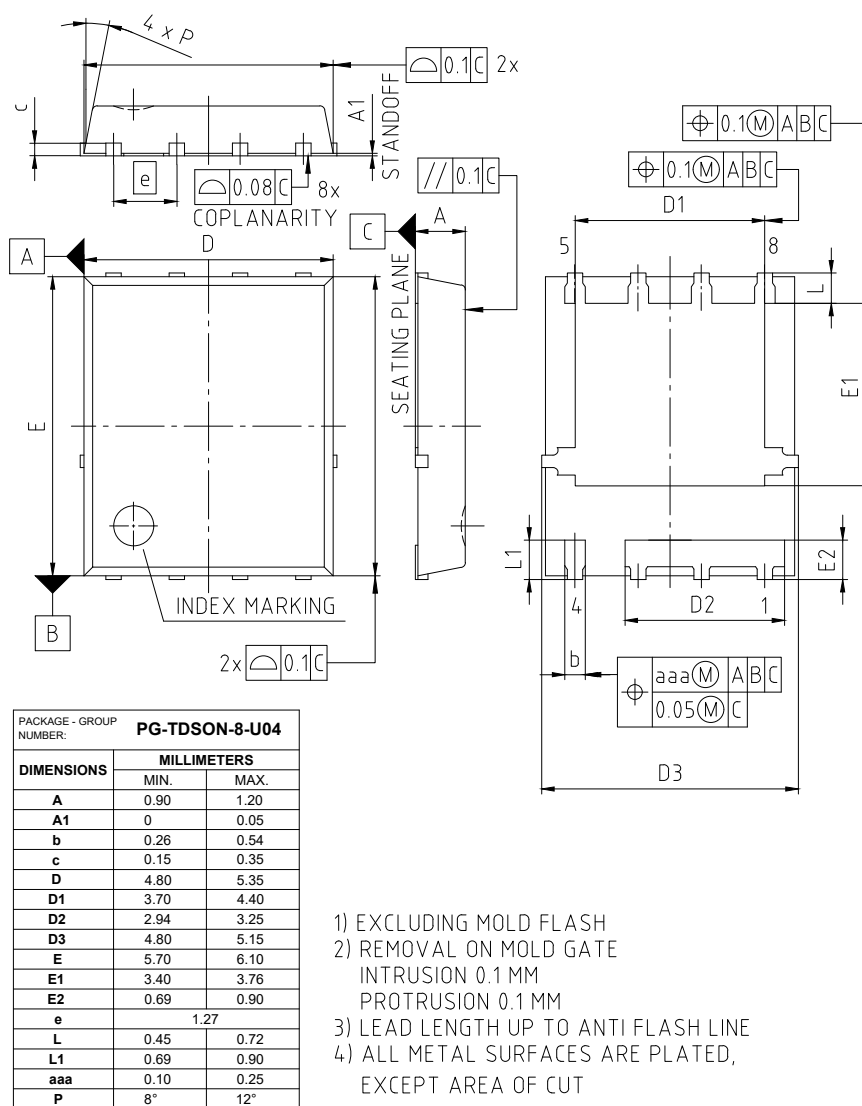


Figure 1 Outline PG-TDSON-8, dimensions in mm

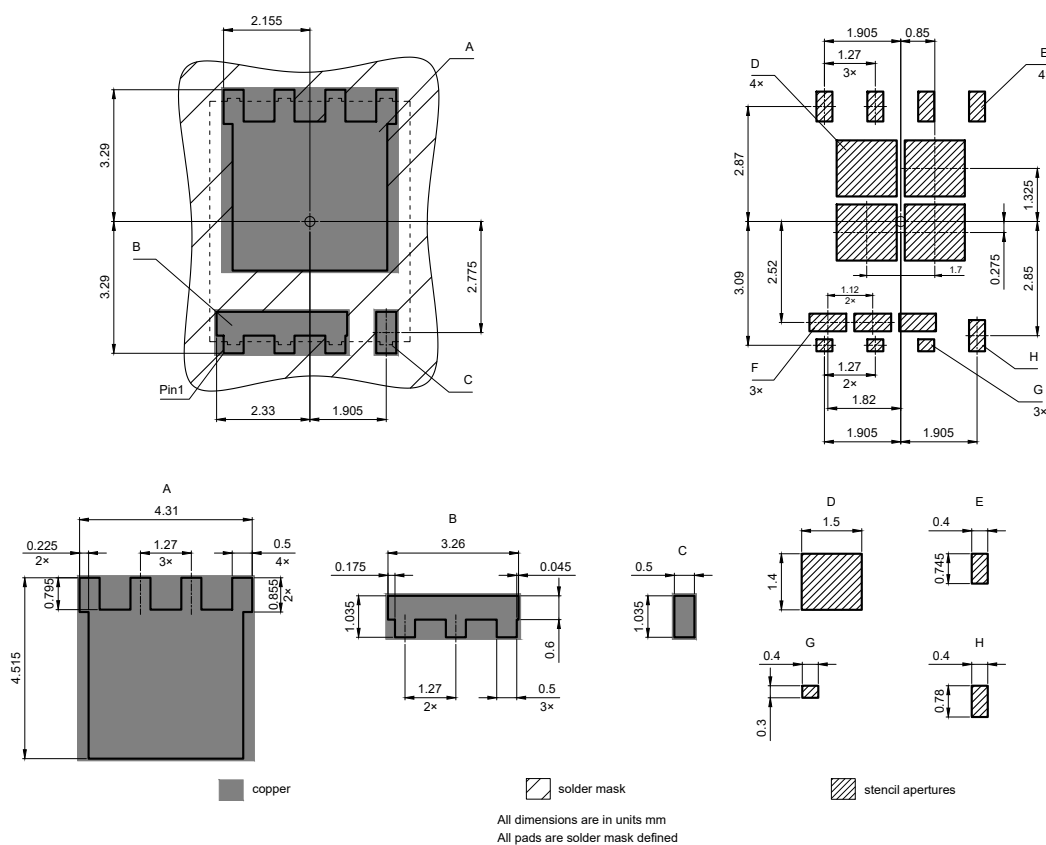


Figure 2 Footprint drawing PG-TDSON-8, dimensions in mm

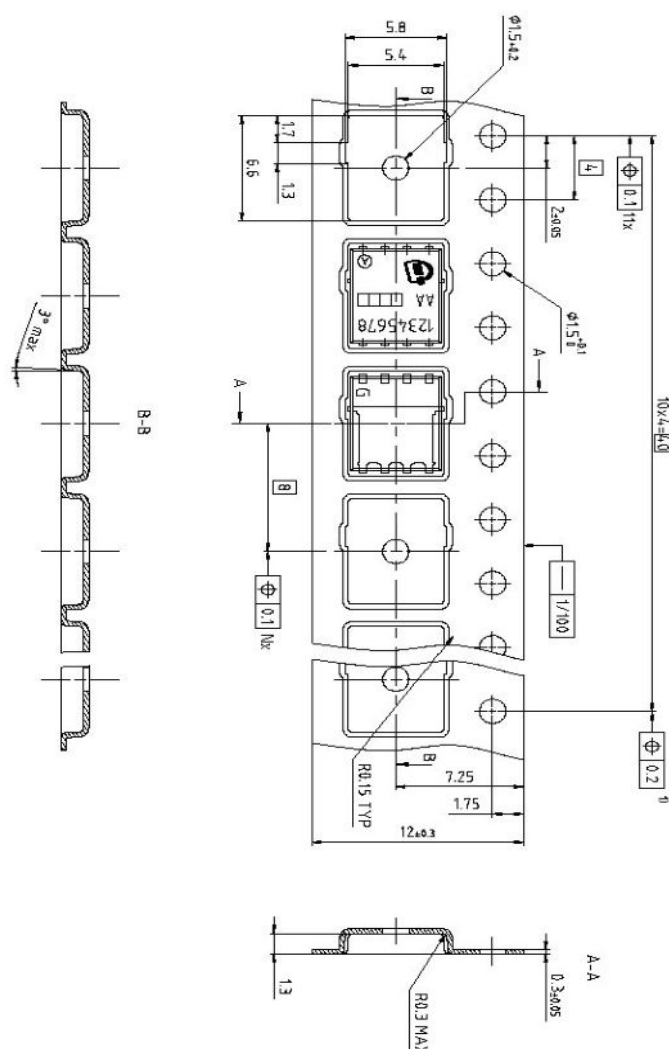


Figure 3 Packaging variant PG-TDSON-8, dimensions in mm

Revision history

BSC004NE2LS5

Revision 2024-12-10, Rev. 2.3

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2020-04-23	Release of final version
2.1	2021-03-08	Update Id condition for EAS and VGS(th)
2.2	2022-10-24	Update outline drawing
2.3	2024-12-10	Update Qrr and insert trr

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