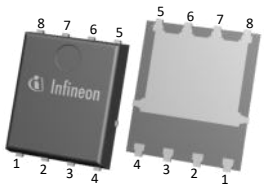
MOSFET

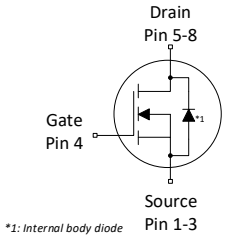
PG-TDSON-8

OptiMOS™ Power-MOSFET, 40 V



Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 175°C rated
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	1.9	mΩ
I_D	161	A
Q_{OSS}	37	nC
Q_G(0V..10V)	41	nC

Type/Ordering Code	Package	Marking	Related Links
BSC019N04LS	PG-TDSON-8	019N04LS	-

Table of Contents

1 Maximum ratings

unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	161 114 135 96 28	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	644	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	90	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage [5]	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	94 3.0	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

[5] The negative rating is for low duty cycle pulse occurrence. No continuous rating is implied

2 Thermal characteristics

at T_j=25 °C, unless otherwise specified

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.0	1.6	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm^2 cooling area [6)]	R_{thJA}	-	-	50	K/W	-

[6)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.5 1.9	1.9 2.7	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=4.5 V, I_D=50 A
Gate resistance	R_G	-	0.8	1.6	Ω	-
Transconductance	g_{fs}	95	190	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics [7)]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2900	4060	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance	C_{oss}	-	840	1180	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	68	136	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	4	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	26	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	4	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω

7) Defined by design. Not subject to production test

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	7.6	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	6.2	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	6.7	9.4	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	8.1	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	41	57	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate plateau voltage	$V_{plateau}$	-	2.6	-	V	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	21	29	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	16	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge	Q_{oss}	-	37	52	nC	V_{DD}=20 V, V_{GS}=0 V

[8)] See "gate charge waveforms" for parameter definition. Defined by design. Not subject to production test

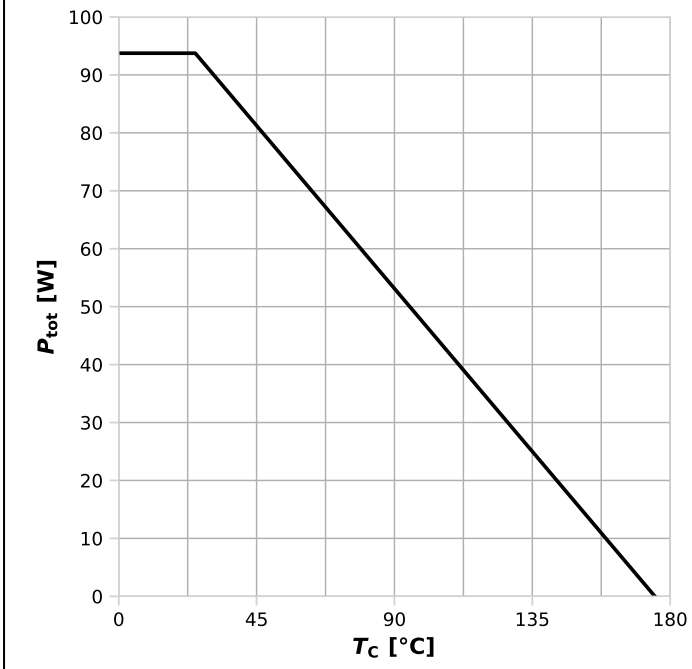
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	94	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	644	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.84	1	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	70	140	ns	V_R=20 V, I_F=50 A, di_F/dt=400 A/µs
Reverse recovery charge [9)]	Q_{rr}	-	27	-	nC	V_R=20 V, I_F=50 A, di_F/dt=400 A/µs

[9)] Defined by design. Not subject to production test

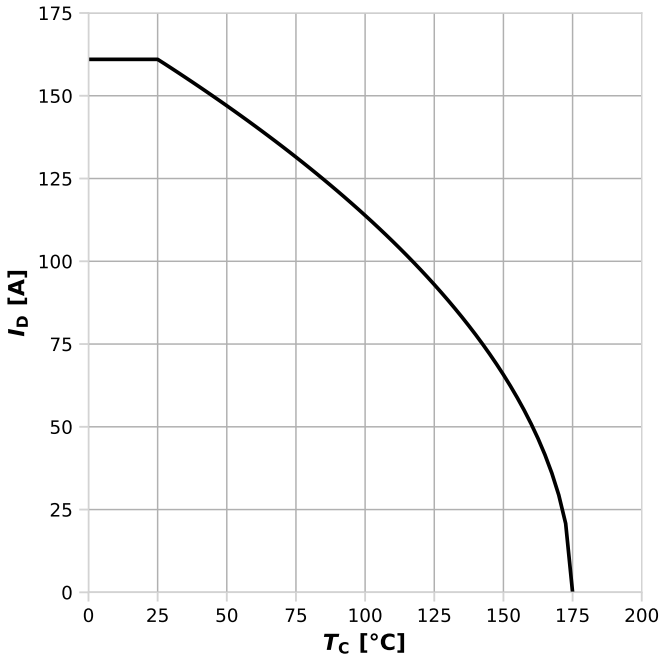
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



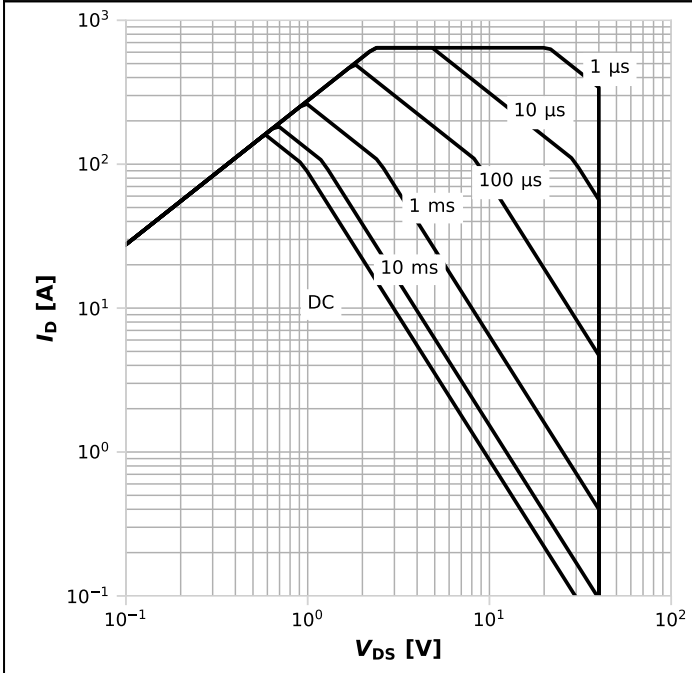
P_{tot}=f(T_C)

Diagram 2: Drain current



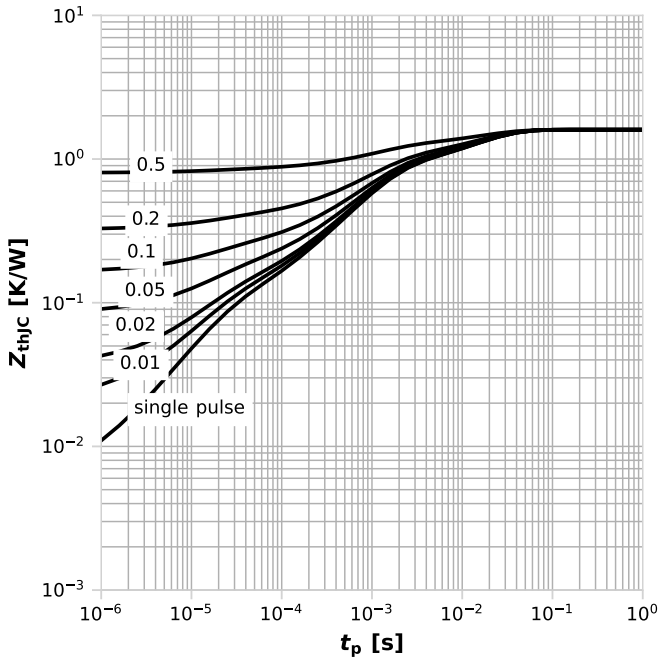
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC}=f(t_p); parameter: D=t_p/T

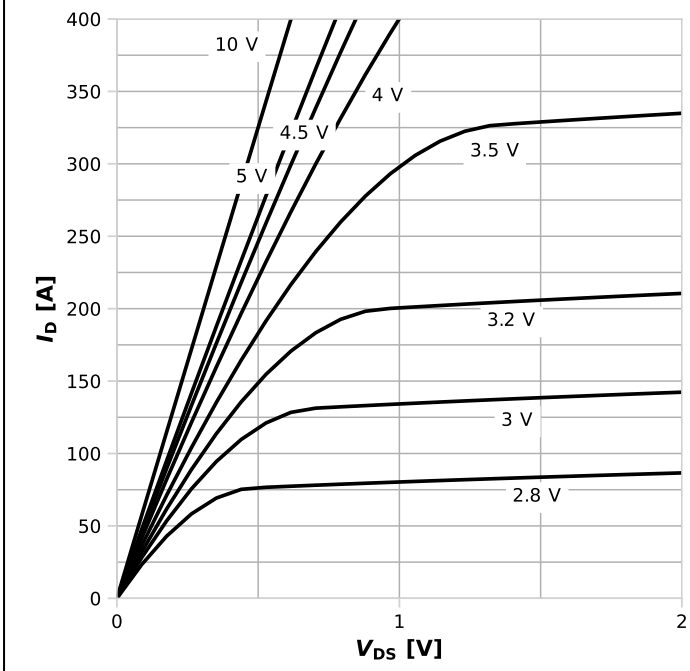
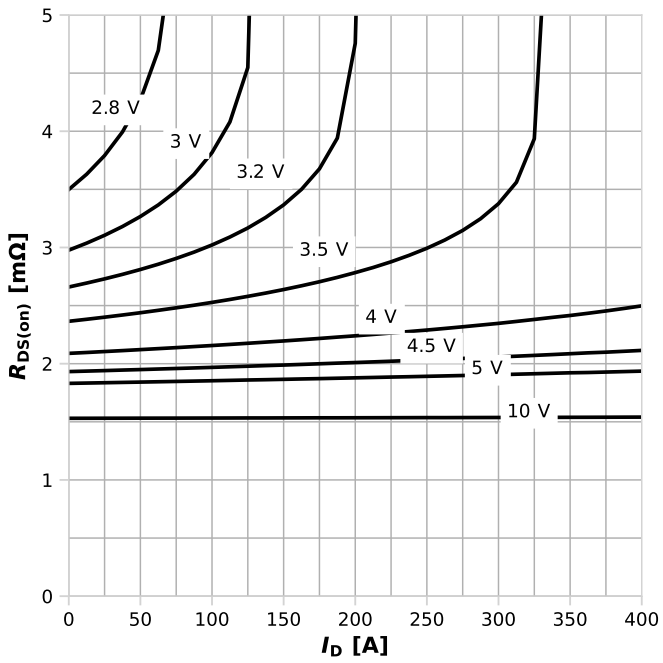
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on resistance
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

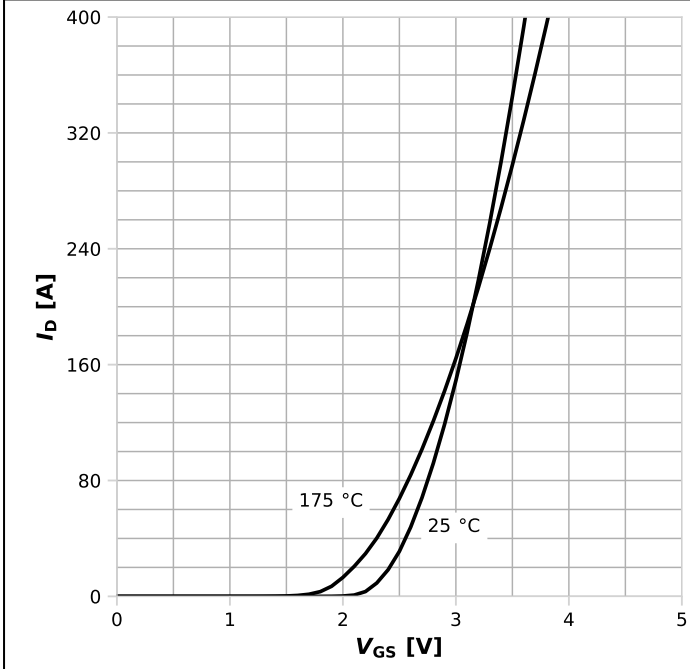
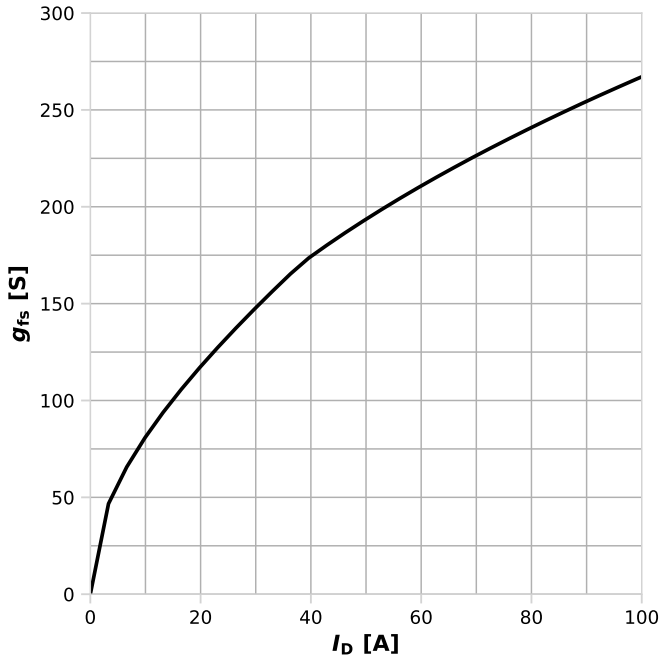
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. forward transconductance
	
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j	g_{fs}=f(I_D); T_j=25 °C

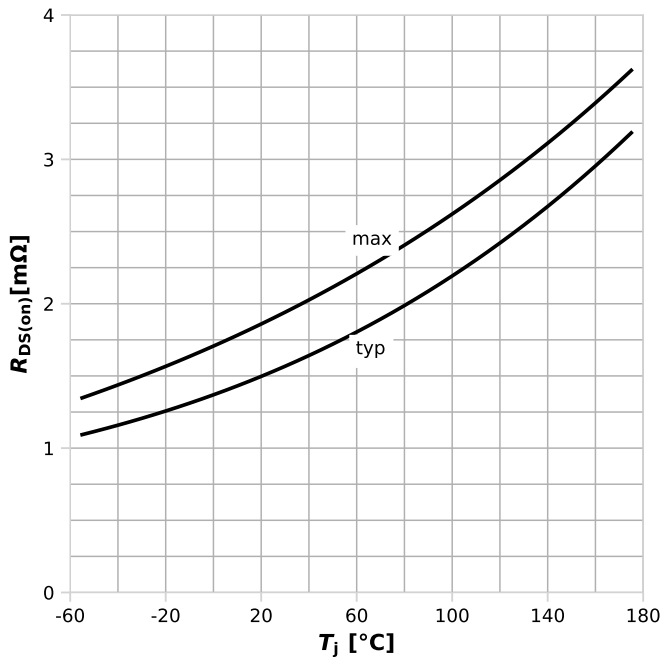
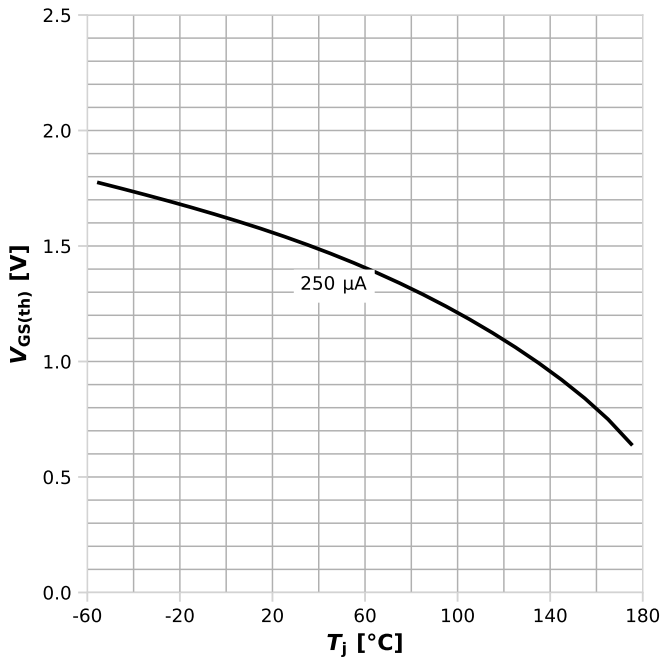
Diagram 9: Drain-source on-state resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j); I_D=50 A; V_{GS}=10 V	$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA

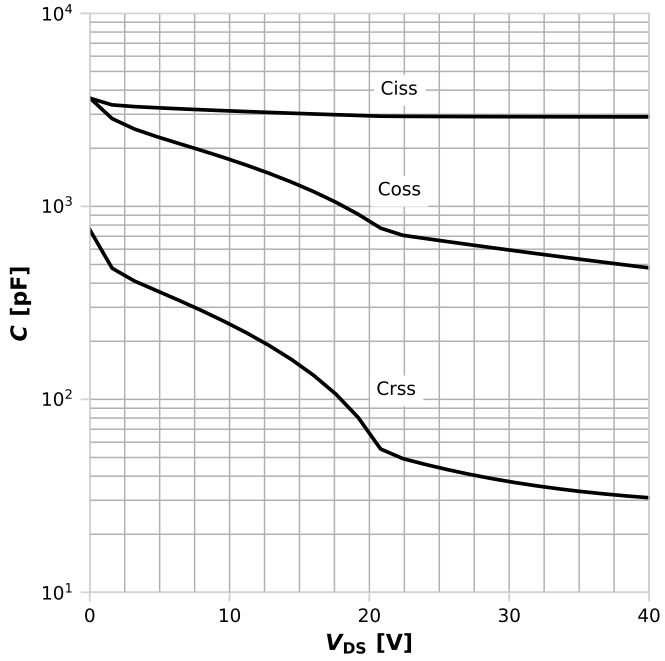
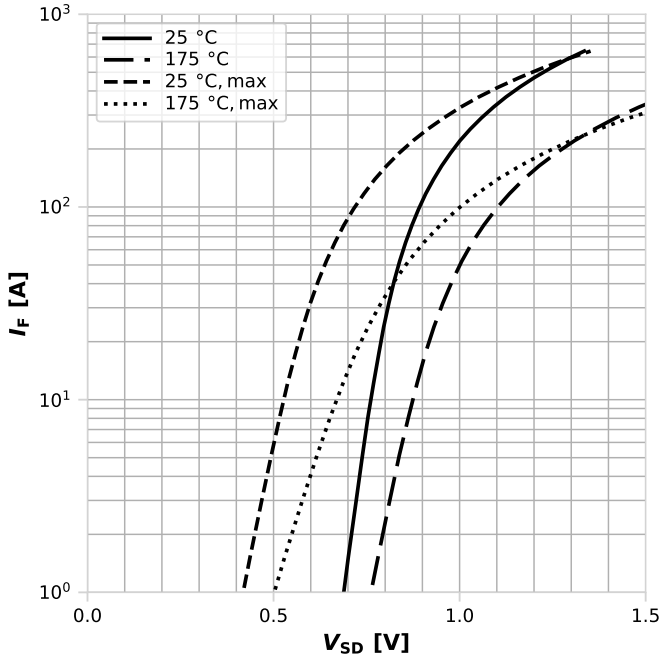
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

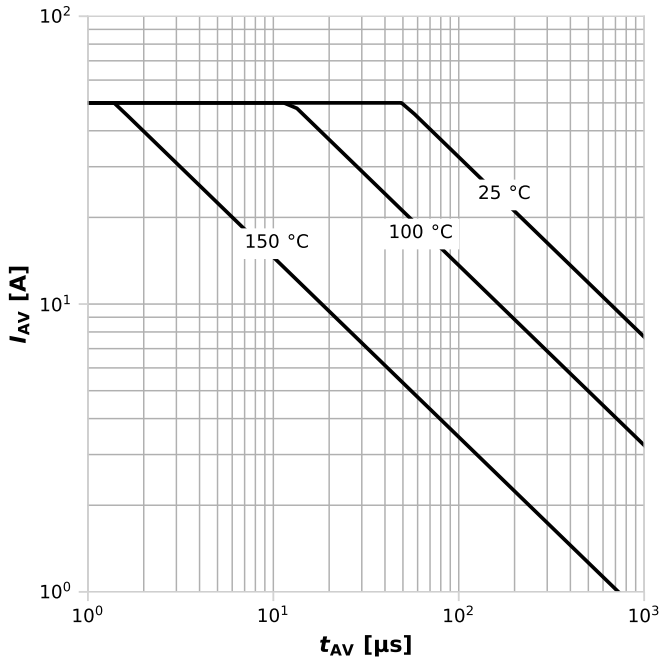
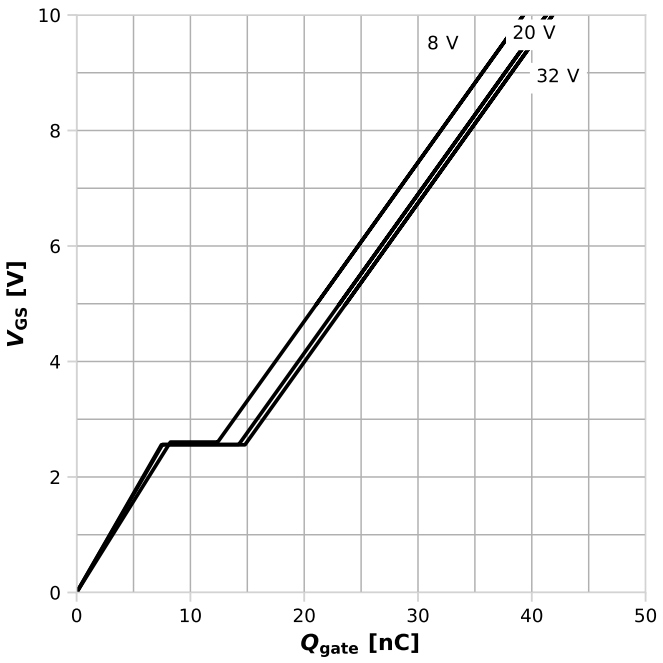
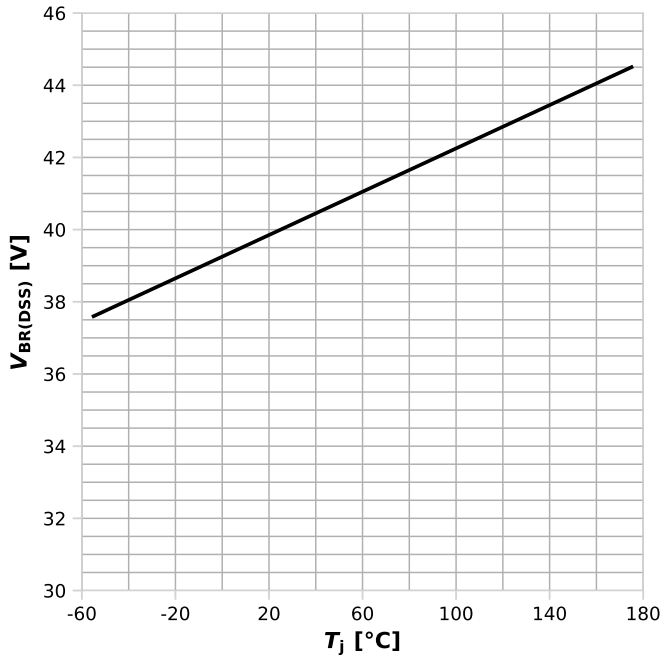
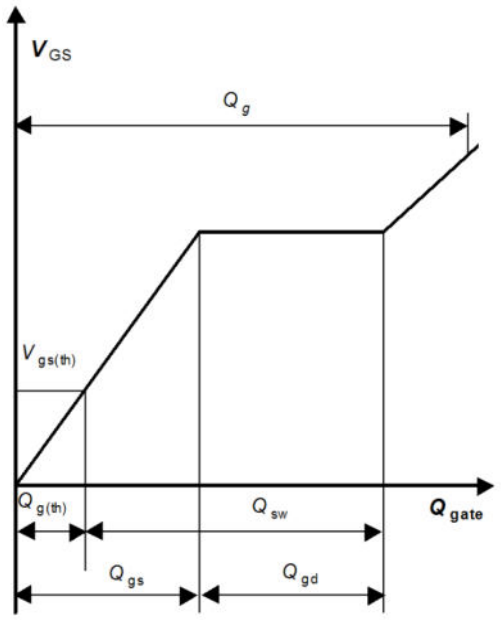
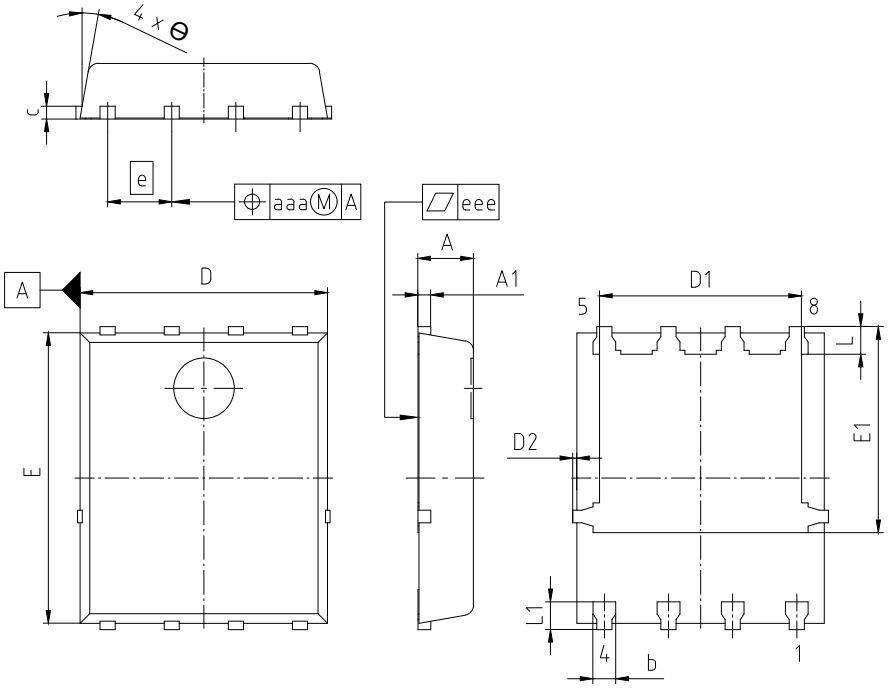
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$	V_{GS}=f(Q_{gate}); I_D=50 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TDSON-8-U08	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	4.03	4.25
e	1.27	
L	0.45	0.72
L1	0.45	0.71
aaa	0.25	
eee	0.05	
Θ	8°	12°

1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
3) ALL METAL SURFACES ARE PLATED,
EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

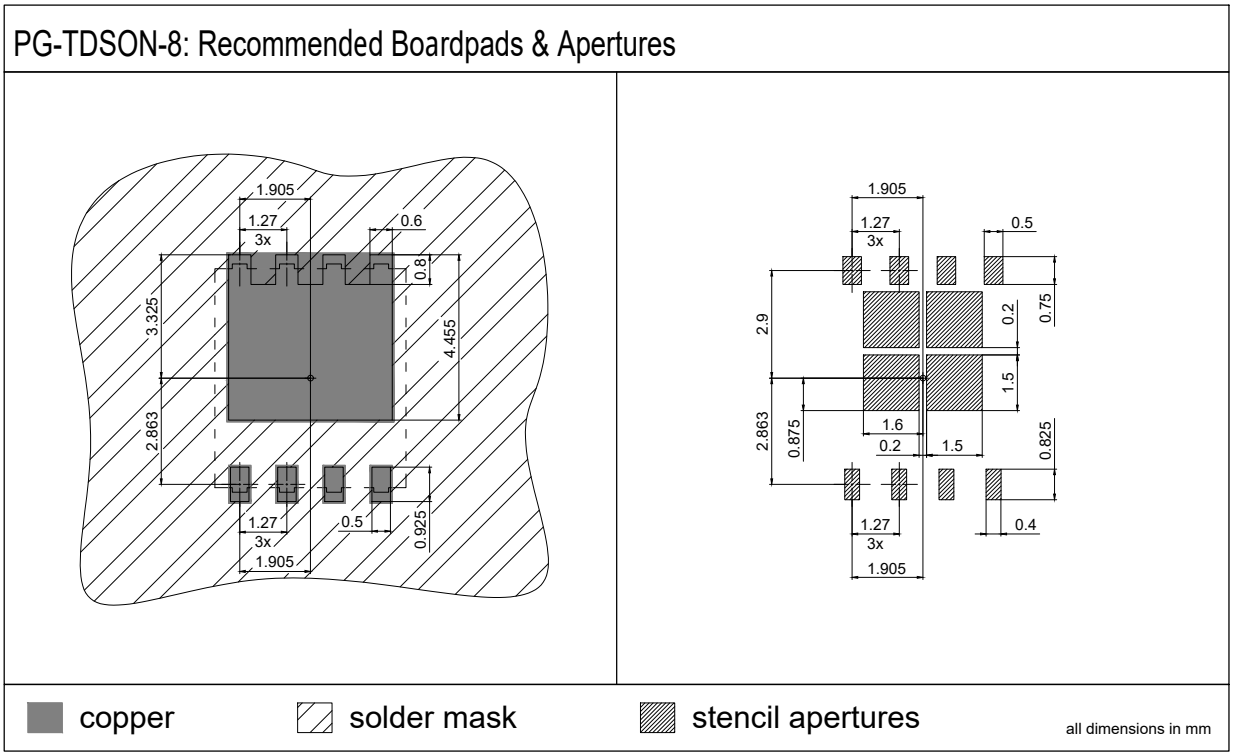
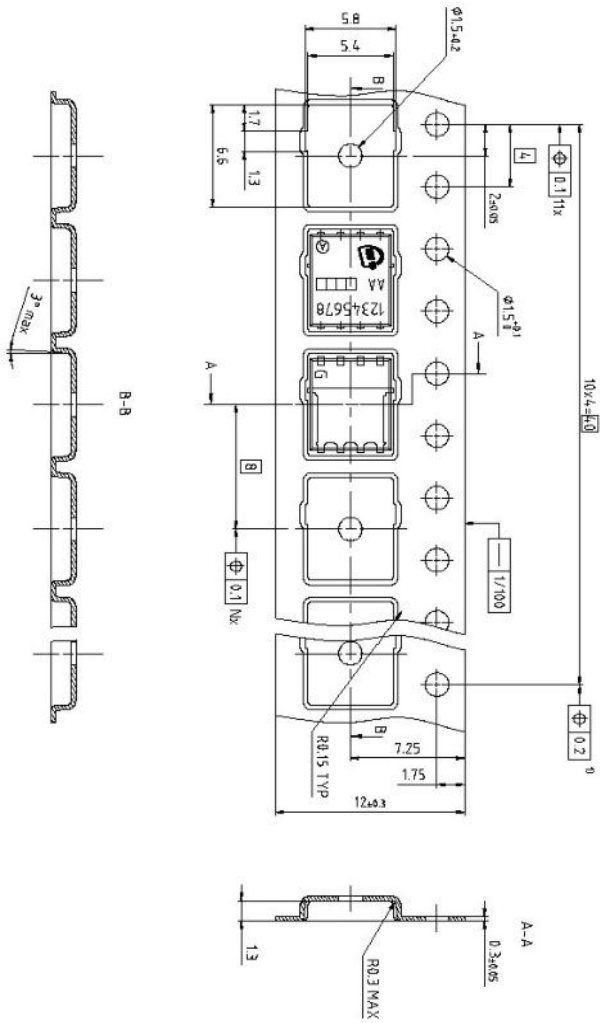


Figure 2 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 3 Outline PG-TDSON-8, dimensions in mm

Revision History

BSC019N04LS

Revision 2024-06-11, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2016-05-24	Update footnotes and insert max values
2.2	2020-02-10	Update package drawings
2.3	2021-04-27	Update current rating
2.4	2024-06-11	Upgrade Operating and storage temperature max to 175°C . Update drawings in section 5 Package Outlines. Production validation added on page1

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