

MOSFET
OptiMOS™ Power-Transistor, 60 V

Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 175°C rated
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Table with 3 columns: Parameter, Value, Unit. Rows include V\_DS (60 V), R\_DS(on),max (9.7 mΩ), I\_D (48 A), Q\_OSS (14 A), and Q\_G(0V..10V) (12 A).

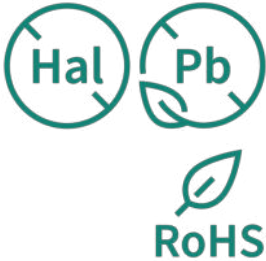
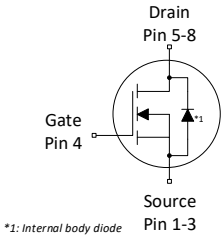


Table with 4 columns: Type/Ordering Code, Package, Marking, Related Links. Row 1: BSC097N06NS, PG-TDSON-8, 097N06NS, -



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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

| Parameter                                    | Symbol         | Values |      |                | Unit | Note/ Test Condition                                                                                                                                                         |
|----------------------------------------------|----------------|--------|------|----------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                              |                | Min.   | Typ. | Max.           |      |                                                                                                                                                                              |
| Continuous drain current <sup>1)</sup>       | $I_D$          | -      | -    | 48<br>34<br>13 | A    | $V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$<br>$V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$<br>$V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{K/W}$ <sup>2)</sup> |
| Pulsed drain current <sup>3)</sup>           | $I_{D,pulse}$  | -      | -    | 192            | A    | $T_C=25\text{ °C}$                                                                                                                                                           |
| Avalanche energy, single pulse <sup>4)</sup> | $E_{AS}$       | -      | -    | 13             | mJ   | $I_D=30\text{ A}$ , $R_{GS}=25\text{ }\Omega$                                                                                                                                |
| Gate source voltage                          | $V_{GS}$       | -20    | -    | 20             | V    | -                                                                                                                                                                            |
| Power dissipation                            | $P_{tot}$      | -      | -    | 43<br>3.0      | W    | $T_C=25\text{ °C}$<br>$T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}$ <sup>2)</sup>                                                                                            |
| Operating and storage temperature            | $T_j, T_{stg}$ | -55    | -    | 175            | °C   | -                                                                                                                                                                            |

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. Derating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter                                                   | Symbol     | Values |      |      | Unit | Note/ Test Condition |
|-------------------------------------------------------------|------------|--------|------|------|------|----------------------|
|                                                             |            | Min.   | Typ. | Max. |      |                      |
| Thermal resistance, junction - case, bottom                 | $R_{thJC}$ | -      | 2.1  | 3.5  | K/W  | -                    |
| Thermal resistance, junction - case, top                    | $R_{thJC}$ | -      | -    | 20   | K/W  | -                    |
| Device on PCB, 6 cm <sup>2</sup> cooling area <sup>5)</sup> | $R_{thJA}$ | -      | -    | 50   | K/W  | -                    |

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

| Parameter                        | Symbol        | Values |             |             | Unit          | Note/ Test Condition                                                                                                                |
|----------------------------------|---------------|--------|-------------|-------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------|
|                                  |               | Min.   | Typ.        | Max.        |               |                                                                                                                                     |
| Drain-source breakdown voltage   | $V_{(BR)DSS}$ | 60     | -           | -           | V             | $V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$                                                                                             |
| Gate threshold voltage           | $V_{GS(th)}$  | 2.1    | 2.8         | 3.3         | V             | $V_{DS}=V_{GS}$ , $I_D=14\text{ }\mu\text{A}$                                                                                       |
| Zero gate voltage drain current  | $I_{DSS}$     | -      | 0.1<br>10   | 1<br>100    | $\mu\text{A}$ | $V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$<br>$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$ |
| Gate-source leakage current      | $I_{GSS}$     | -      | 10          | 100         | nA            | $V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$                                                                                          |
| Drain-source on-state resistance | $R_{DS(on)}$  | -      | 8.0<br>12.0 | 9.7<br>14.6 | m $\Omega$    | $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$<br>$V_{GS}=6\text{ V}$ , $I_D=10\text{ A}$                                                 |
| Gate resistance <sup>6)</sup>    | $R_G$         | -      | 1.1         | 1.7         | $\Omega$      | -                                                                                                                                   |
| Transconductance                 | $g_{fs}$      | 24     | 48          | -           | S             | $ V_{DS} >2 I_D $ , $R_{DS(on)max}$ , $I_D=40\text{ A}$                                                                             |

<sup>6)</sup> Defined by design. Not subject to production test

**Table 5 Dynamic characteristics<sup>7)</sup>**

| Parameter                    | Symbol       | Values |      |      | Unit | Note/ Test Condition                                                                                   |
|------------------------------|--------------|--------|------|------|------|--------------------------------------------------------------------------------------------------------|
|                              |              | Min.   | Typ. | Max. |      |                                                                                                        |
| Input capacitance            | $C_{iss}$    | -      | 860  | 1075 | pF   | $V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$                                          |
| Output capacitance           | $C_{oss}$    | -      | 210  | 263  | pF   | $V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$                                          |
| Reverse transfer capacitance | $C_{rss}$    | -      | 16   | 32   | pF   | $V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$                                          |
| Turn-on delay time           | $t_{d(on)}$  | -      | 6    | -    | ns   | $V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ ,<br>$R_{G,ext,ext}=1.6\text{ }\Omega$ |
| Rise time                    | $t_r$        | -      | 2    | -    | ns   | $V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ ,<br>$R_{G,ext,ext}=1.6\text{ }\Omega$ |
| Turn-off delay time          | $t_{d(off)}$ | -      | 10   | -    | ns   | $V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ ,<br>$R_{G,ext,ext}=1.6\text{ }\Omega$ |
| Fall time                    | $t_f$        | -      | 2    | -    | ns   | $V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ ,<br>$R_{G,ext,ext}=1.6\text{ }\Omega$ |

<sup>7)</sup> Defined by design. Not subject to production test

**Table 6 Gate charge characteristics<sup>8)</sup>**

| Parameter                | Symbol      | Values |      |      | Unit | Note/ Test Condition                                                        |
|--------------------------|-------------|--------|------|------|------|-----------------------------------------------------------------------------|
|                          |             | Min.   | Typ. | Max. |      |                                                                             |
| Gate to source charge    | $Q_{gs}$    | -      | 4.5  | -    | nC   | $V_{DD}=30\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge at threshold | $Q_{g(th)}$ | -      | 2.4  | -    | nC   | $V_{DD}=30\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate to drain charge     | $Q_{gd}$    | -      | 2.6  | 3.7  | nC   | $V_{DD}=30\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$ |

**Table 6 Gate charge characteristics** <sup>8)</sup>

| Parameter                    | Symbol        | Values |      |      | Unit | Note/ Test Condition                                                        |
|------------------------------|---------------|--------|------|------|------|-----------------------------------------------------------------------------|
|                              |               | Min.   | Typ. | Max. |      |                                                                             |
| Switching charge             | $Q_{sw}$      | -      | 4.7  | -    | nC   | $V_{DD}=30\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total            | $Q_g$         | -      | 12   | 15   | nC   | $V_{DD}=30\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate plateau voltage         | $V_{plateau}$ | -      | 5.2  | -    | V    | $V_{DD}=30\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | -      | 10   | -    | nC   | $V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$                    |
| Output charge                | $Q_{oss}$     | -      | 14   | 19   | nC   | $V_{DD}=30\text{ V}$ , $V_{GS}=0\text{ V}$                                  |

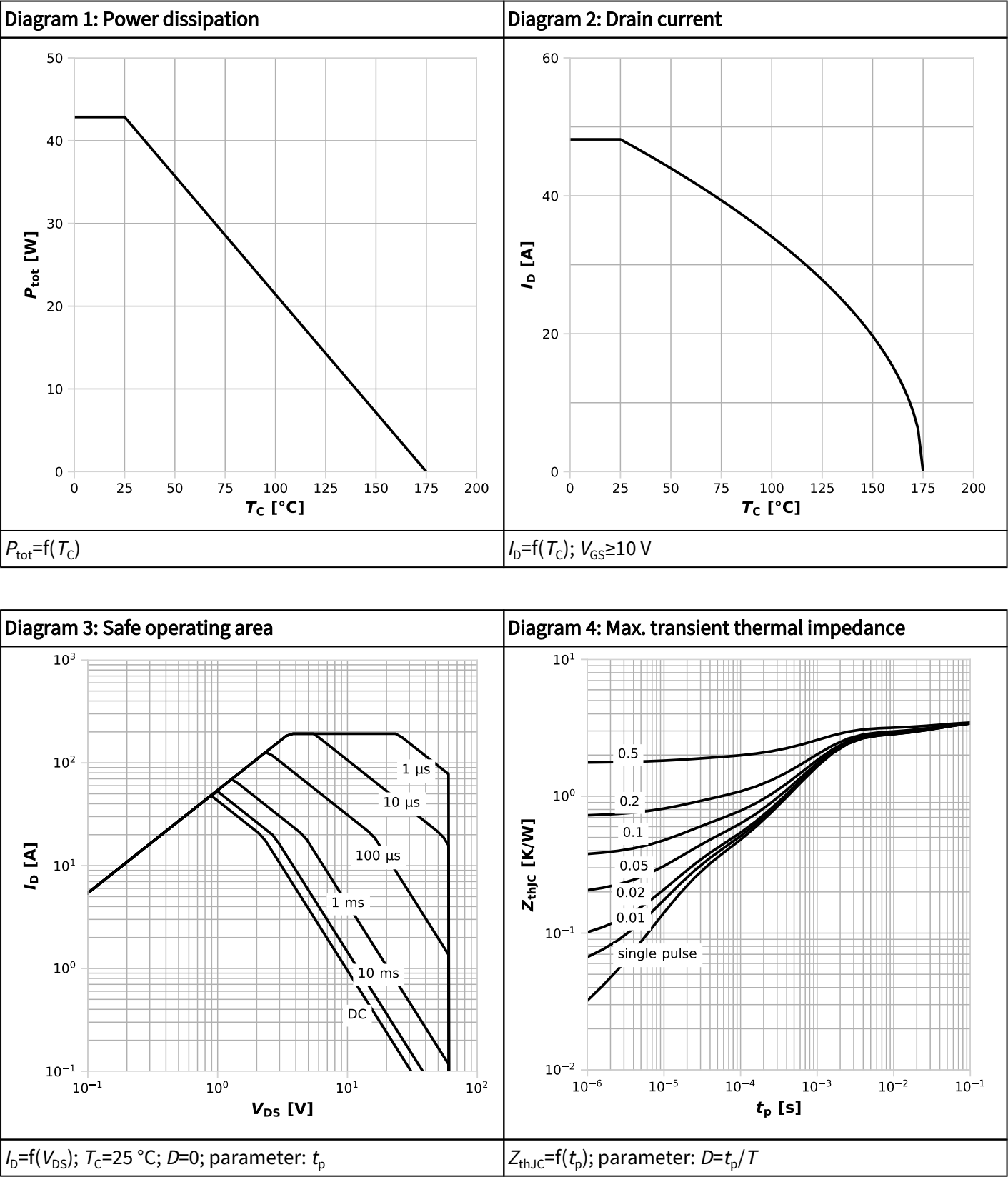
<sup>8)</sup> Defined by design. Not subject to production test. See figure 16 for gate charge parameter definition

**Table 7 Reverse diode**

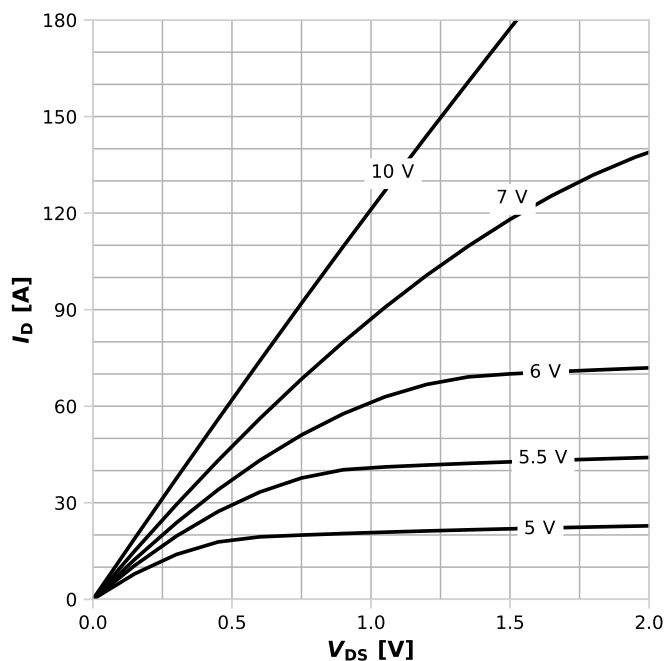
| Parameter                             | Symbol        | Values |      |      | Unit | Note/ Test Condition                                                       |
|---------------------------------------|---------------|--------|------|------|------|----------------------------------------------------------------------------|
|                                       |               | Min.   | Typ. | Max. |      |                                                                            |
| Diode continuous forward current      | $I_S$         | -      | -    | 36   | A    | $T_C=25\text{ °C}$                                                         |
| Diode pulse current                   | $I_{S,pulse}$ | -      | -    | 192  | A    | $T_C=25\text{ °C}$                                                         |
| Diode forward voltage                 | $V_{SD}$      | -      | 1.0  | 1.2  | V    | $V_{GS}=0\text{ V}$ , $I_F=30\text{ A}$ , $T_J=25\text{ °C}$               |
| Reverse recovery time <sup>9)</sup>   | $t_{rr}$      | -      | 33   | 53   | ns   | $V_R=30\text{ V}$ , $I_F=30\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$ |
| Reverse recovery charge <sup>9)</sup> | $Q_{rr}$      | -      | 30   | -    | nC   | $V_R=30\text{ V}$ , $I_F=30\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$ |

<sup>9)</sup> Defined by design. Not subject to production test

4 Electrical characteristics diagrams

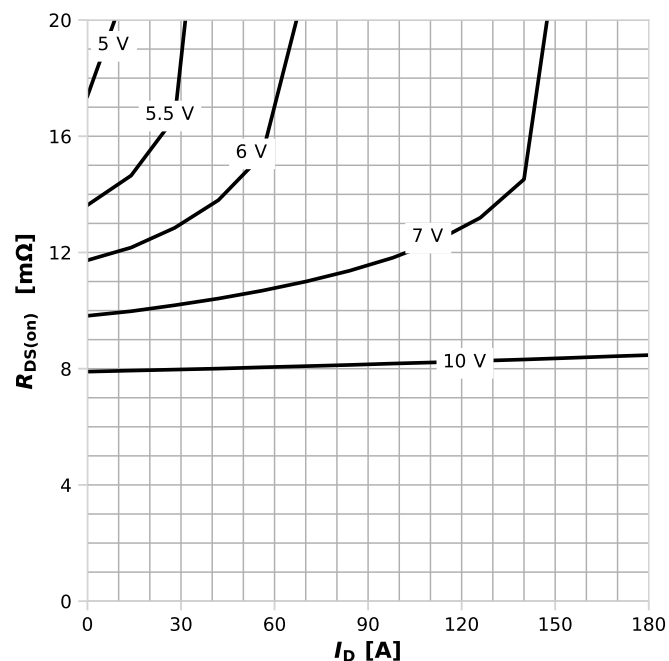


**Diagram 5: Typ. output characteristics**



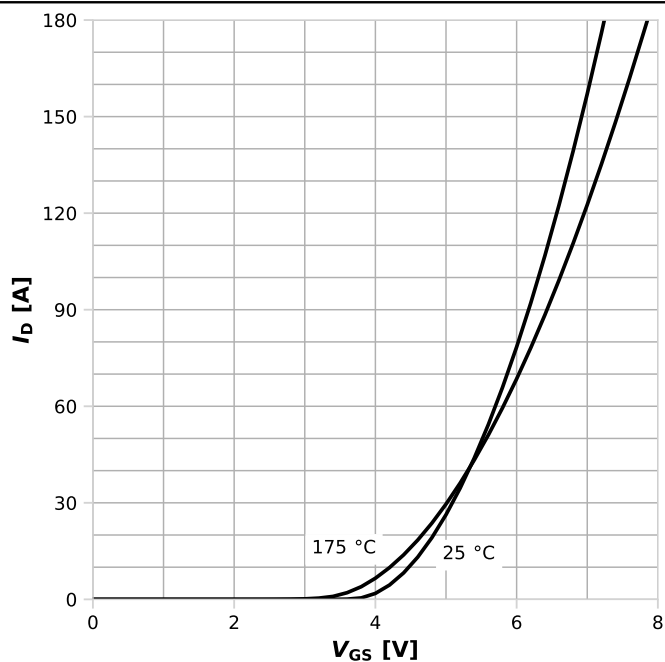
$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



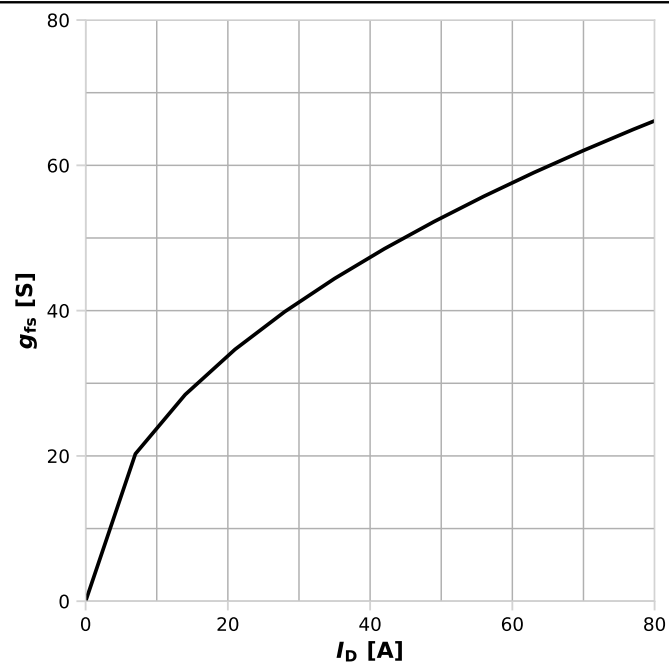
$R_{DS(on)} = f(I_D)$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



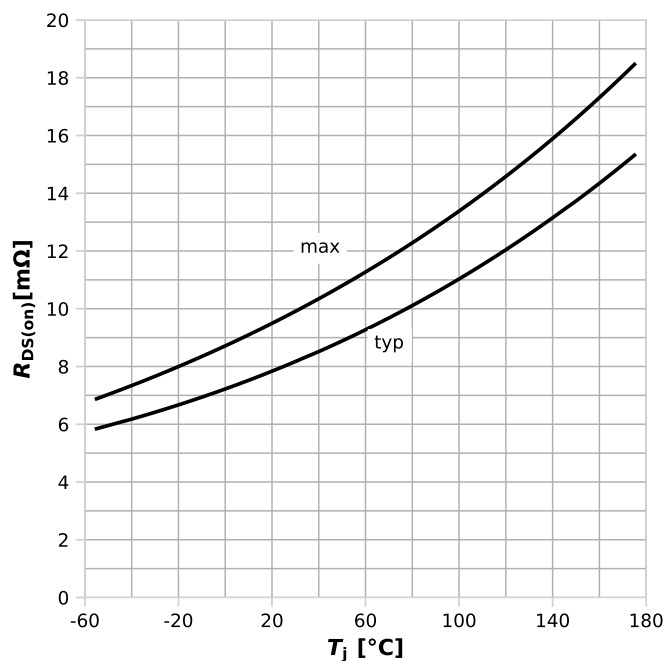
$I_D = f(V_{GS})$ ;  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

**Diagram 8: Typ. forward transconductance**



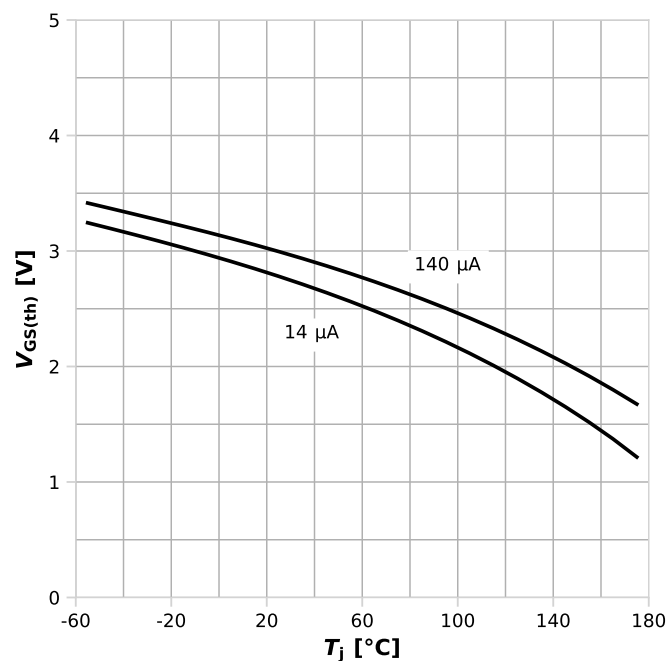
$g_{fs} = f(I_D)$ ;  $T_j = 25^\circ\text{C}$

**Diagram 9: Drain-source on-state resistance**



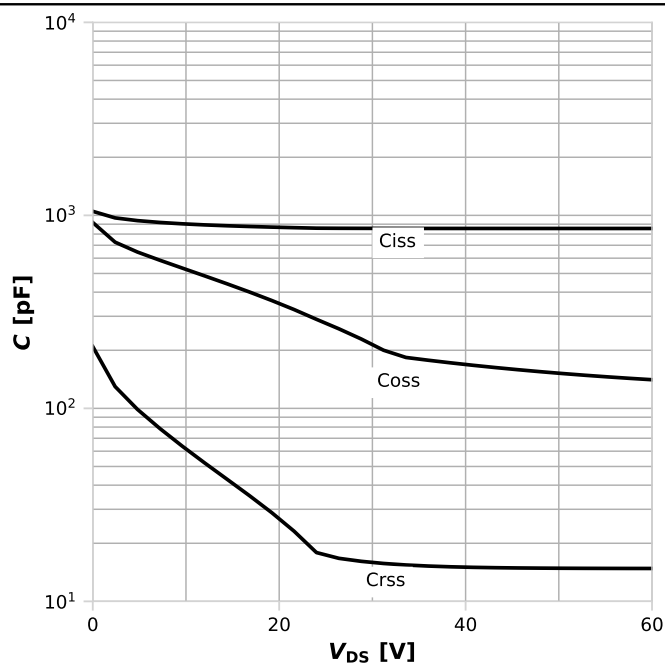
$$R_{DS(on)} = f(T_j); I_D = 40 \text{ A}; V_{GS} = 10 \text{ V}$$

**Diagram 10: Typ. gate threshold voltage**



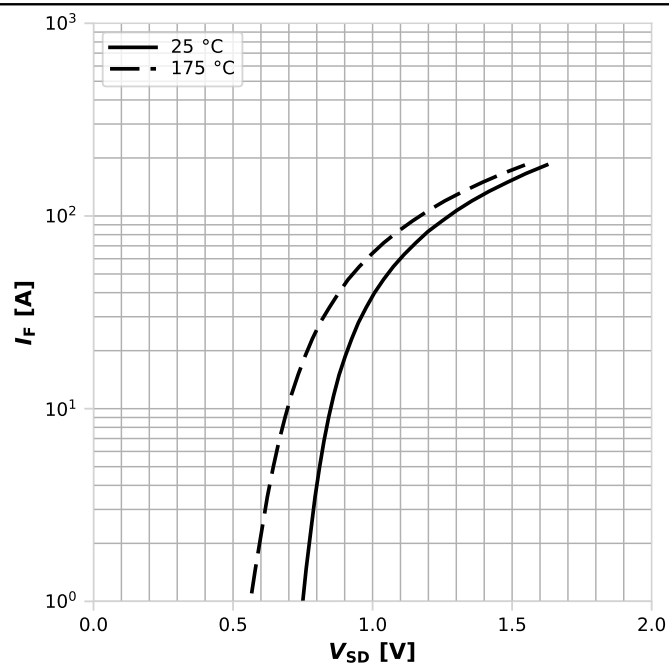
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

**Diagram 11: Typ. capacitances**



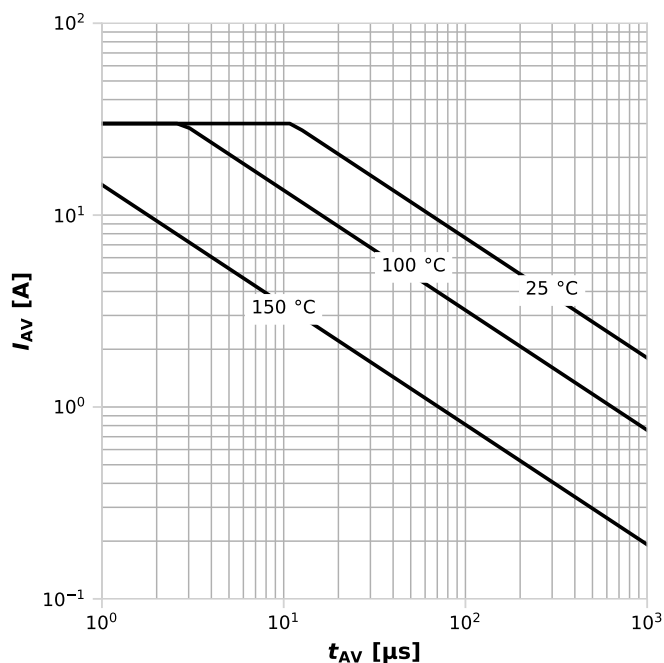
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

**Diagram 12: Forward characteristics of reverse diode**



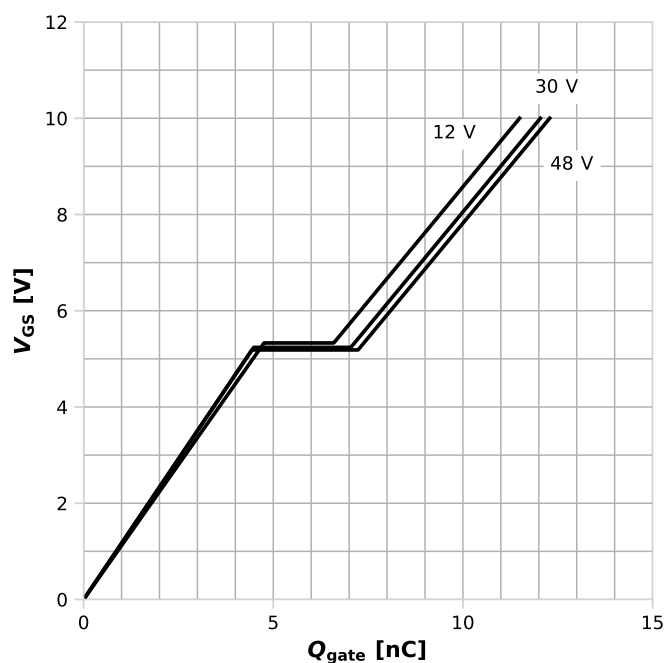
$$I_F = f(V_{SD}); \text{parameter: } T_j$$

Diagram 13: Avalanche characteristics



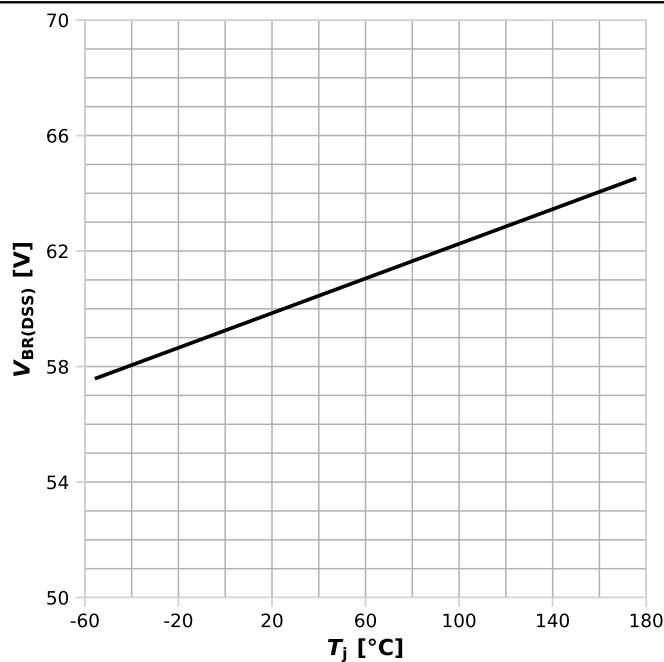
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25\ \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



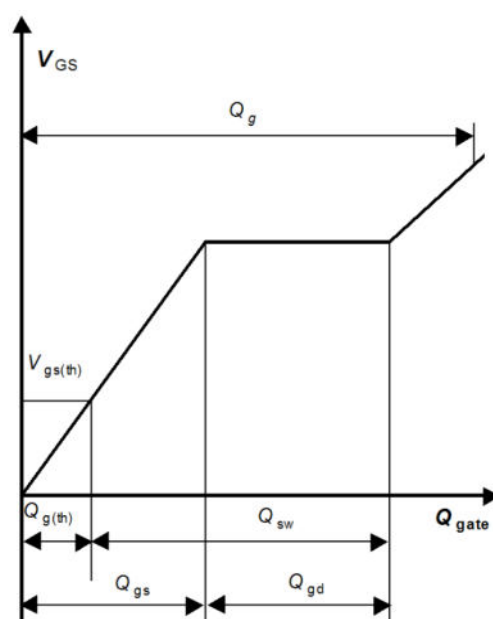
$V_{GS}=f(Q_{gate})$ ;  $I_D=40\text{ A}$  pulsed; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$ ;  $I_D=1\text{ mA}$

Gate charge waveforms



-

5 Package Outlines

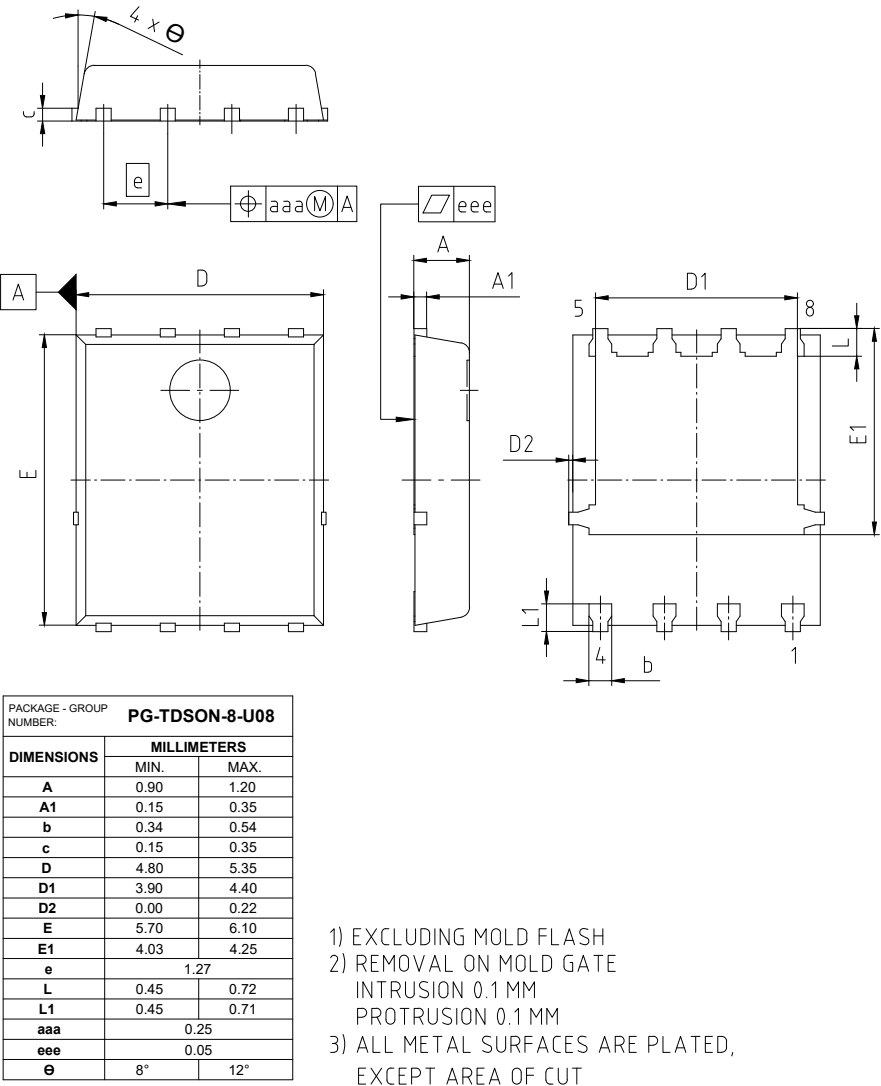


Figure 1 Outline PG-TDSON-8, dimensions in mm

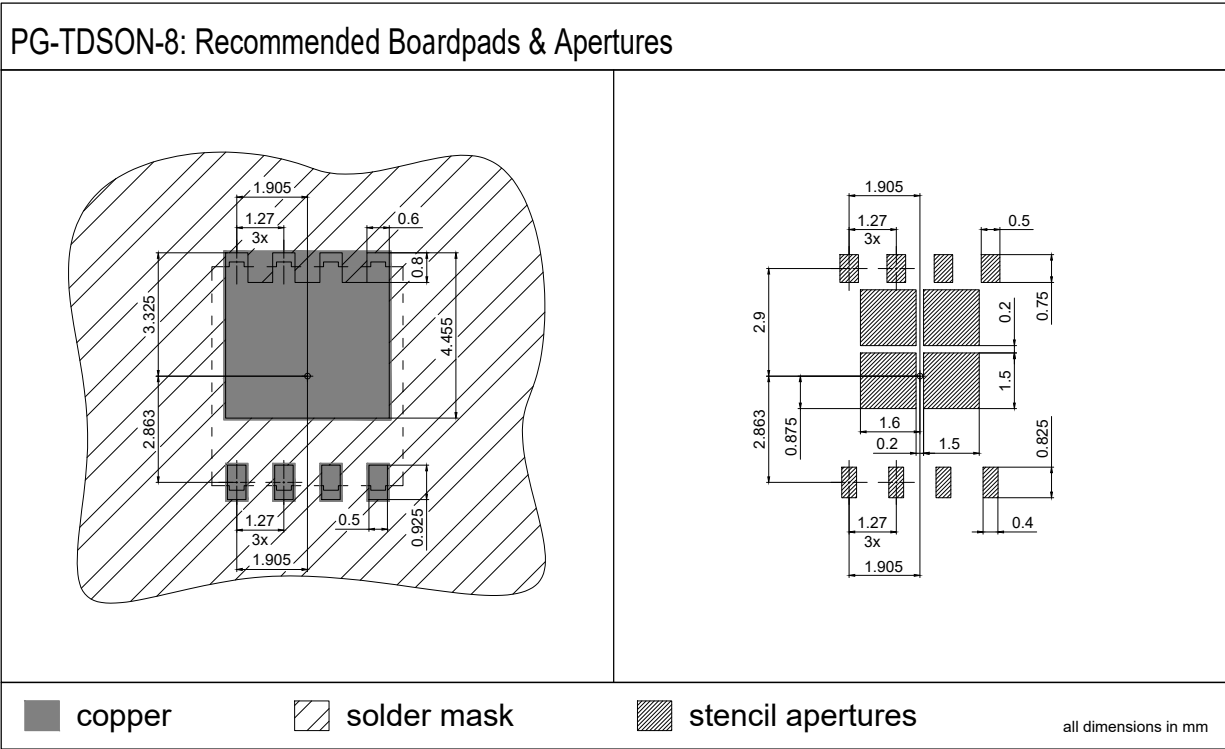
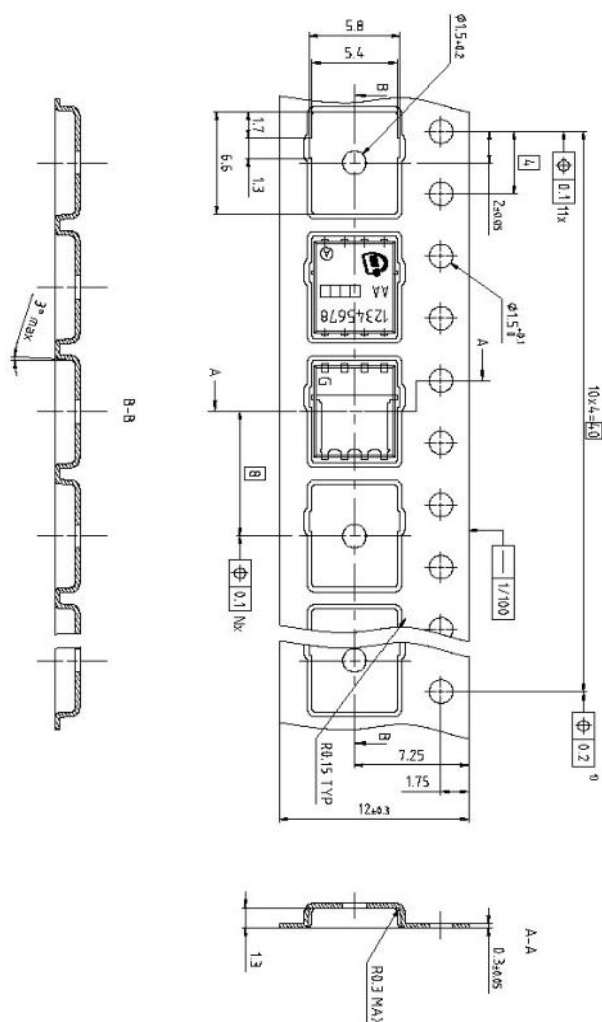


Figure 2 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 3 Outline PG-TDSON-8, dimensions in mm

## Revision History

BSC097N06NS

### Revision 2024-06-12, Rev. 2.3

Previous Revision

| Revision | Date       | Subjects (major changes since last revision)                                                                                                                                |
|----------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2.2      | 2019-11-15 | Update package drawings and footnotes, addition RthJC_typ and Qoss_max                                                                                                      |
| 2.3      | 2024-06-12 | Upgrade Operating and storage temperature max to 175°C . Update drawings in section 5 Package Outlines. Production validation added on page1. Add footnote to Id on page 1. |

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