



IAUC100N08S5N034

## OptiMOS™ -5 Power Transistor



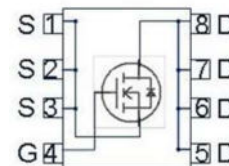
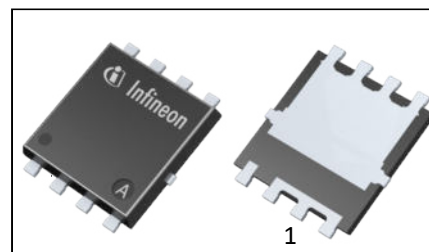
### Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- MSL1 up to 260°C peak reflow
- 175 °C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

### Product Summary

|                  |     |    |
|------------------|-----|----|
| $V_{DS}$         | 80  | V  |
| $R_{DS(on),max}$ | 3.4 | mΩ |
| $I_D$            | 100 | A  |

### PG-TDSON-8-34



| Type             | Package                       | Marking |
|------------------|-------------------------------|---------|
| IAUC100N08S5N034 | <a href="#">PG-TDSON-8-34</a> | 5N08034 |

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified

| Parameter                                    | Symbol         | Conditions                                                                     | Value        | Unit |
|----------------------------------------------|----------------|--------------------------------------------------------------------------------|--------------|------|
| Drain current                                | $I_D$          | $V_{GS}=10\text{ V}$ , Chip limitation <sup>1,2)</sup>                         | 132          | A    |
|                                              |                | $V_{GS}=10\text{ V}$ , DC current <sup>3)</sup>                                | 100          |      |
|                                              |                | $T_a=85\text{ °C}$ , $V_{GS}=10\text{ V}$ , $R_{thJA}$ on 2s2p <sup>2,4)</sup> | 22           |      |
| Pulsed drain current <sup>2)</sup>           | $I_{D,pulse}$  | $T_C=25\text{ °C}$                                                             | 400          |      |
| Avalanche energy, single pulse <sup>2)</sup> | $E_{AS}$       | $I_D=50\text{ A}$                                                              | 240          | mJ   |
| Avalanche current, single pulse              | $I_{AS}$       | -                                                                              | 100          | A    |
| Gate source voltage                          | $V_{GS}$       | -                                                                              | ±20          | V    |
| Power dissipation                            | $P_{tot}$      | $T_C=25\text{ °C}$                                                             | 136          | W    |
| Operating and storage temperature            | $T_j, T_{stg}$ | -                                                                              | -55 ... +175 | °C   |

| Parameter | Symbol | Conditions | Values |      |      | Unit |
|-----------|--------|------------|--------|------|------|------|
|           |        |            | min.   | typ. | max. |      |

### Thermal characteristics<sup>2)</sup>

|                                                      |            |   |   |      |     |     |
|------------------------------------------------------|------------|---|---|------|-----|-----|
| Thermal resistance, junction - case                  | $R_{thJC}$ | - | - | -    | 1.1 | K/W |
| Thermal resistance, junction - ambient <sup>4)</sup> | $R_{thJA}$ | - | - | 23.5 | -   |     |

### Electrical characteristics, at $T_j=25^\circ\text{C}$ , unless otherwise specified

#### Static characteristics

|                                  |               |                                                    |     |     |     |            |
|----------------------------------|---------------|----------------------------------------------------|-----|-----|-----|------------|
| Drain-source breakdown voltage   | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=1mA$                               | 80  | -   | -   | V          |
| Gate threshold voltage           | $V_{GS(th)}$  | $V_{DS}=V_{GS}, I_D=78\mu A$                       | 2.2 | 3.0 | 3.8 |            |
| Zero gate voltage drain current  | $I_{DSS}$     | $V_{DS}=80V, V_{GS}=0V, T_j=25^\circ\text{C}$      | -   | 0.1 | 1   | $\mu A$    |
|                                  |               | $V_{DS}=80V, V_{GS}=0V, T_j=85^\circ\text{C}^{2)}$ | -   | 1   | 20  |            |
| Gate-source leakage current      | $I_{GSS}$     | $V_{GS}=20V, V_{DS}=0V$                            | -   | -   | 100 | nA         |
| Drain-source on-state resistance | $R_{DS(on)}$  | $V_{GS}=6V, I_D=25A$                               | -   | 3.9 | 4.8 | m $\Omega$ |
|                                  |               | $V_{GS}=10V, I_D=50A$                              | -   | 2.8 | 3.4 |            |
| Gate resistance <sup>2)</sup>    | $R_G$         | -                                                  | -   | 1.5 | -   | $\Omega$   |



| Parameter | Symbol | Conditions | Values |      |      | Unit |
|-----------|--------|------------|--------|------|------|------|
|           |        |            | min.   | typ. | max. |      |

**Dynamic characteristics<sup>2)</sup>**

|                              |              |                                                             |   |      |      |    |
|------------------------------|--------------|-------------------------------------------------------------|---|------|------|----|
| Input capacitance            | $C_{iss}$    | $V_{GS}=0V, V_{DS}=40V,$<br>$f=1MHz$                        | - | 3507 | 4559 | pF |
| Output capacitance           | $C_{oss}$    |                                                             | - | 620  | 806  |    |
| Reverse transfer capacitance | $C_{rss}$    |                                                             | - | 27   | 41   |    |
| Turn-on delay time           | $t_{d(on)}$  | $V_{DD}=40V, V_{GS}=10V,$<br>$I_D=50A, R_{G,ext}=3.5\Omega$ | - | 10   | -    | ns |
| Turn-off delay time          | $t_{d(off)}$ |                                                             | - | 18   | -    |    |
| Rise time                    | $t_r$        |                                                             | - | 6    | -    |    |
| Fall time                    | $t_f$        |                                                             | - | 12   | -    |    |

**Gate Charge Characteristics<sup>2)</sup>**

|                       |               |                                                      |   |     |    |    |
|-----------------------|---------------|------------------------------------------------------|---|-----|----|----|
| Gate to source charge | $Q_{gs}$      | $V_{DD}=40V, I_D=50A,$<br>$V_{GS}=0 \text{ to } 10V$ | - | 17  | 22 | nC |
| Gate to drain charge  | $Q_{gd}$      |                                                      | - | 12  | 18 |    |
| Gate charge total     | $Q_g$         |                                                      | - | 51  | 66 |    |
| Gate plateau voltage  | $V_{plateau}$ |                                                      | - | 4.7 | -  | V  |

**Reverse Diode**

|                                                |               |                                             |   |     |     |    |
|------------------------------------------------|---------------|---------------------------------------------|---|-----|-----|----|
| Diode continuous forward current <sup>2)</sup> | $I_S$         | $T_C=25^\circ C$                            | - | -   | 100 | A  |
| Diode pulse current <sup>2)</sup>              | $I_{S,pulse}$ | $T_C=25^\circ C$                            | - | -   | 400 |    |
| Diode forward voltage                          | $V_{SD}$      | $V_{GS}=0V, I_F=50A,$<br>$T_j=25^\circ C$   | - | 0.9 | 1.2 | V  |
| Reverse recovery time <sup>2)</sup>            | $t_{rr}$      | $V_R=40V, I_F=50A,$<br>$di_F/dt=100A/\mu s$ | - | 48  | -   | ns |
| Reverse recovery charge <sup>2)</sup>          | $Q_{rr}$      |                                             | - | 55  | -   | nC |

<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

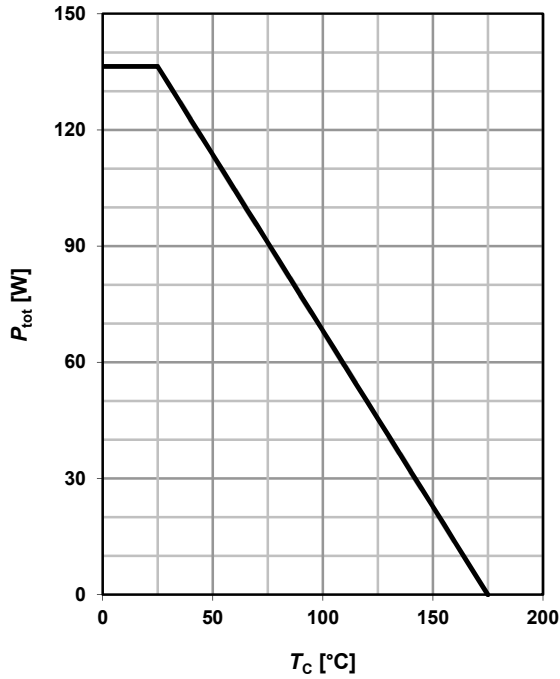
<sup>2)</sup> The parameter is not subject to production test - verified by design/characterization.

<sup>3)</sup> The product can operate at a specified current based on best practice to minimize electro-migration at the solder joint. For rare events and inrush currents, the value may be exceeded.

<sup>4)</sup> Device on a four-layer 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5-7). PCB is vertical in still air.

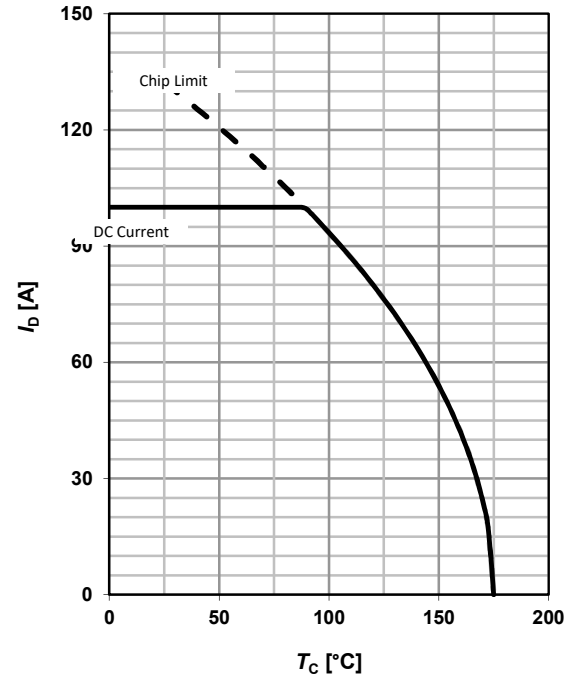
### 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



### 2 Drain current

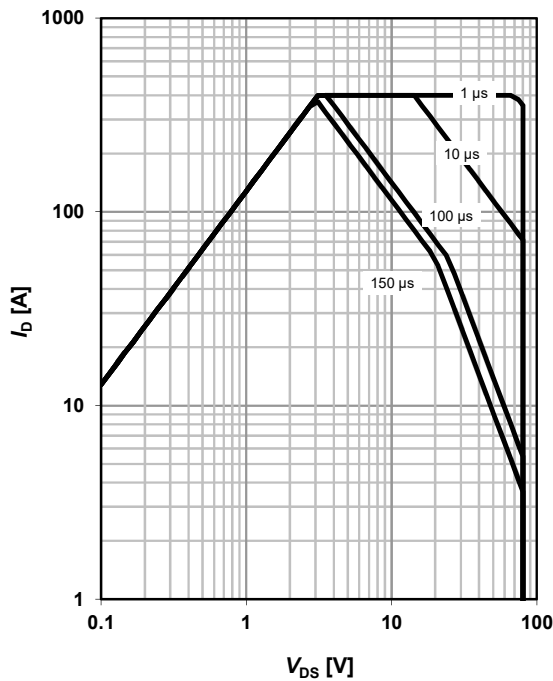
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



### 3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

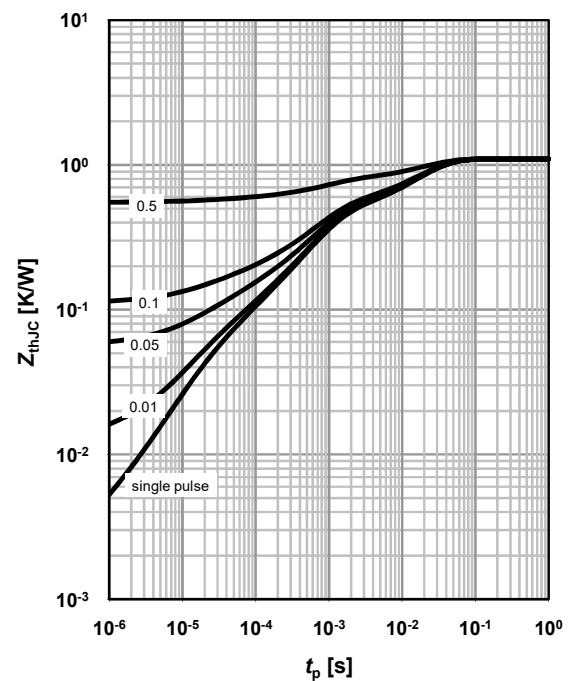
parameter:  $t_p$



### 4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

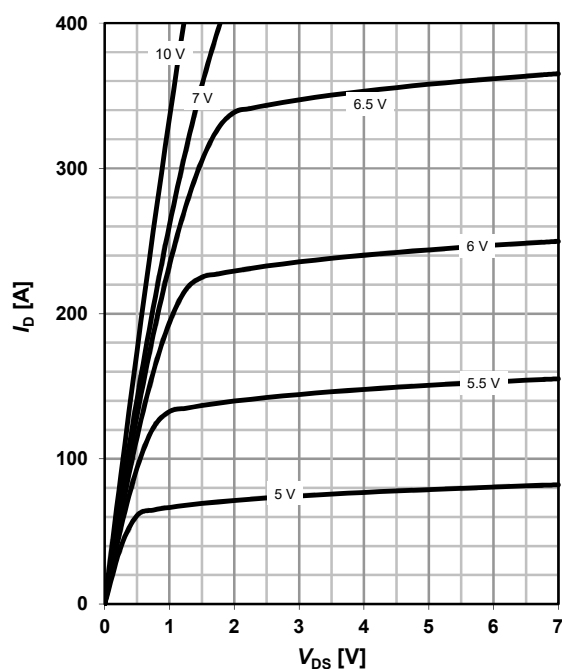
parameter:  $D = t_p/T$



## 5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

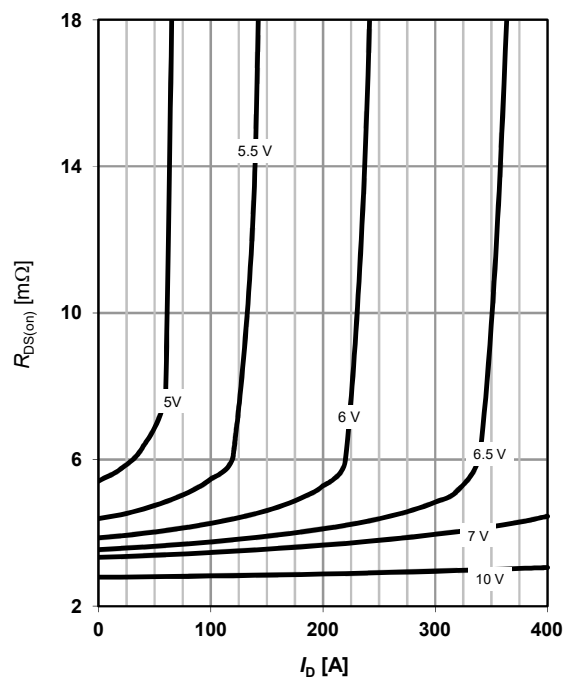
parameter:  $V_{GS}$



## 6 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

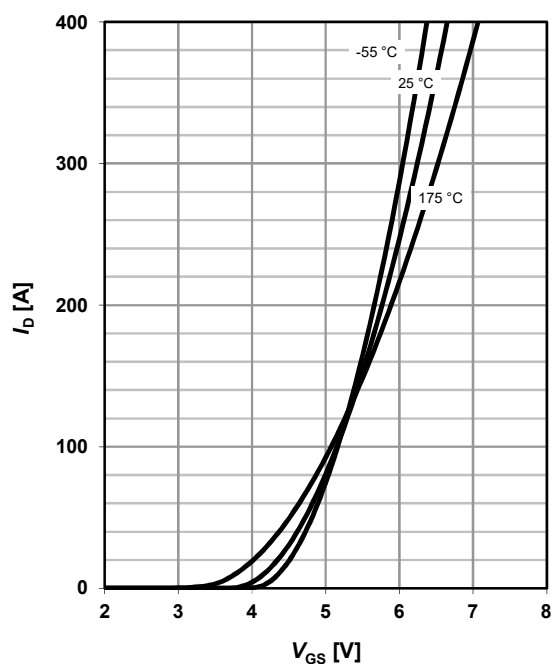
parameter:  $V_{GS}$



## 7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} = 6V$$

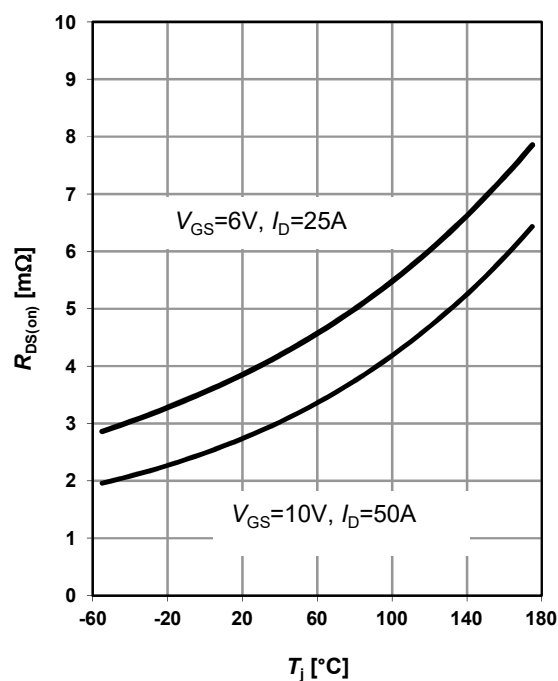
parameter:  $T_j$



## 8 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(T_j);$$

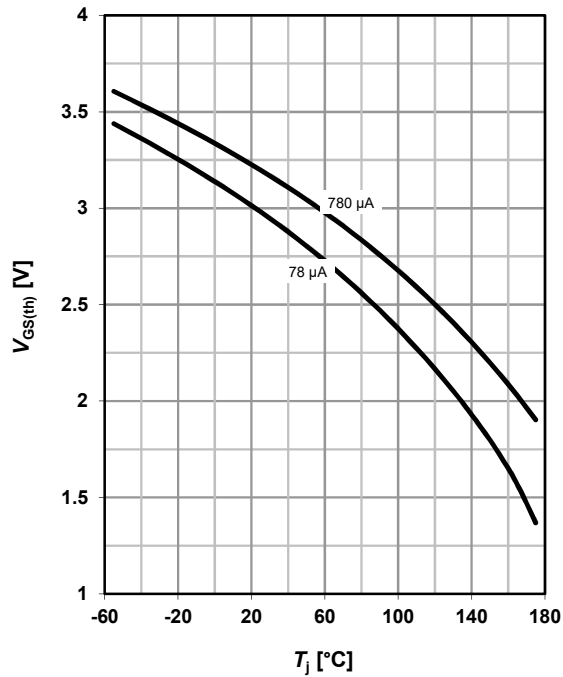
parameter:  $I_D, V_{GS}$



### 9 Typ. gate threshold voltage

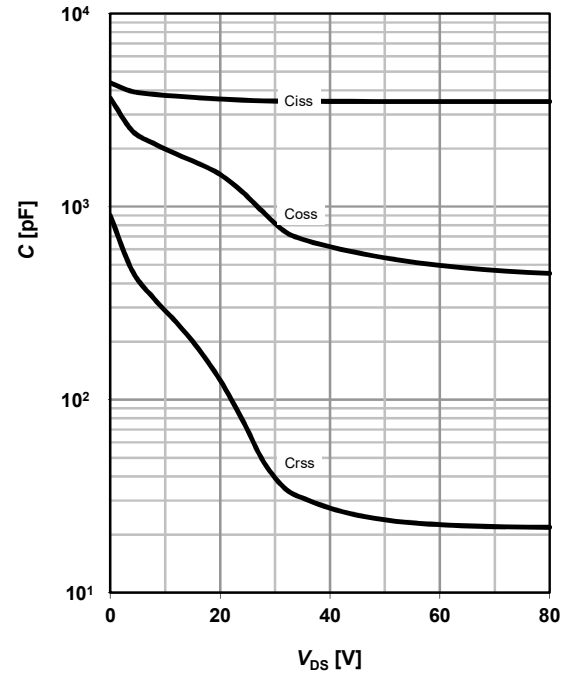
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter:  $I_D$



### 10 Typ. capacitances

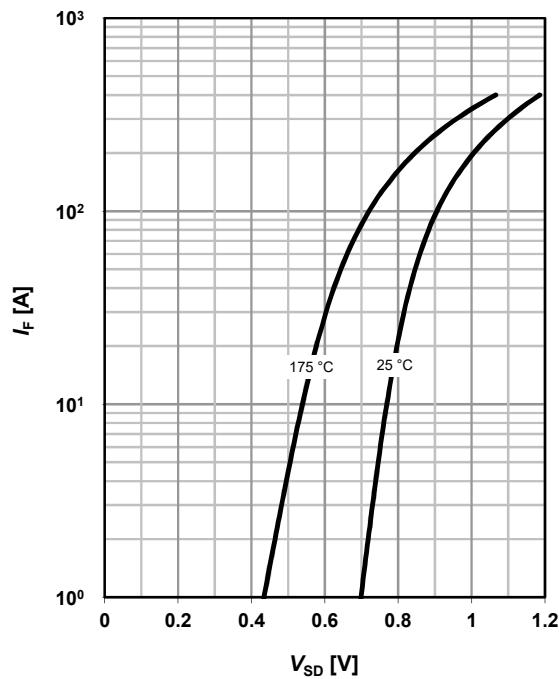
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



### 11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

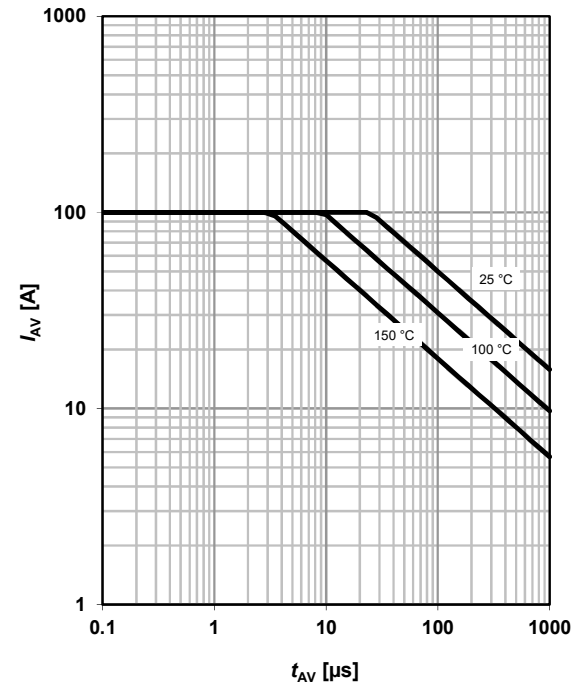
parameter:  $T_j$



### 12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

parameter:  $T_{j(start)}$



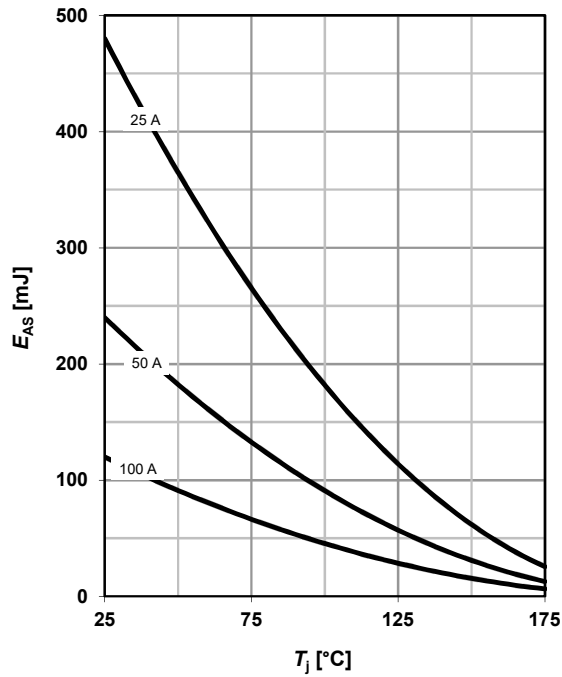


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### 13 Avalanche energy

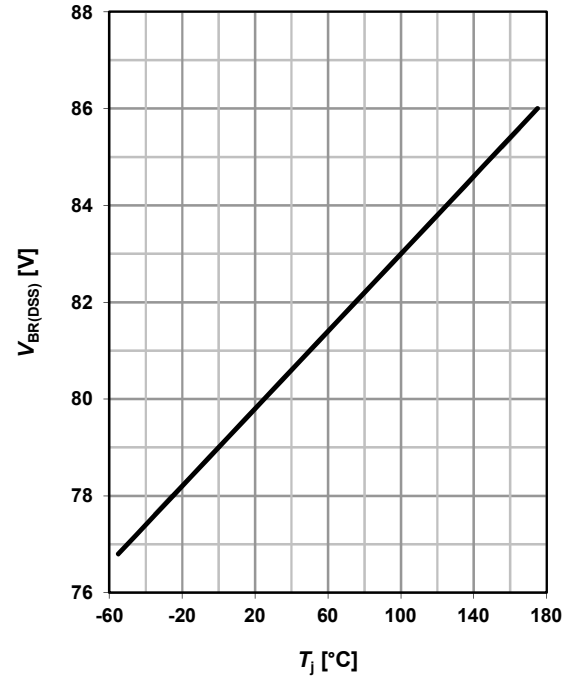
$$E_{AS} = f(T_j)$$

parameter:  $I_D$



### 14 Drain-source breakdown voltage

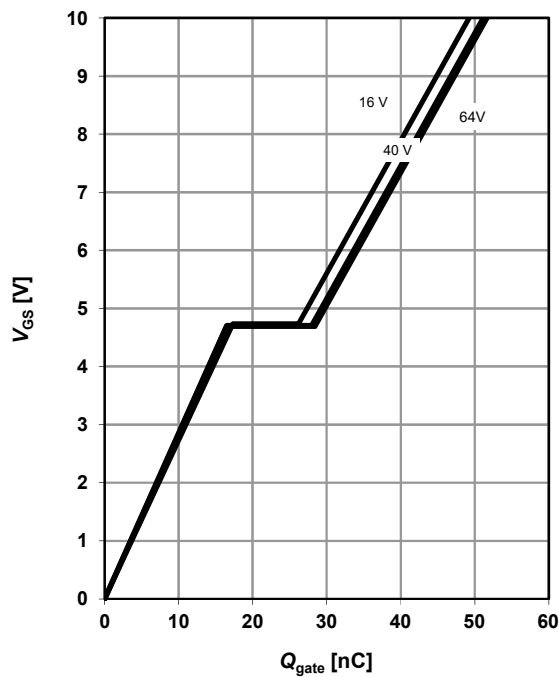
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



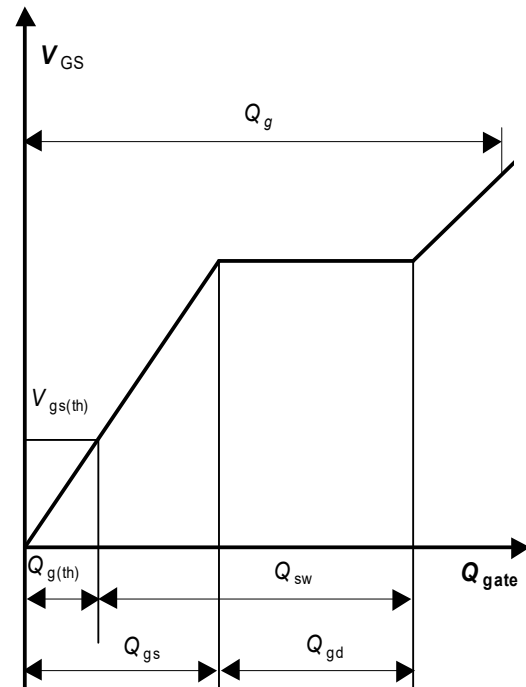
### 15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 50 \text{ A pulsed}$$

parameter:  $V_{DD}$

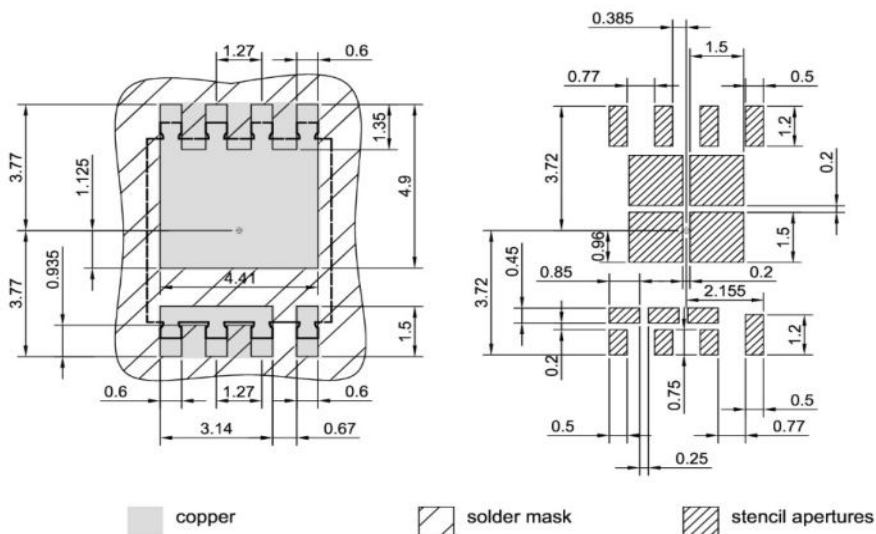


### 16 Gate charge waveforms

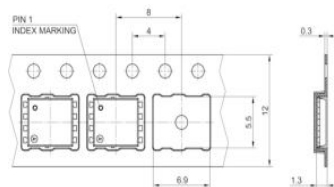


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- ## Footprint



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ALL DIMENSIONS ARE IN UNITS MM  
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 (1st Angle)



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**Revision History**

| Version      | Date       | Changes                                                       |
|--------------|------------|---------------------------------------------------------------|
| Revision 1.0 | 2021-05-17 | Final Data Sheet                                              |
| Revision 1.1 | 2021-06-18 | - Company logo size adjusted<br>- Datasheet file name updated |