



IAUC41N06S5L100

OptiMOS™ -5 Power Transistor



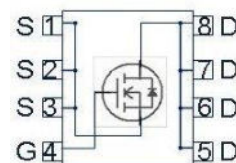
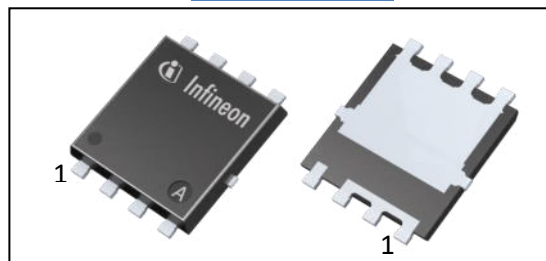
Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- MSL1 up to 260°C peak reflow
- 175 °C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	60	V
$R_{DS(on),max}$	10	mΩ
I_D	41	A

PG-TDSON-8-33



Type	Package	Marking
IAUC41N06S5L100	PG-TDSON-8-33	5N06L100

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	41	A
		$V_{GS}=10\text{ V}$, DC current	41	
		$T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,3)}	12	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$	115	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=20\text{ A}$	37	mJ
Avalanche current, single pulse	I_{AS}	-	41	A
Gate source voltage	V_{GS}	-	± 16	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	42	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	3.6	K/W
Thermal resistance, junction - ambient ³⁾	R_{thJA}	-	-	25.5	-	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=13\mu A$	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=60V, V_{GS}=0V, T_j=125^\circ\text{C}^{1)}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=16V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=20A$	-	11.6	13.9	$m\Omega$
		$V_{GS}=10V, I_D=20A$	-	7.9	10	
Gate resistance ²⁾	R_G	-	-	1.1	-	Ω



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=30V,$ $f=1MHz$	-	927	1205	pF
Output capacitance	C_{oss}		-	183	238	
Reverse transfer capacitance	C_{rss}		-	12	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V,$ $I_D=20A, R_{G,ext}=3.5\Omega$	-	2.4	-	ns
Turn-off delay time	$t_{d(off)}$		-	6.7	-	
Rise time	t_r		-	1.0	-	
Fall time	t_f		-	2.2	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=30V, I_D=20A,$ $V_{GS}=0 \text{ to } 10V$	-	3.0	4.0	nC
Gate to drain charge	Q_{gd}		-	2.1	3.1	
Gate charge total	Q_g		-	12.7	16.4	
Gate plateau voltage	$V_{plateau}$		-	3.3	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	41	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25^\circ C, t_p=100 \mu s$	-	-	115	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=20A,$ $T_j=25^\circ C$	-	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=30V, I_F=41A,$ $di_F/dt=100A/\mu s$	-	26	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	16	-	nC

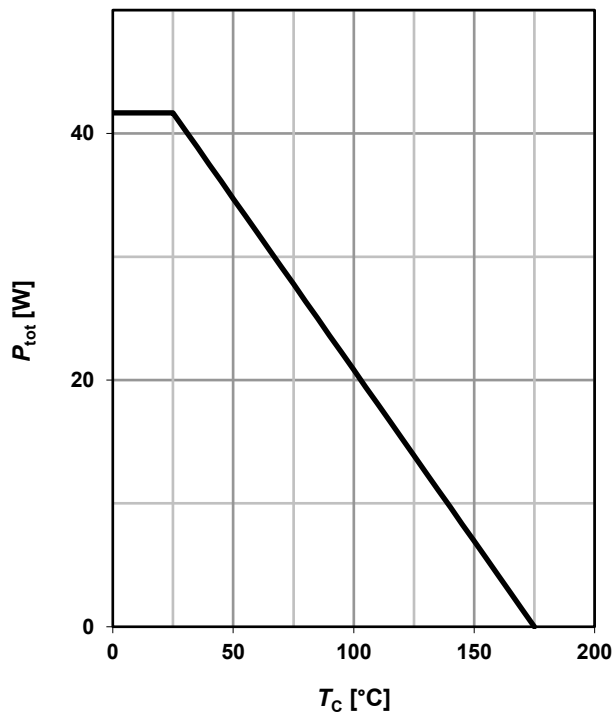
¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production test - verified by design/characterization.

³⁾ Device on a four-layer 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5-7). PCB is vertical in still air.

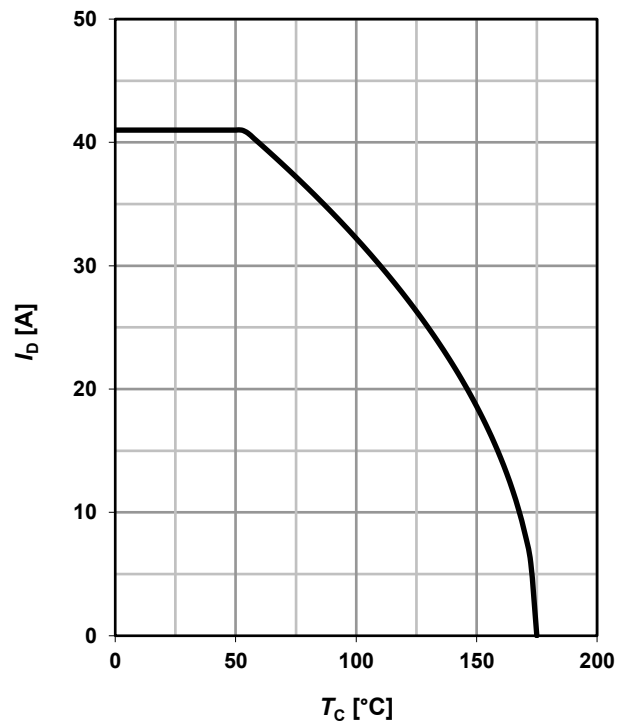
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



2 Drain current

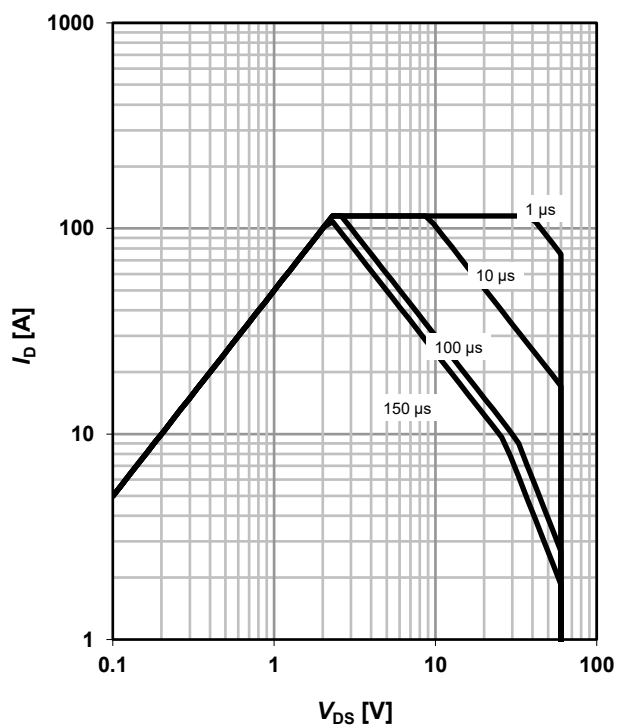
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

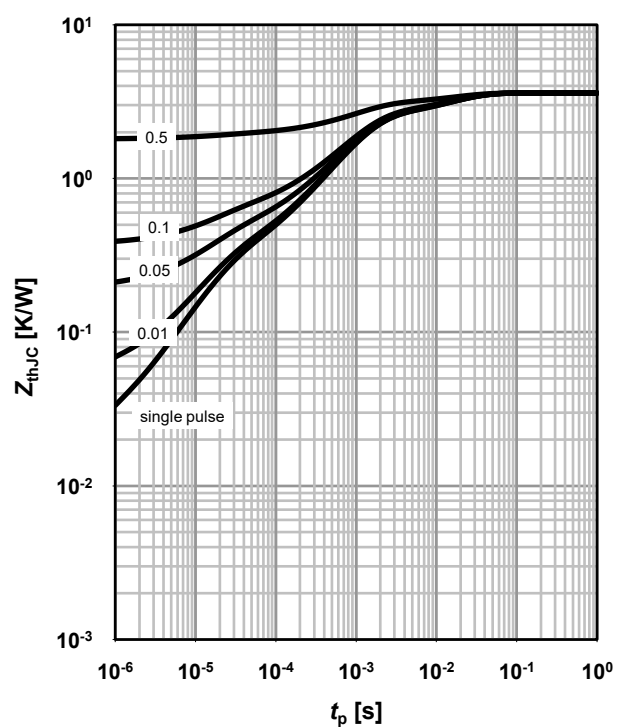
parameter: t_p



4 Max. transient thermal impedance

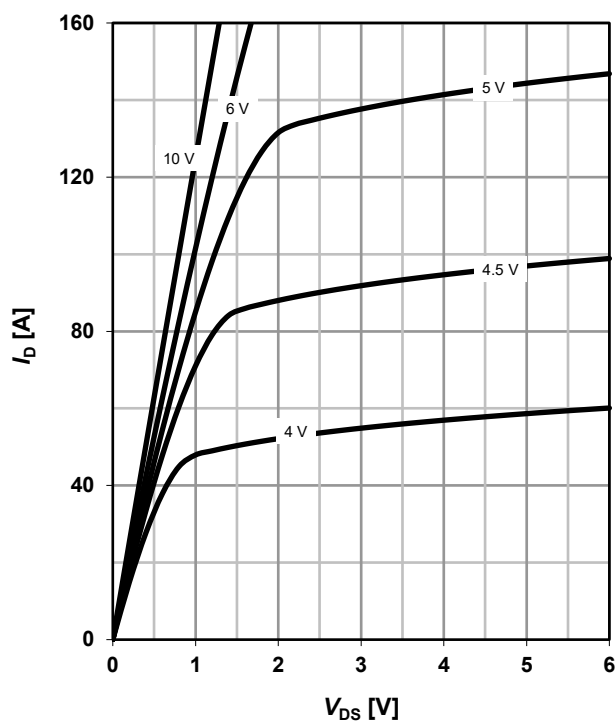
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$

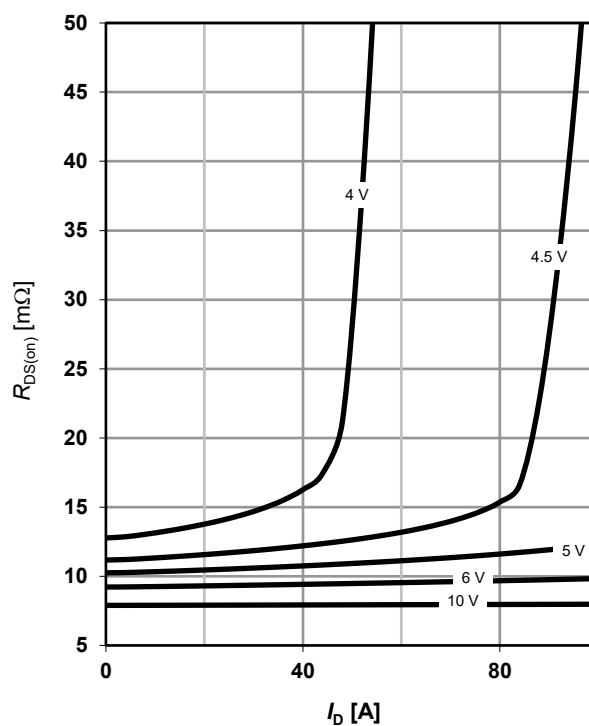


5 Typ. output characteristics

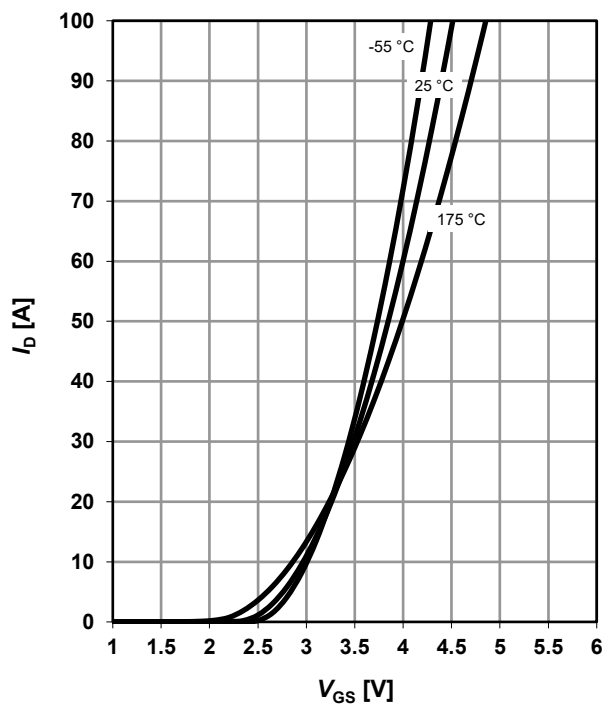
$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

parameter: V_{GS} **6 Typ. drain-source on-state resistance**

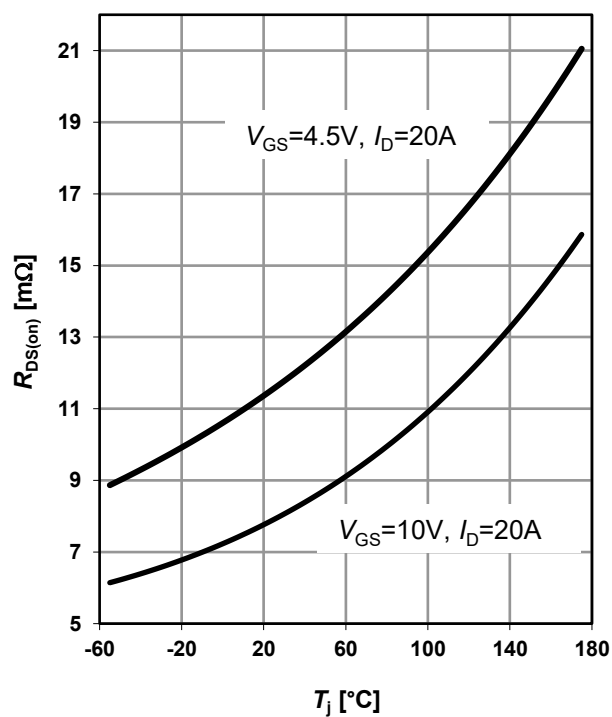
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

parameter: V_{GS} **7 Typ. transfer characteristics**

$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

parameter: T_j **8 Typ. drain-source on-state resistance**

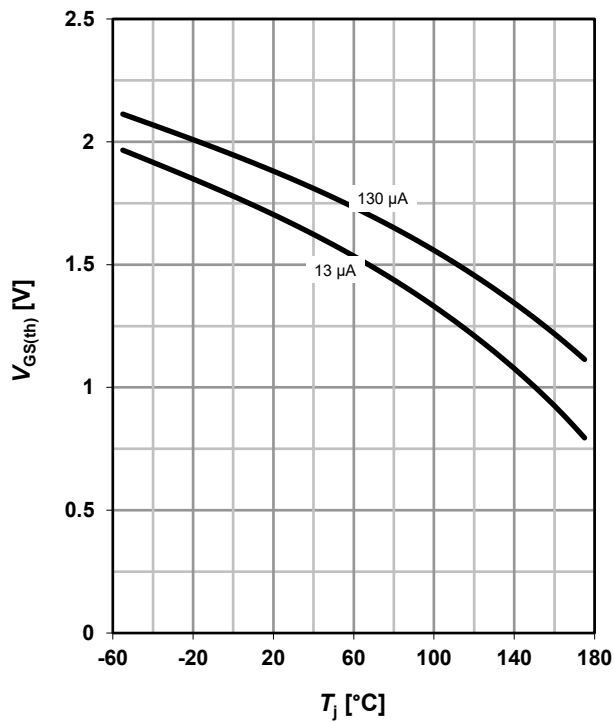
$$R_{DS(on)} = f(T_j);$$

parameter: I_D, V_{GS} 

9 Typ. gate threshold voltage

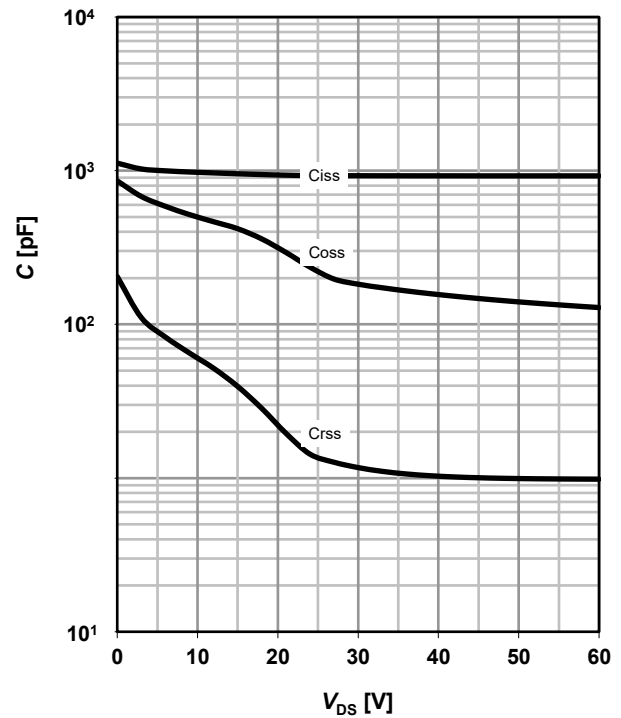
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

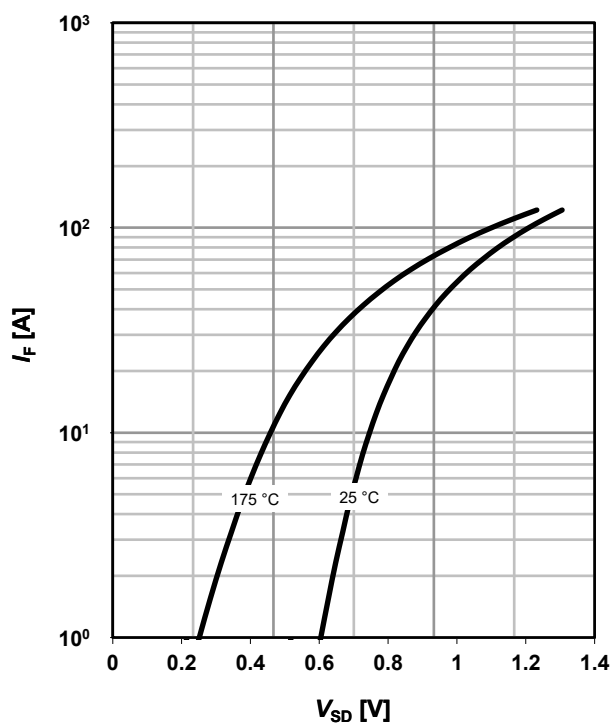
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

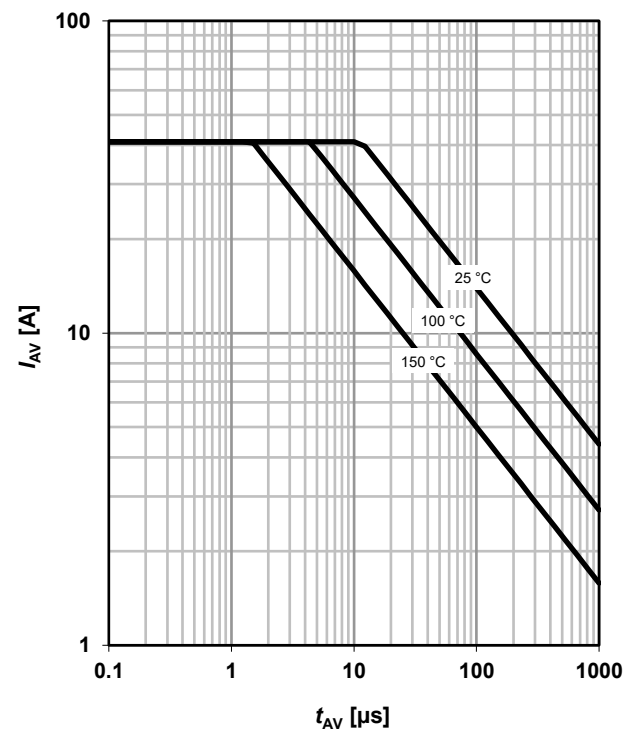
parameter: T_j



12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

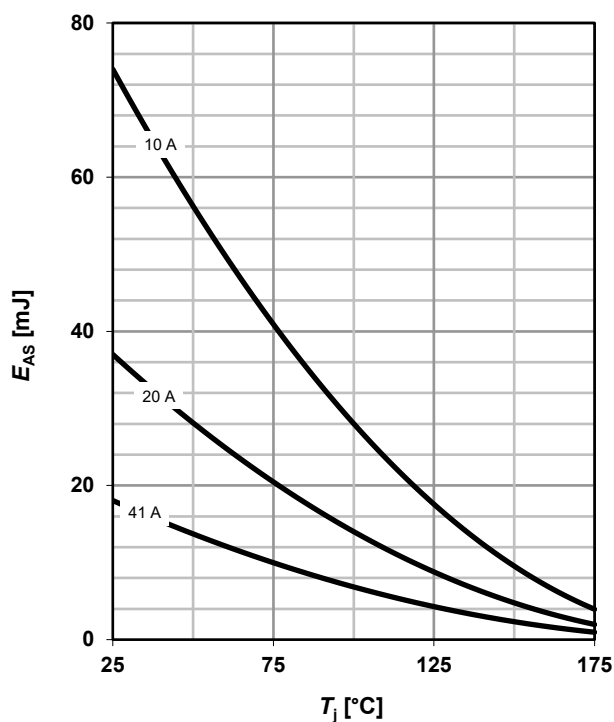
parameter: $T_{j(start)}$



13 Avalanche energy

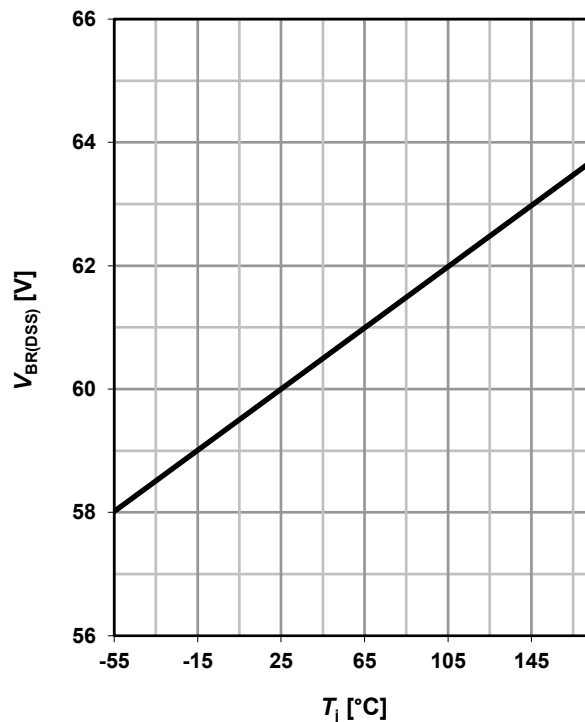
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

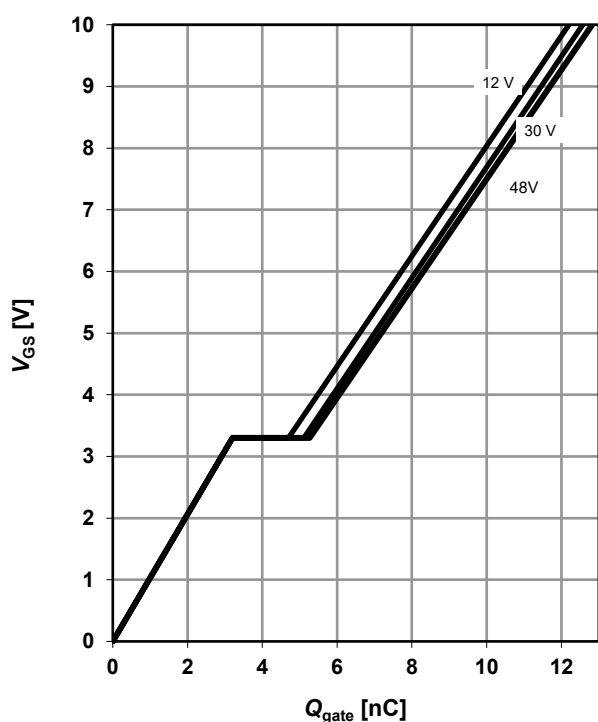
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



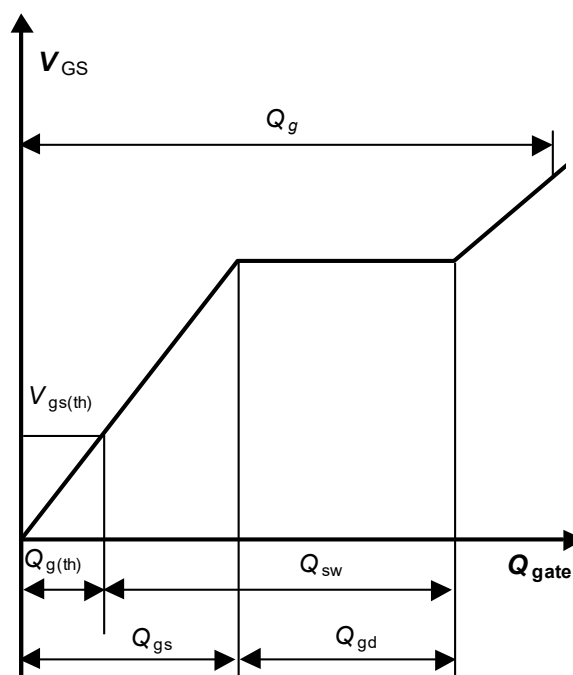
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 20 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



Technical drawing of a rectangular metal component, showing multiple views and dimensions:

- Top View:**
 - Overall width: 5.15 ± 0.1
 - Overall height: 6.44 ± 0.1
 - Internal width: 4.48 ± 0.1
 - Internal height: 5.48 ± 0.1
 - Top edge features: 8 (left), 5 (right)
 - Bottom edge features: 1 (left), 4 (right)
 - Bottom edge dimension: 0.44 ± 0.1
 - Bottom edge feature dimension: 1.27
 - Bottom edge feature dimension: $0 \dots 0.075$
 - Feature A: INDEX MARKING
 - Feature B: 0.03
 - Feature C: 0.25 (M)
 - Feature D: 0.12 ± 0.1
- Side View:**
 - Overall height: 0.25 ± 0.1
- Front View:**
 - Overall width: 4.3 ± 0.1
 - Overall height: 0.9 ± 0.1
 - Internal width: 4.3 ± 0.1
 - Internal height: 0.4 ± 0.1
 - Top edge features: 5 (left), 8 (right)
 - Bottom edge features: 4 (left), 1 (right)
 - Bottom edge dimension: 0.12 ± 0.1
 - Bottom edge feature dimension: 0.8 ± 0.1
 - Bottom edge feature dimension: 3.8 ± 0.1

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Revision History

Version	Date	Changes
Revision 1.0	05.05.2020	Final Data Sheet