

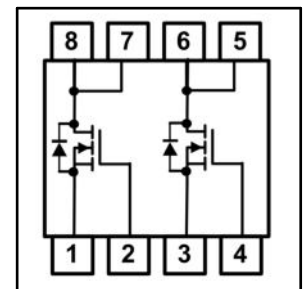
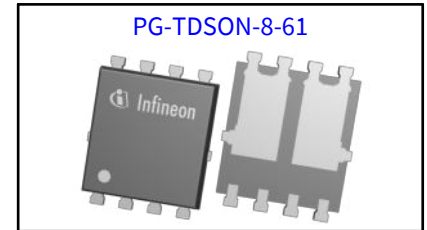
## Automotive MOSFET

### OptiMOS™ 7 Power-Transistor



#### Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested



#### Potential Applications

General automotive applications.

#### Product Validation

Qualified for automotive applications. Product validation according to AEC-Q101.

#### Product Summary

$V_{DS}$	40	V
$R_{DS(on)}$	5.34	mΩ
$I_D$ (chip limited)	64	A

Type	Package	Marking
IAUCN04S7L053D	PG-TDSON-8-61	7N4L053D

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## Maximum Ratings

 at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS} = 10\text{ V}$ , Chip limitation <sup>1,2)</sup>	64	A
		$V_{GS} = 10\text{ V}$ , DC current	60	
		$T_a = 100^\circ\text{C}$ , $V_{GS} = 10\text{ V}$ , $R_{thJA}$ on 2s2p <sup>2,3)</sup>	12	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C = 25^\circ\text{C}$ , $t_p = 100\ \mu\text{s}$	140	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D = 14\text{ A}$	25	mJ
Avalanche current, single pulse	$I_{AS}$	–	27	A
Gate source voltage	$V_{GS}$	–	$\pm 16$	V
		Limited to duty factor of 1%	+20	
Power dissipation	$P_{tot}$	$T_C = 25^\circ\text{C}$	41	W
Operating and storage temperature	$T_j, T_{stg}$	–	-55 ... +175	$^\circ\text{C}$

**Thermal Characteristics<sup>2)</sup>**

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	–	–	–	3.7	K/W
Thermal resistance, junction - ambient <sup>3)</sup>	$R_{thJA}$	–	–	49	–	

**Electrical Characteristics**

 at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Static Characteristics**

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	40	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 10\text{ }\mu\text{A}$	1.2	1.5	1.8	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 25\text{ °C}$	–	–	1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 100\text{ °C}^{2)}$	–	–	3	
Gate-source leakage current	$I_{GSS}$	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}$ , $I_D = 30\text{ A}$	–	6.70	7.70	m $\Omega$
		$V_{GS} = 10\text{ V}$ , $I_D = 30\text{ A}$	–	4.69	5.34	
Gate resistance <sup>2)</sup>	$R_G$	–	–	2.3	–	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Dynamic Characteristics<sup>2)</sup></b>						
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	-	700	910	pF
Output capacitance	$C_{oss}$		-	350	455	
Reverse transfer capacitance	$C_{rss}$		-	15	22	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 30\text{ A}, R_G = 3.5\ \Omega$	-	4	-	ns
Rise time	$t_r$		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	11	-	
Fall time	$t_f$		-	3	-	

<b>Gate Charge Characteristics<sup>2)</sup></b>						
Gate to source charge	$Q_{gs}$	$V_{DD} = 20\text{ V}, I_D = 30\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$	-	2.1	3	nC
Gate to drain charge	$Q_{gd}$		-	1.9	3	
Gate charge total	$Q_g$		-	11	14	
Gate plateau voltage	$V_{plateau}$		-	3	-	V

<b>Reverse Diode</b>						
Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C = 25^\circ\text{C}$	-	-	60	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	$T_C = 25^\circ\text{C}, t_p = 100\ \mu\text{s}$	-	-	140	
Diode forward voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_F = 30\text{ A}, T_j = 25^\circ\text{C}$	-	0.8	0.95	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R = 20\text{ V}, I_F = 50\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	10	15	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	1	2	nC

<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

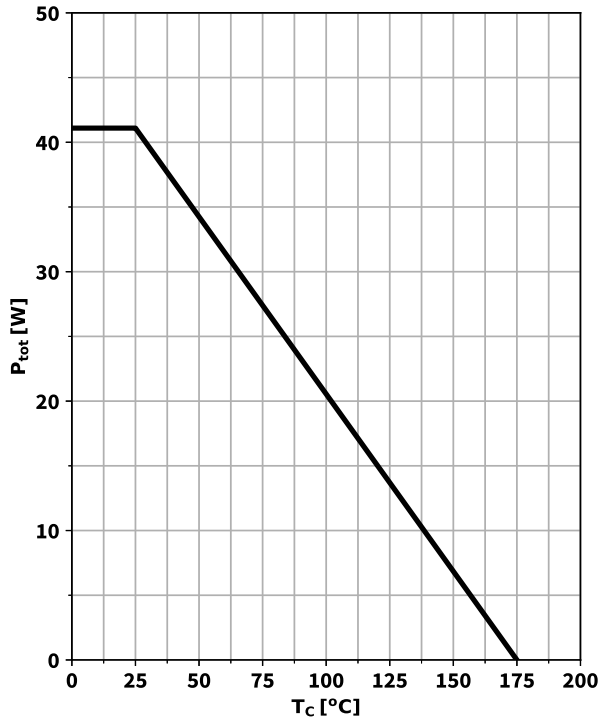
<sup>2)</sup> The parameter is not subject to production testing – specified by design.

<sup>3)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

## Electrical characteristics diagrams

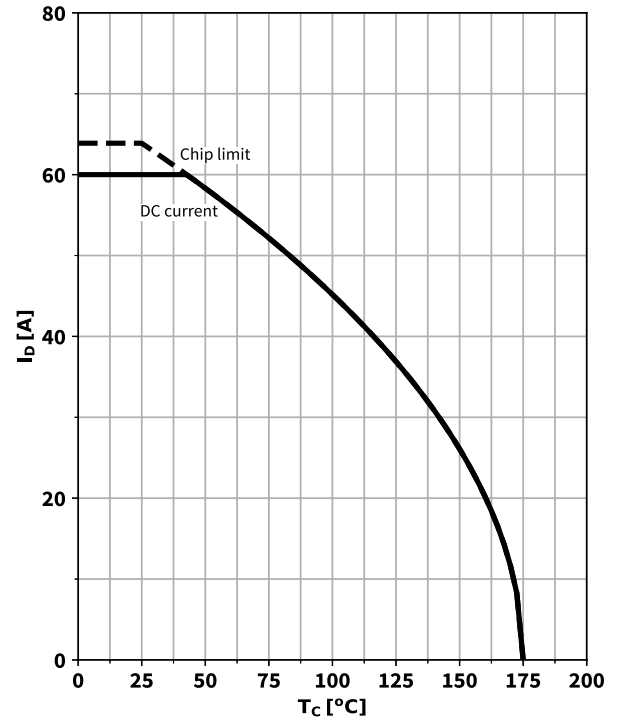
### 1 Power dissipation

$$P_{tot} = f(T_C); V_{GS} \geq 6 \text{ V}$$



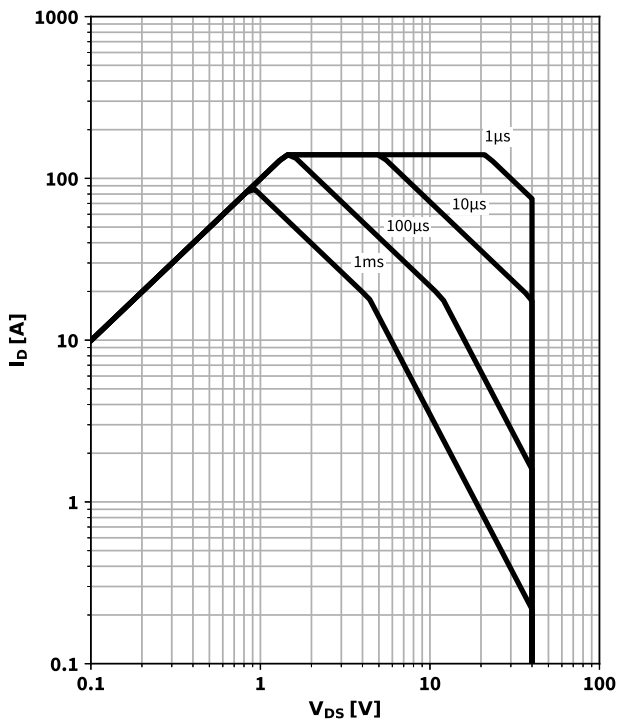
### 2 Drain current

$$I_D = f(T_C); V_{GS} \geq 6 \text{ V}$$



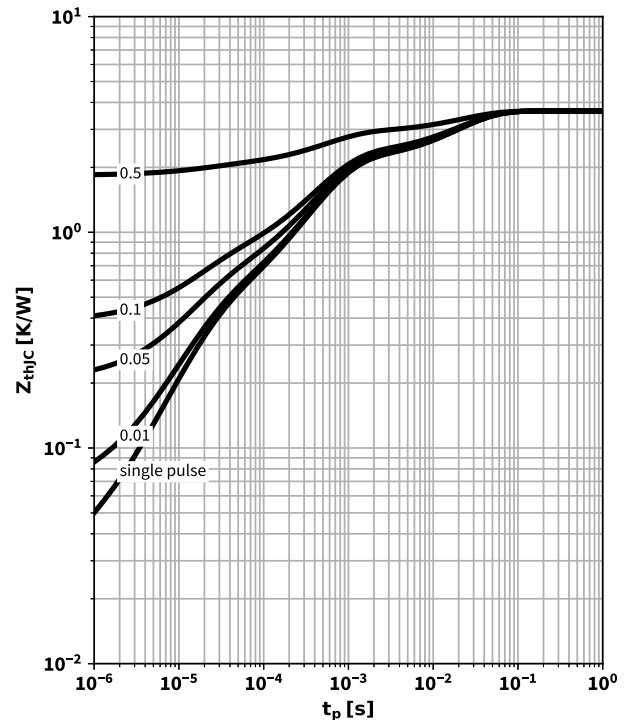
### 3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0; \text{ parameter: } t_p$$



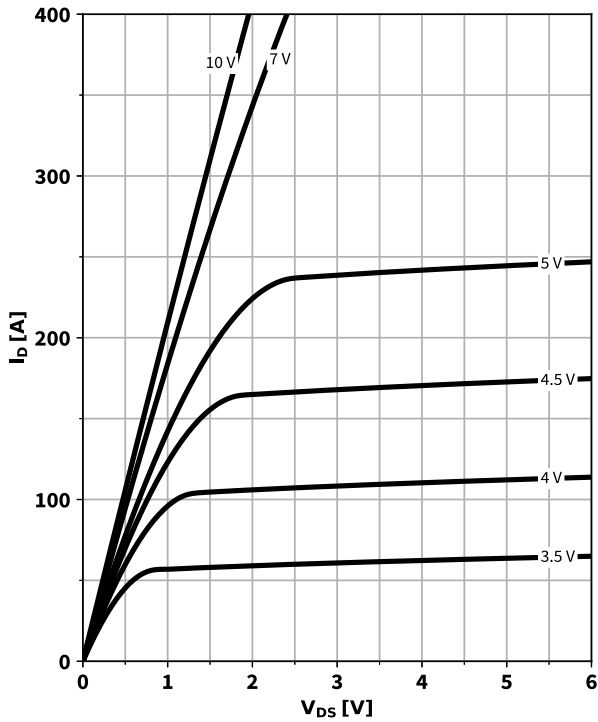
### 4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p); \text{ parameter: } D = t_p/T$$



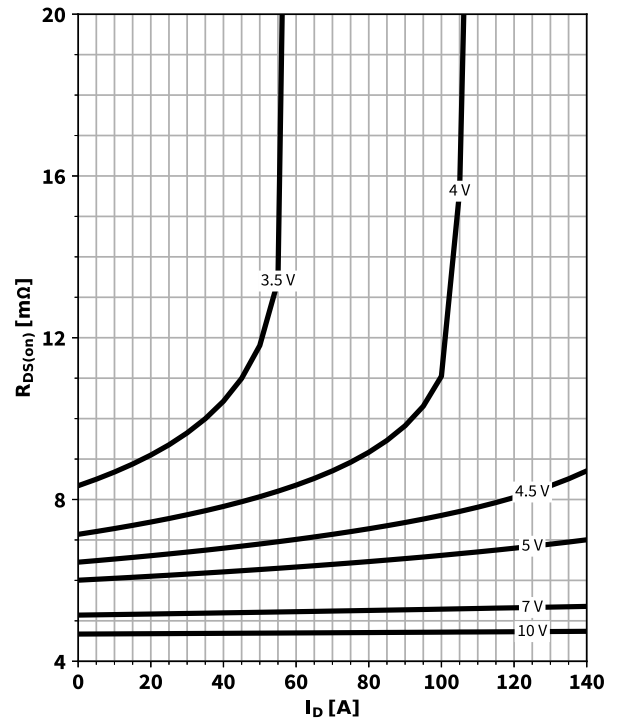
5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C};$  parameter:  $V_{GS}$



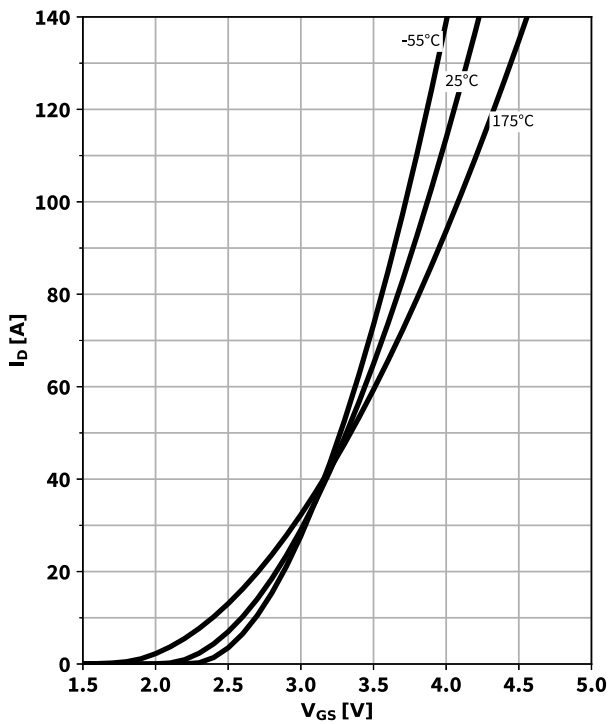
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C};$  parameter:  $V_{GS}$



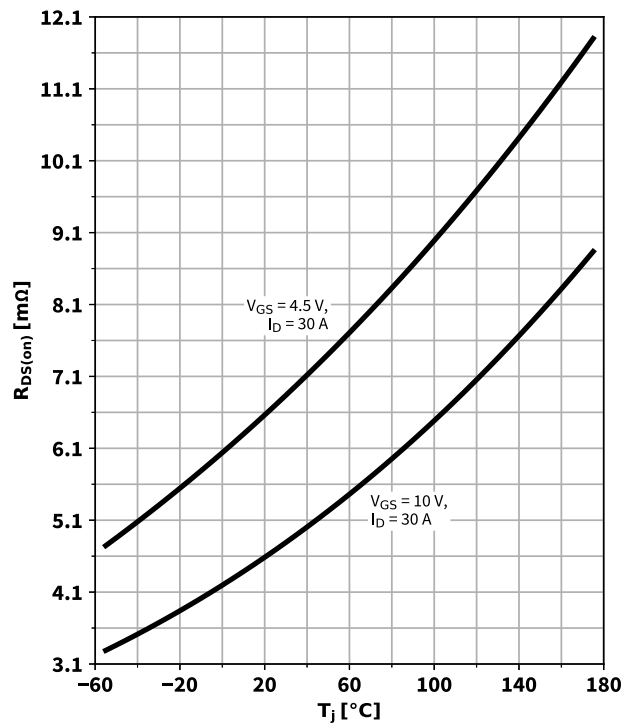
7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{ V};$  parameter:  $T_j$



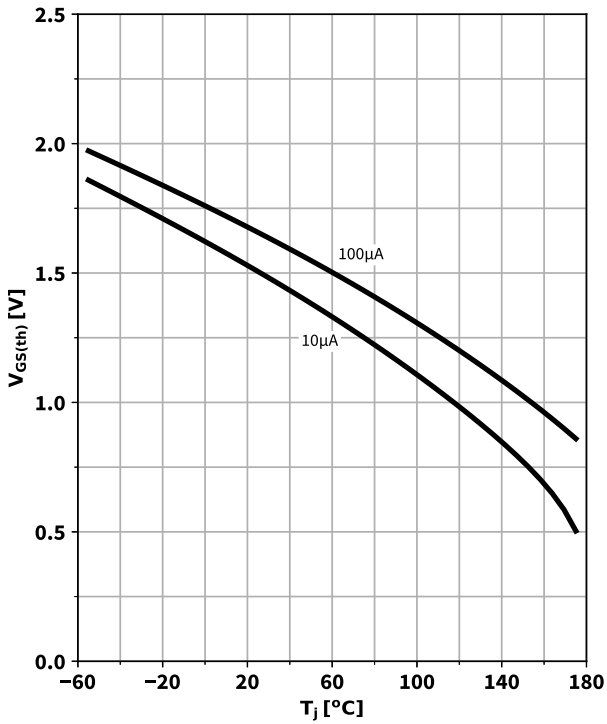
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j);$  parameter:  $I_D, V_{GS}$



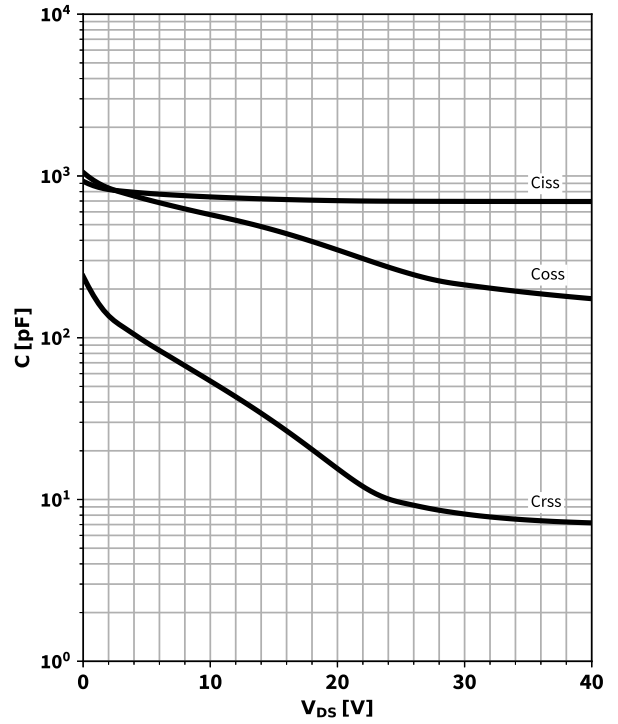
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$ ;  $V_{GS} = V_{DS}$ ; parameter:  $I_D$



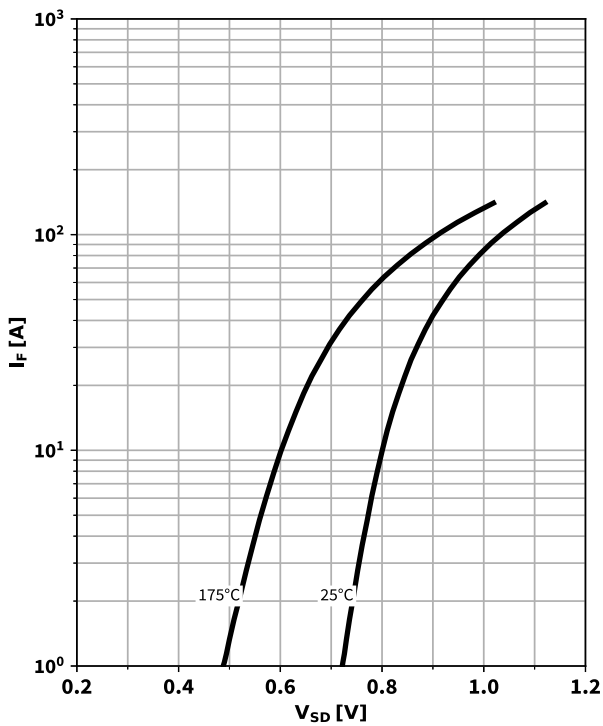
10 Typ. capacitances

$C = f(V_{DS})$ ;  $V_{GS} = 0 V$ ;  $f = 1 MHz$



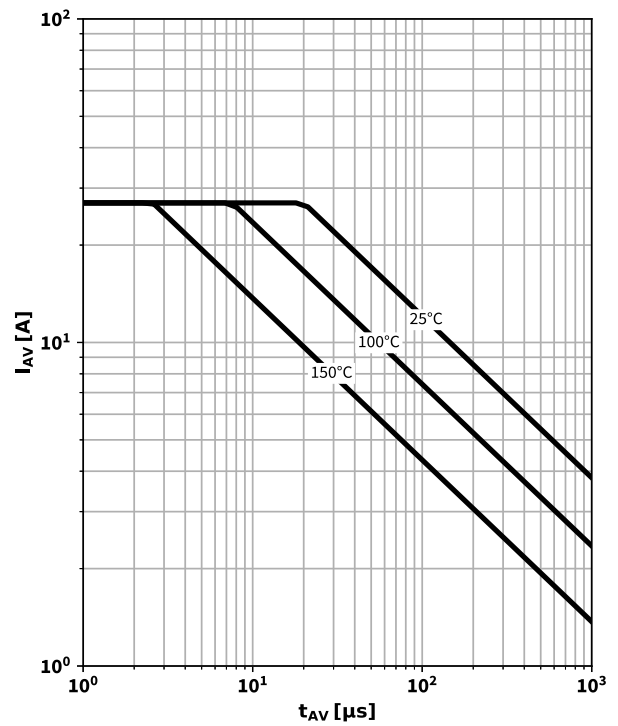
11 Typ. forward diode characteristics

$I_F = f(V_{SD})$ ; parameter:  $T_j$



12 Typ. avalanche characteristics

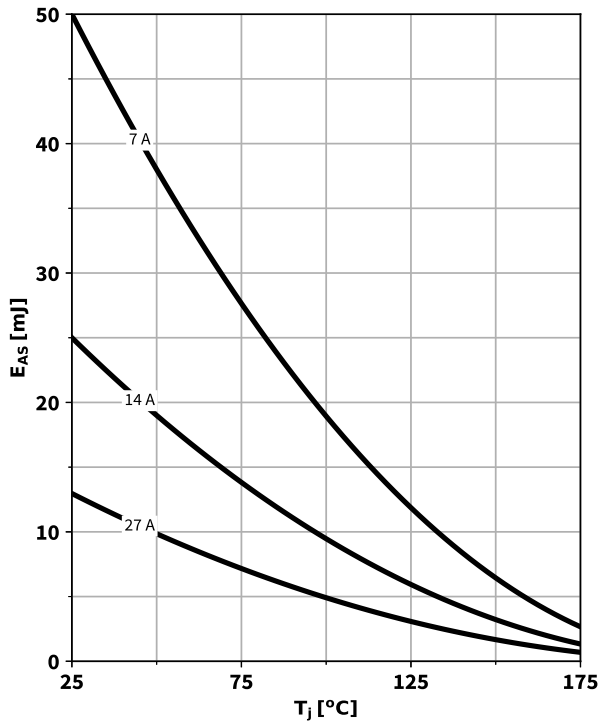
$I_{AS} = f(t_{AV})$ ; parameter:  $T_{j(start)}$





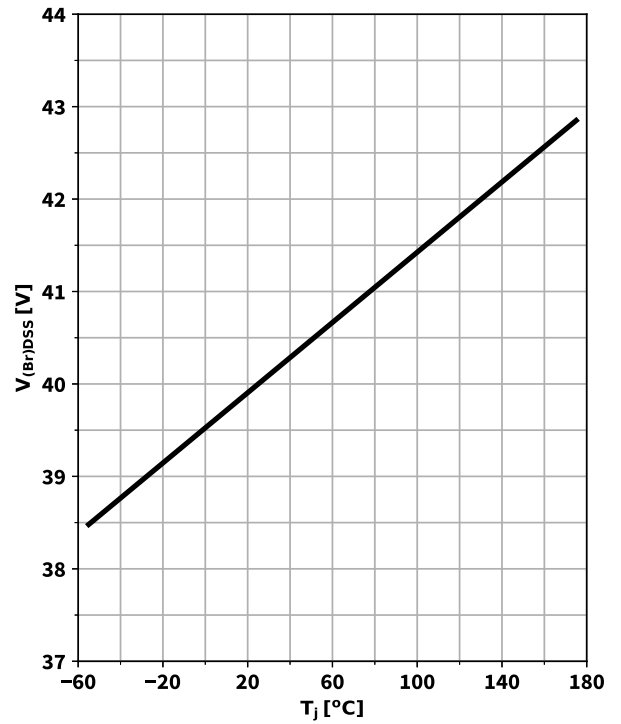
**13 Typical avalanche energy**

$E_{AS} = f(T_j)$ ; parameter:  $I_D$



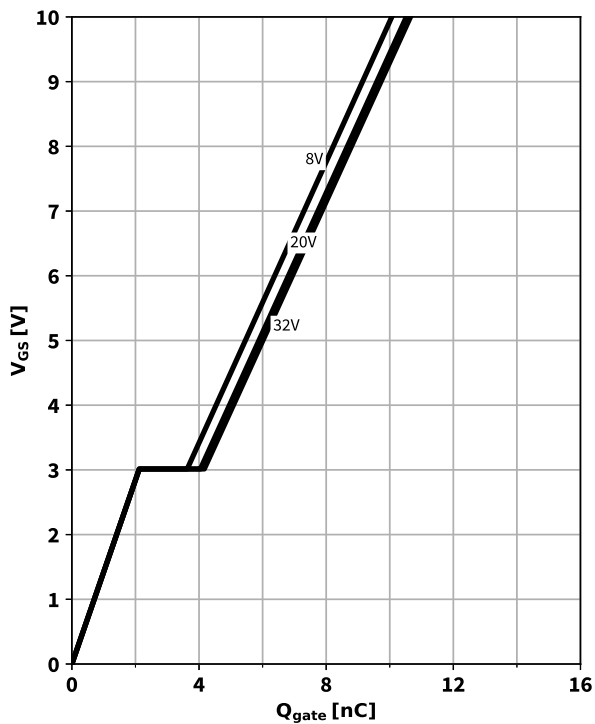
**14 Drain-source breakdown voltage**

$V_{(BR)DSS} = f(T_j)$ ;  $I_D = 1$  mA

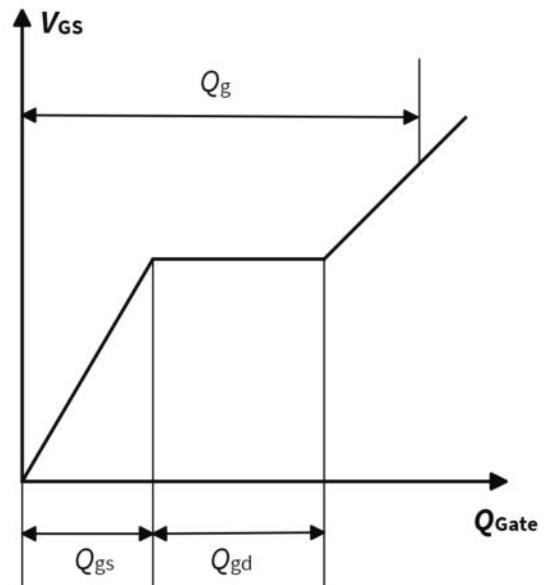


**15 Typ. gate charge**

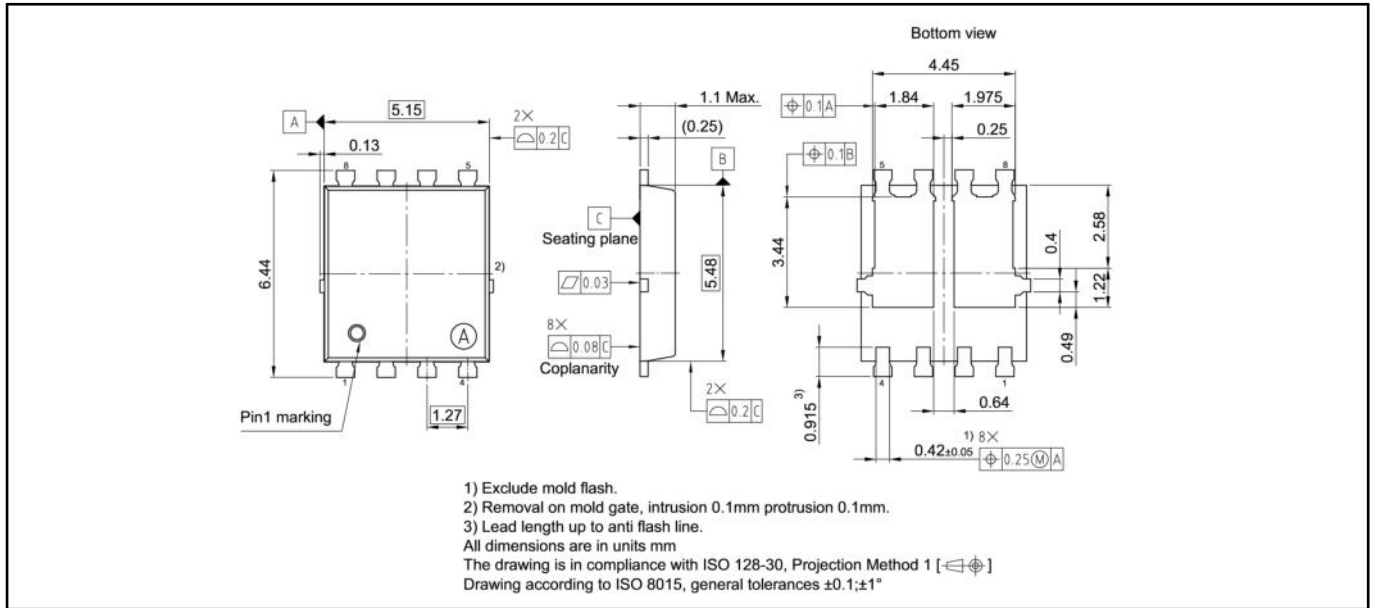
$V_{GS} = f(Q_{gate})$ ;  $I_D = 30$  A pulsed; parameter:  $V_{DD}$



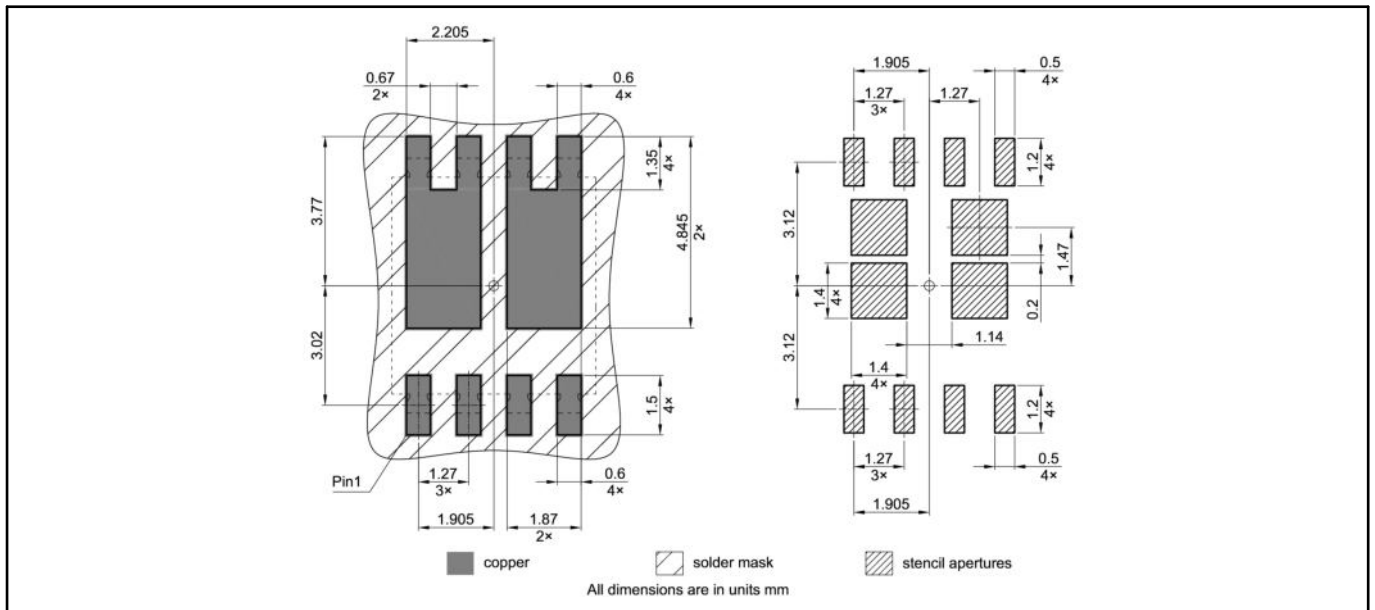
**16 Gate charge waveforms**



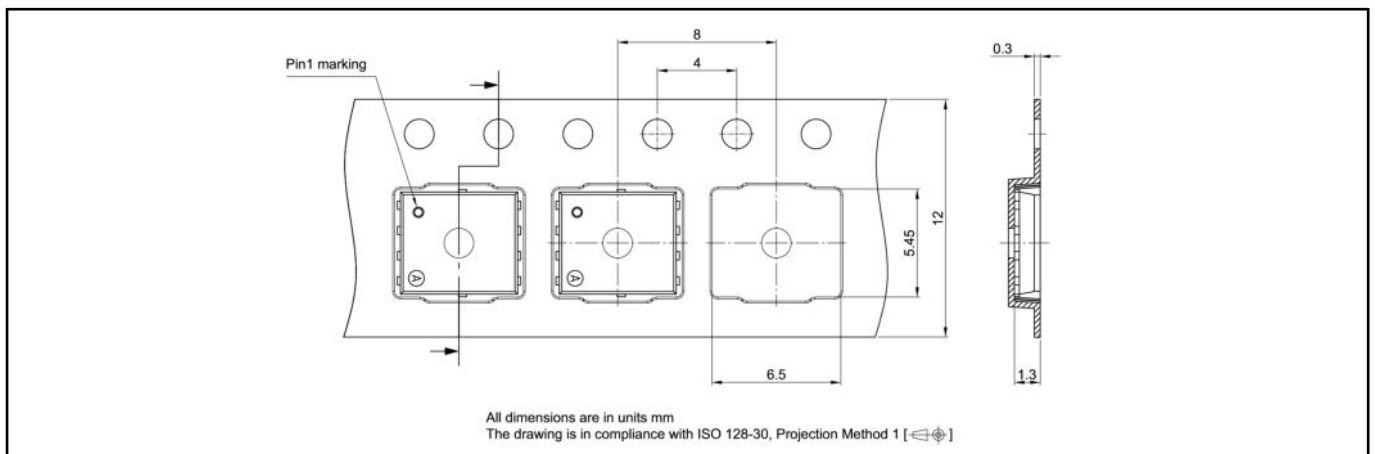
## Package Outline



## Footprint



## Packaging



**Revision History**

Revision	Date	Changes
Revision 1.0	2024-08-01	Final Data Sheet

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