

Automotive MOSFET

OptiMOS™ 5 Power-Transistor



Features

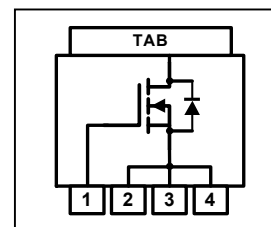
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL2 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



Product Summary

V_{DS}	100	V
$R_{DS(on)}$	1.7	mΩ
I_D (chip limited)	290	A

Type	Package	Marking
IAUMN10S5N017G	PG-HSOG-4-1	5N10N017



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Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	290	A
		$V_{GS}=10\text{ V}$, DC current ³⁾	200	
		$T_a=100\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,4)}	62	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$	1000	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=100\text{ A}$	578	mJ
Avalanche current, single pulse	I_{AS}	–	200	A
Gate source voltage	V_{GS}	–	± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	307	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C

Thermal characteristics²⁾

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	0.49	K/W
Thermal resistance, junction - ambient ³⁾	R_{thJA}	–	–	7.8	–	

Electrical characteristics

 at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Static characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	100	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=215\text{ }\mu\text{A}$	2.2	3	3.8	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	–	–	1	μA
		$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=100\text{ °C}^{2)}$	–	–	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6\text{ V}$, $I_D=50\text{ A}$	–	1.8	2.2	m Ω
		$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$	–	1.3	1.7	
Gate resistance ²⁾	R_G	–	–	1.3	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics ²⁾						
Input capacitance	C _{iss}	V _{GS} =0 V, V _{DS} =50 V, f=1 MHz	–	9626	12514	pF
Output capacitance	C _{oss}		–	1545	2010	
Reverse transfer capacitance	C _{rss}		–	67	90	
Turn-on delay time	t _{d(on)}	V _{DD} =50 V, V _{GS} =10 V, I _D =100 A, R _G =3.5 Ω	–	23	–	ns
Rise time	t _r		–	12	–	
Turn-off delay time	t _{d(off)}		–	50	–	
Fall time	t _f		–	48	–	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=50\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	–	44	57	nC
Gate to drain charge	Q_{gd}		–	26	39	
Gate charge total	Q_g		–	131	170	
Gate plateau voltage	$V_{plateau}$		–	4.5	–	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ °C}$	–	–	200	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	–	–	1000	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$	–	0.9	1.2	V
Reverse recovery time ²⁾	t_{rr}	$V_R=50\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	–	77	116	ns
Reverse recovery charge ²⁾	Q_{rr}		–	166	332	nC

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production testing – specified by design.

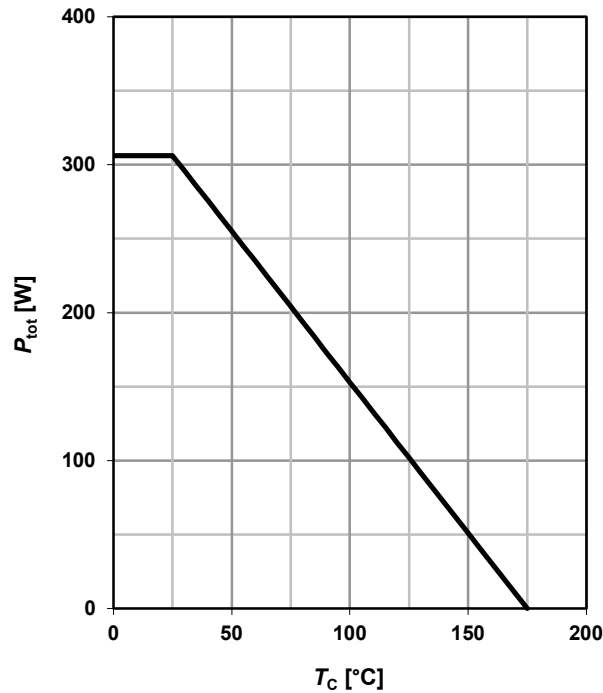
³⁾ Current is limited by package.

⁴⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

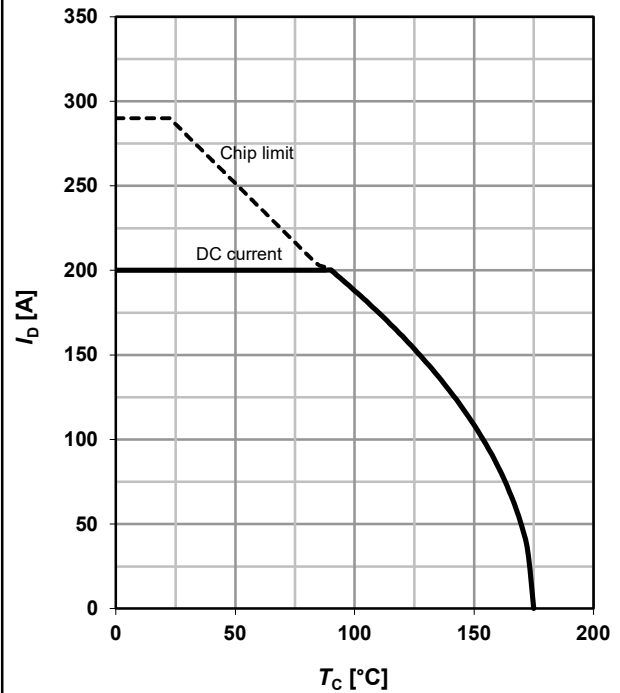
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



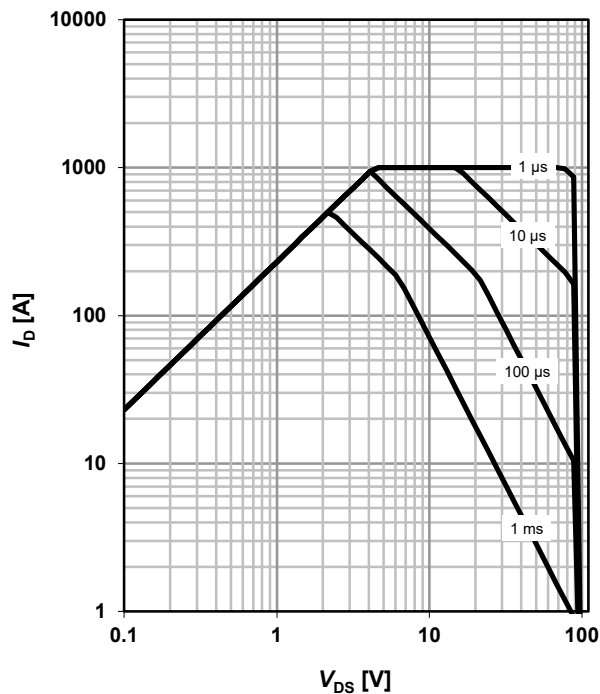
2 Drain current

$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



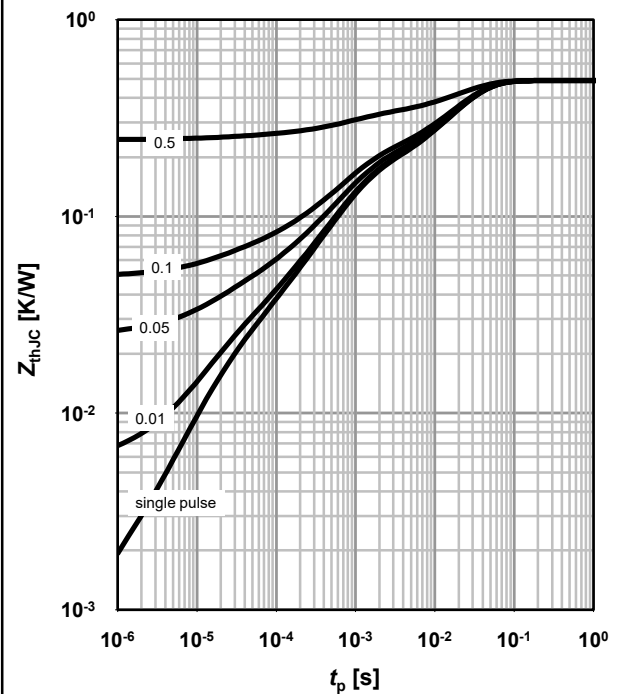
3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0; \text{parameter: } t_p$$



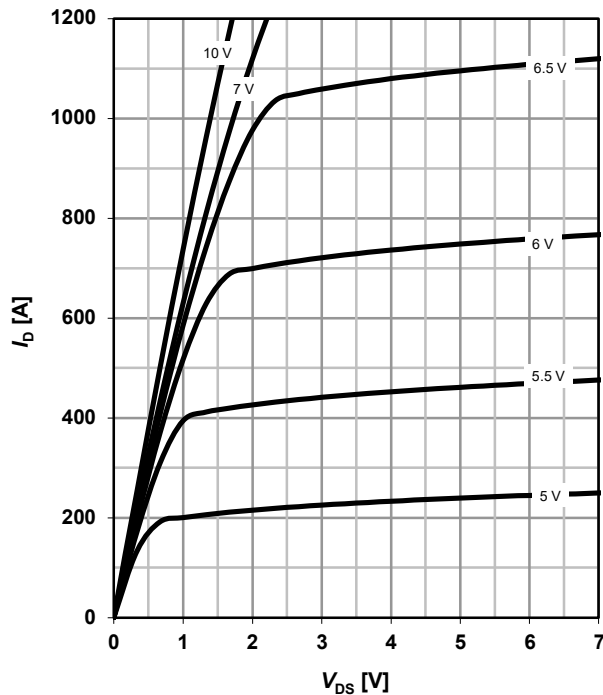
4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p); \text{parameter: } D = t_p/T$$



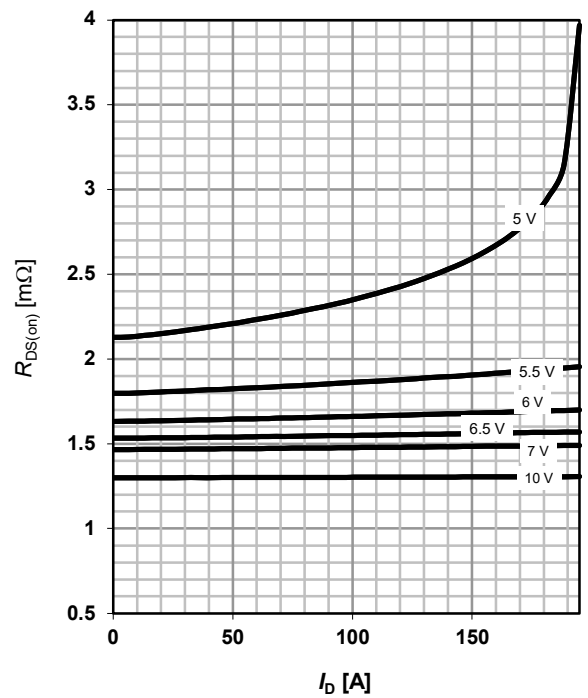
5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



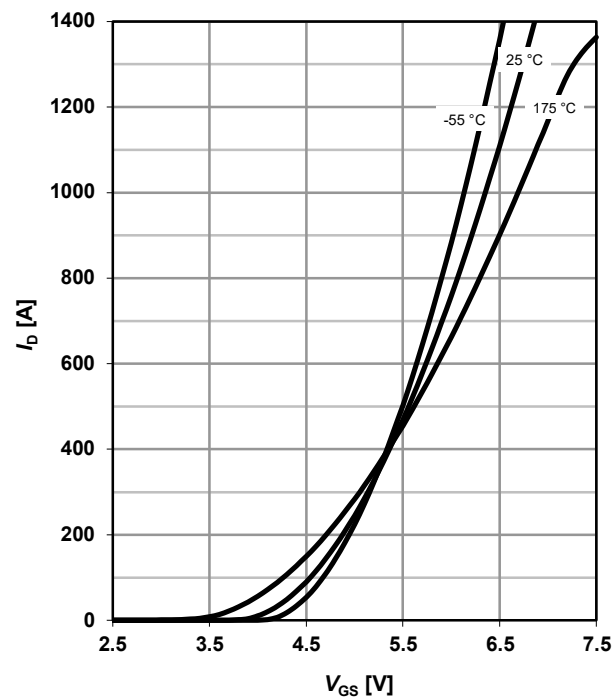
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



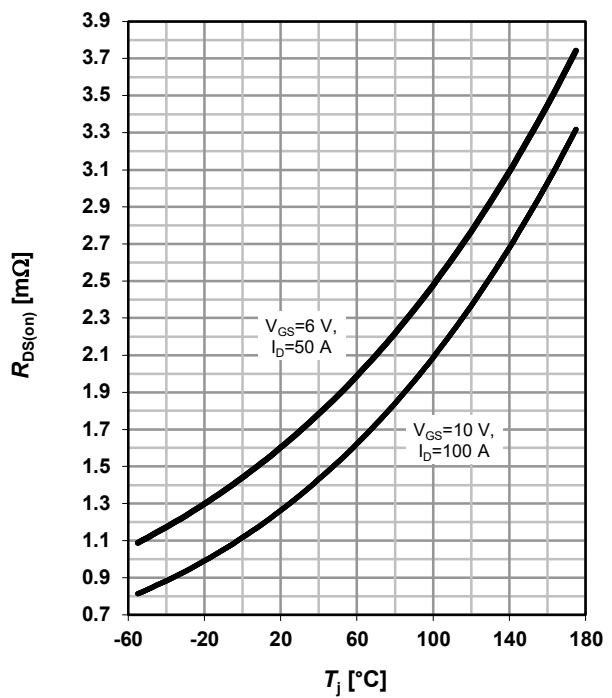
7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{V}; \text{parameter: } T_j$



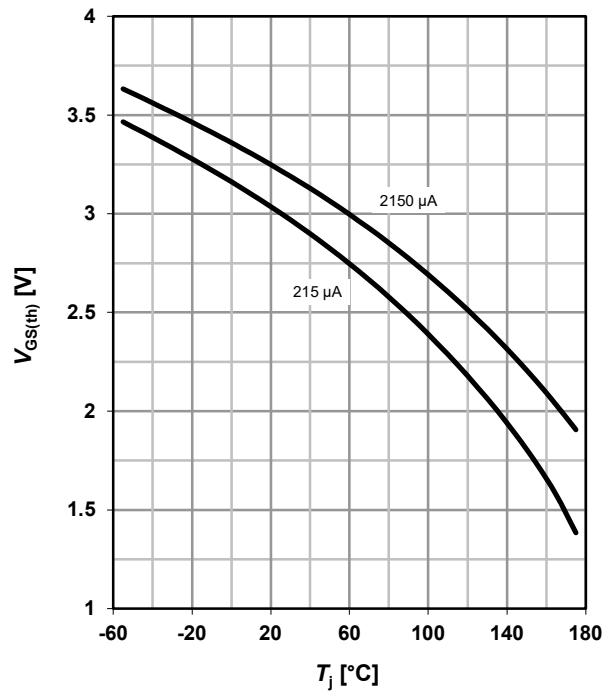
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); \text{parameter: } I_D, V_{GS}$



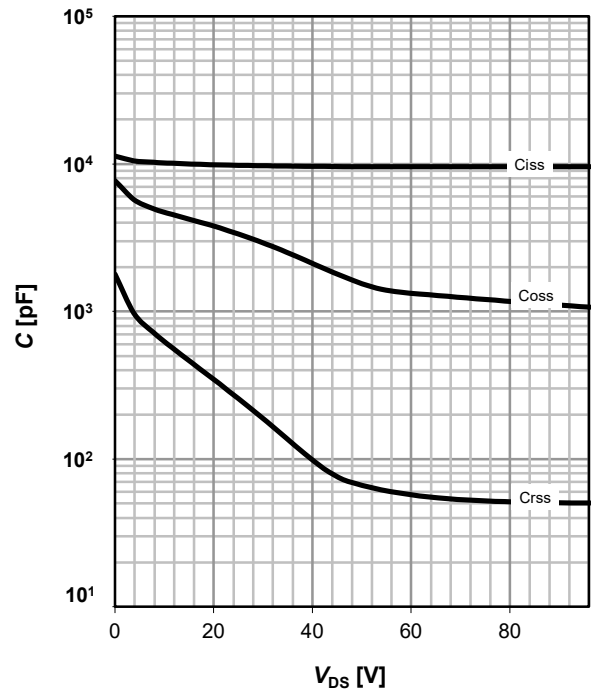
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



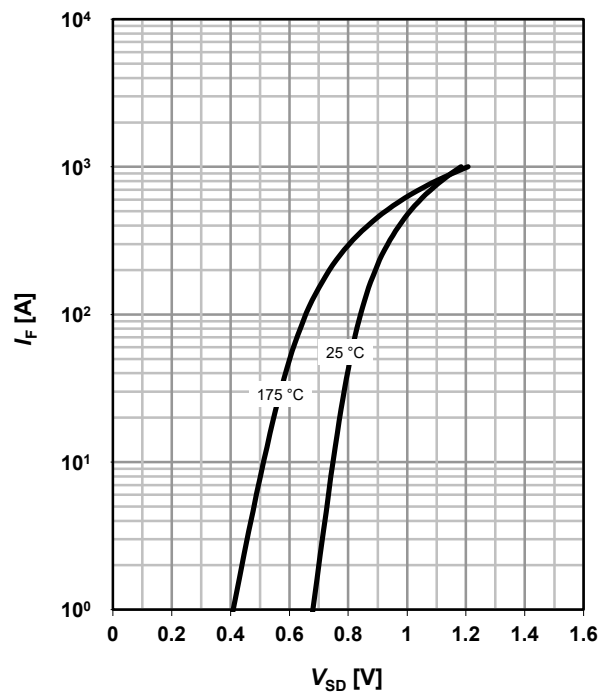
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



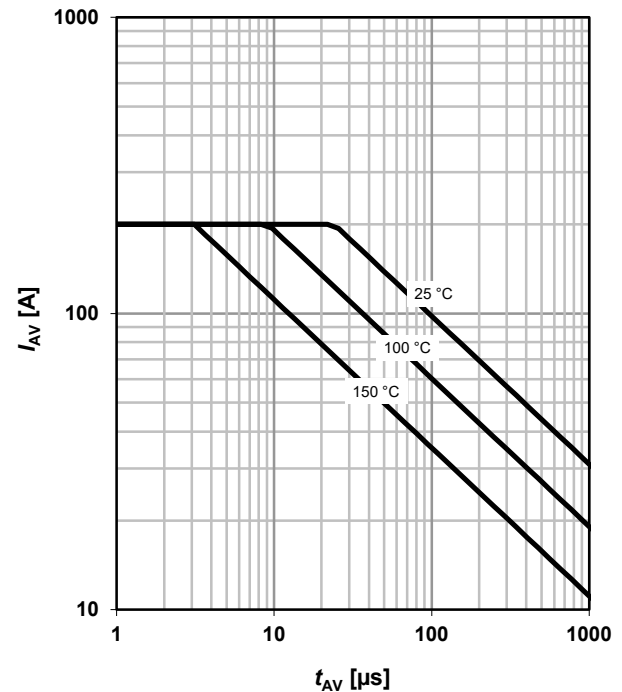
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



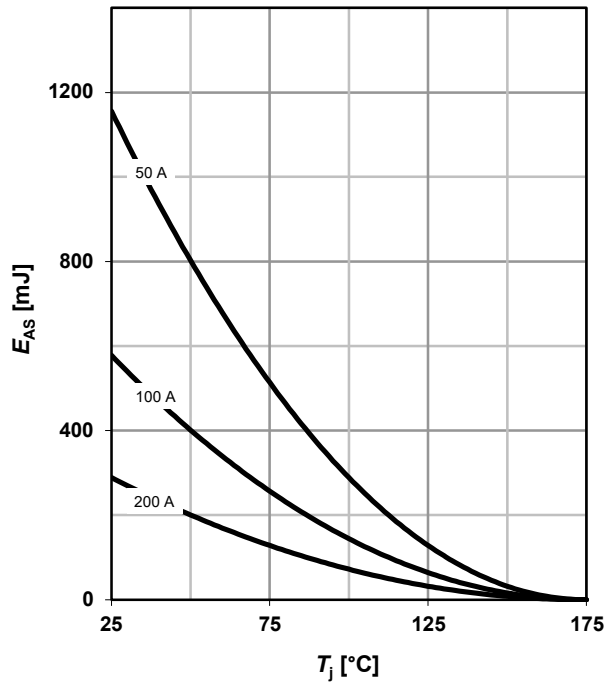
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



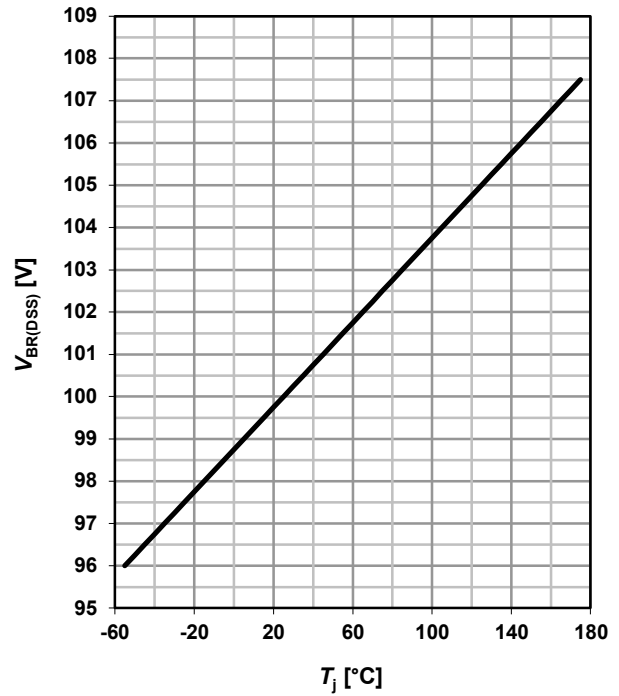
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



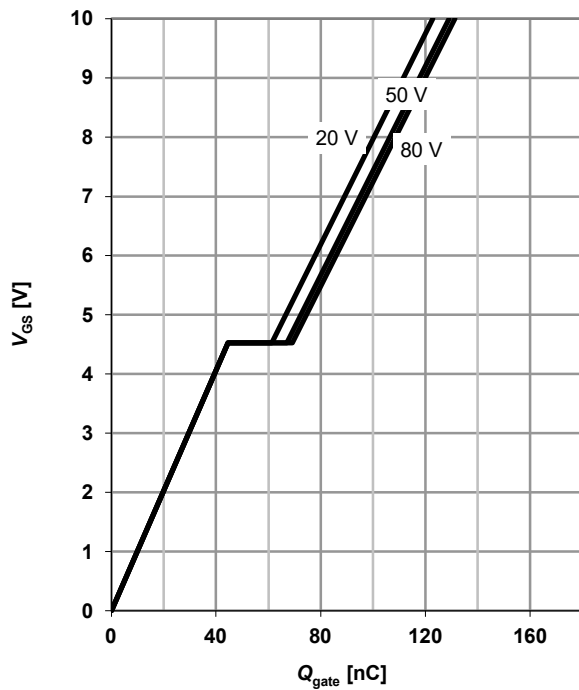
14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA

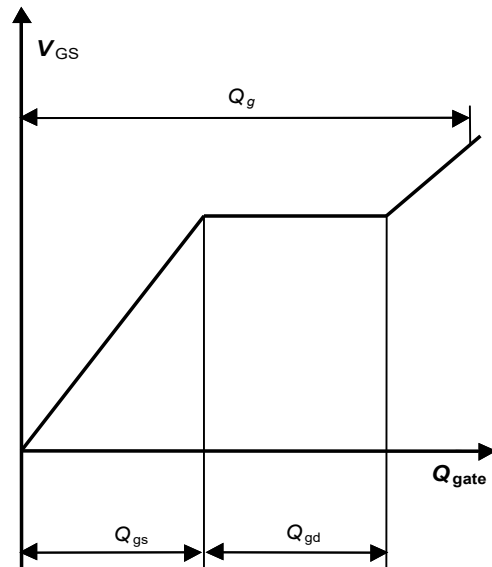


15 Typ. gate charge

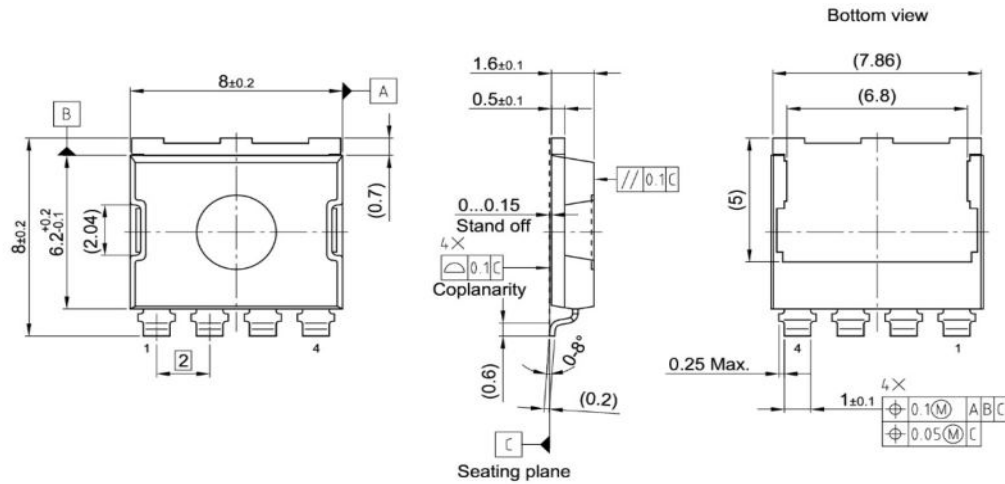
$V_{GS} = f(Q_{gate})$; $I_D = 100$ A pulsed; parameter: V_{DD}



16 Gate charge waveforms

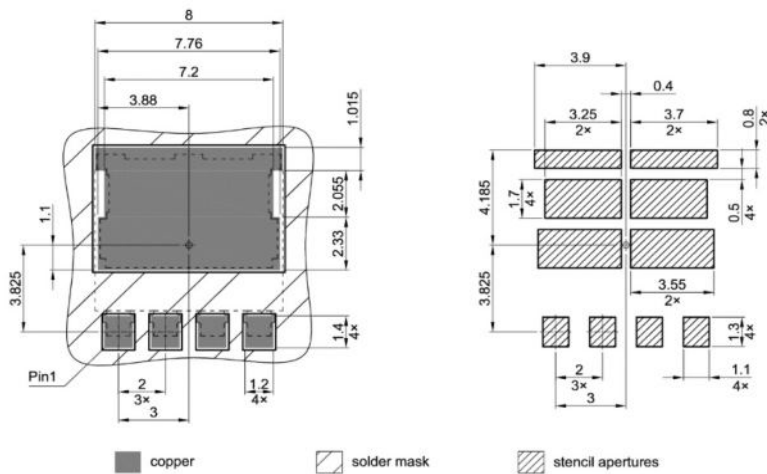


Package Outline



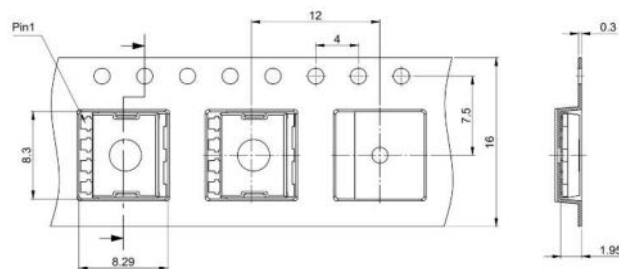
All dimensions are in units mm
 The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥] [⊕]
 Drawing according to ISO 8015, general tolerances ISO 2768-mK

Footprint



All dimensions are in units mm
 All pads are non-solder mask defined

Packaging



All dimensions are in units mm
 The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥] [⊕]

Revision History

Revision	Date	Changes
Revision 1.0	02.05.2024	Final data sheet

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