



IAUT165N08S5N029

OptiMOS™-5 Power-Transistor



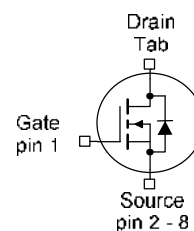
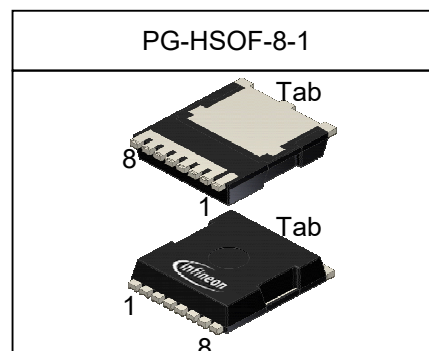
Features

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested

Type	Package	Marking
IAUT165N08S5N029	PG-HSOF-8-1	5N08029

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	2.9	mΩ
I_D	165	A



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}^{(1)}$	165	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{(2)}$	120	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	660	
Avalanche energy, single pulse ⁽²⁾	E_{AS}	$I_D=83\text{ A}$	225	mJ
Avalanche current, single pulse	I_{AS}	-	165	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	167	W
Operating and storage temperature	T_j , T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	0.9	K/W
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Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage ²⁾	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=108\text{ }\mu\text{A}$	2.2	3	3.8	
Zero gate voltage drain current ²⁾	I_{DSS}	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=85\text{ °C}^{2)}$	-	1	20	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6\text{ V}$, $I_D=40\text{ A}$	-	2.9	4.4	m Ω
		$V_{GS}=10\text{ V}$, $I_D=80\text{ A}$	-	2.4	2.9	



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	4900	6370	pF
Output capacitance	C_{oss}		-	790	1027	
Reverse transfer capacitance	C_{rss}		-	36	54	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=3.5\ \Omega$	-	13	-	ns
Rise time	t_r		-	9	-	
Turn-off delay time	$t_{d(off)}$		-	23	-	
Fall time	t_f		-	29	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	24	31	nC
Gate to drain charge	Q_{gd}		-	15	23	
Gate charge total	Q_g		-	70	90	
Gate plateau voltage	$V_{plateau}$		-	5.0	-	V

Reverse Diode

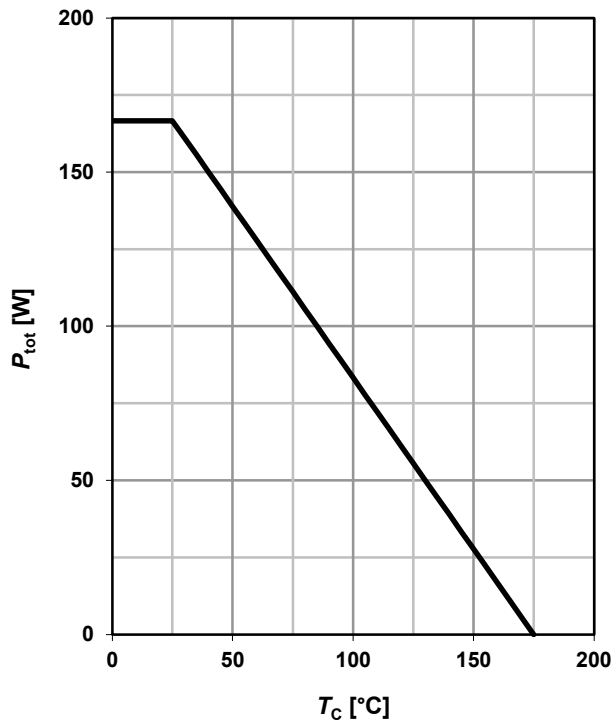
Diode continuous forward current ²⁾	I_S	$T_C=25\text{ °C}$	-	-	165	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	660	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=100\text{ A},$ $T_j=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time ²⁾	t_{rr}	$V_R=40\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	60	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	96	-	nC

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.9\text{ K/W}$ the chip is able to carry 171A at 25°C.

²⁾ Defined by design. Not subject to production test.

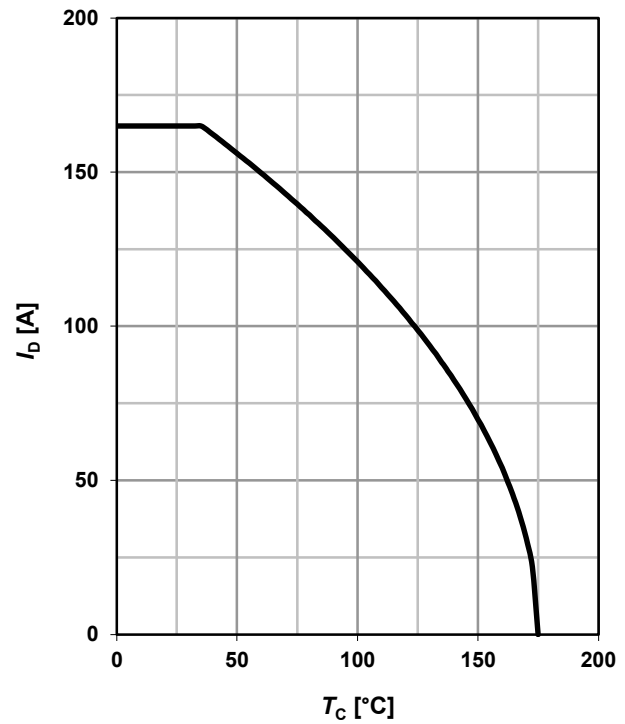
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

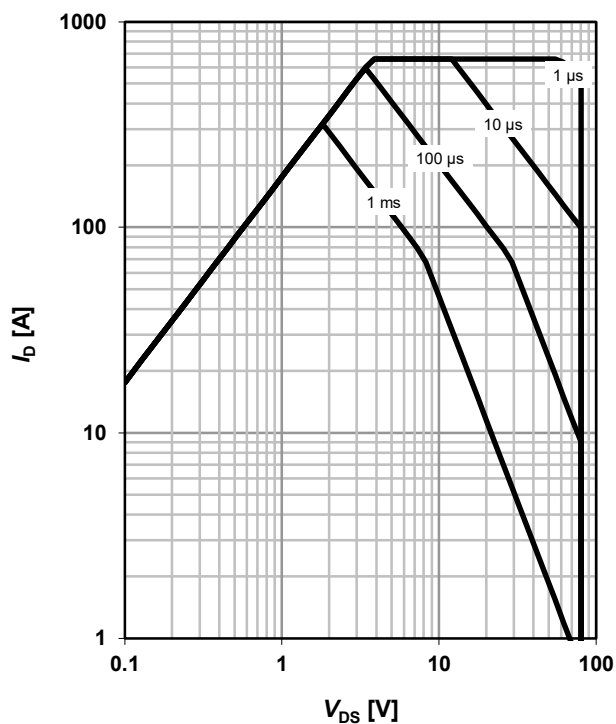
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

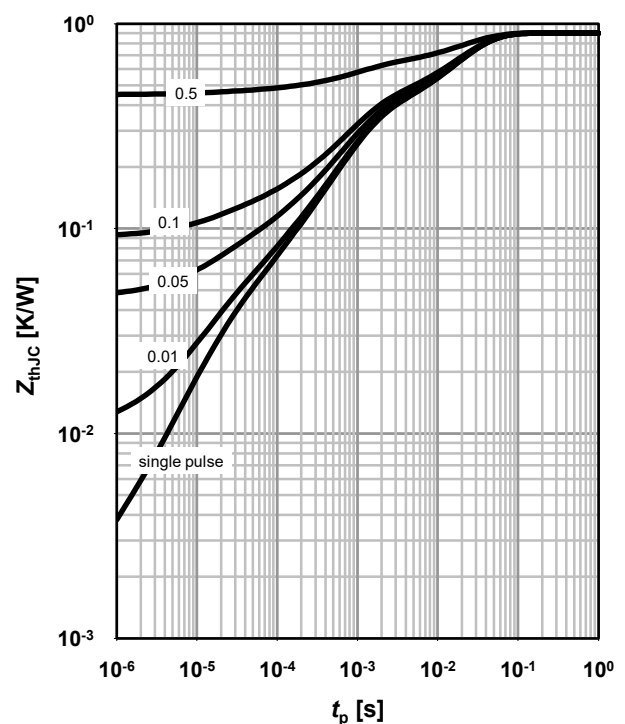
parameter: t_p

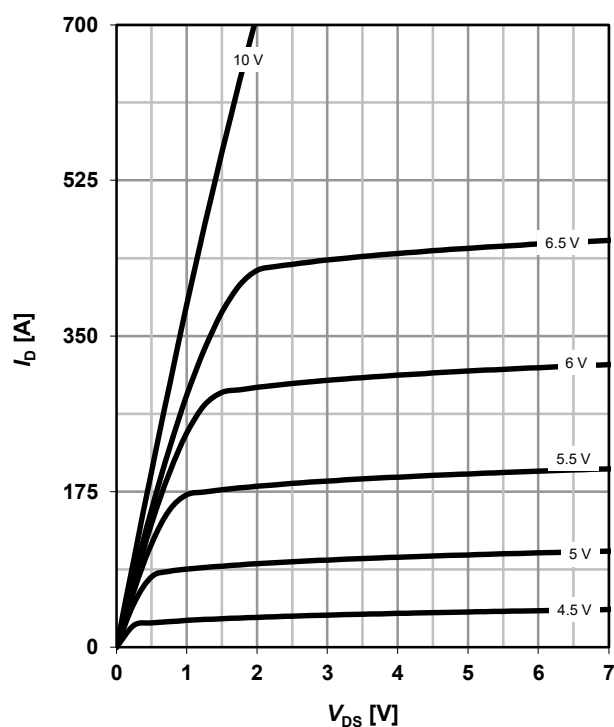
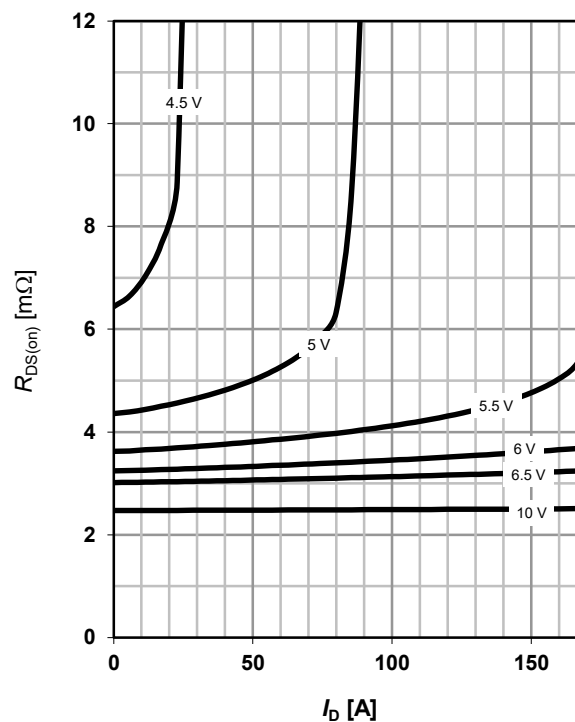
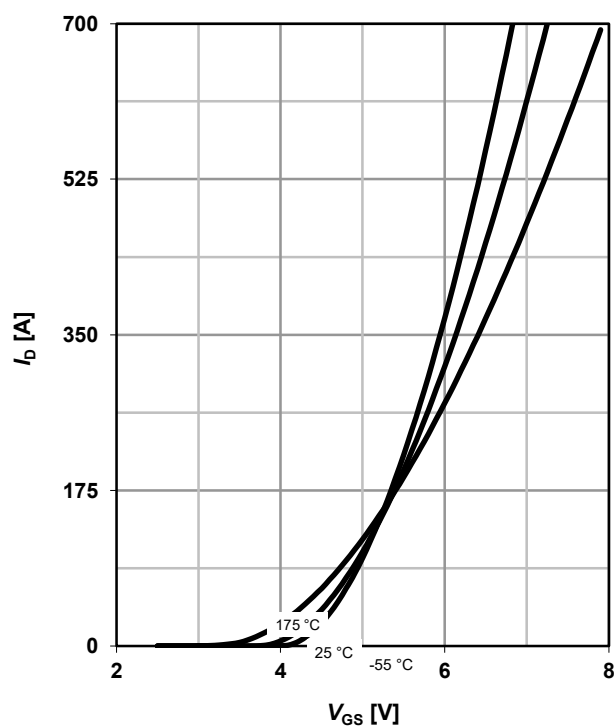
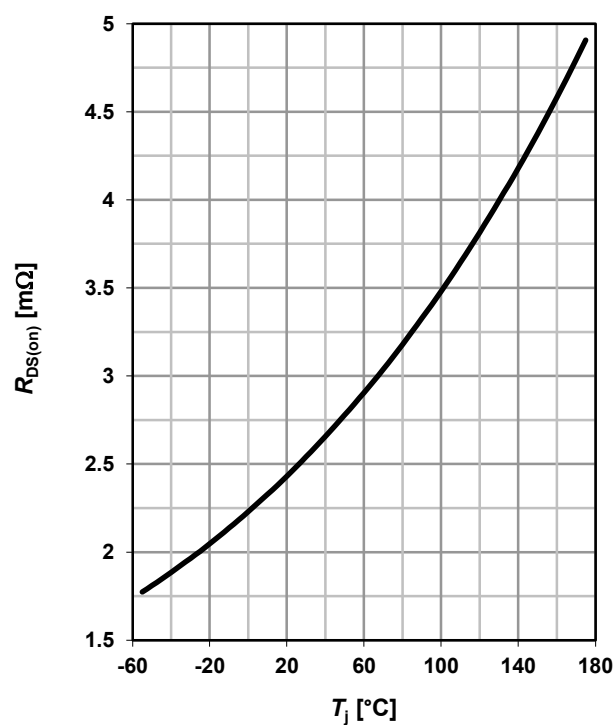


4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$

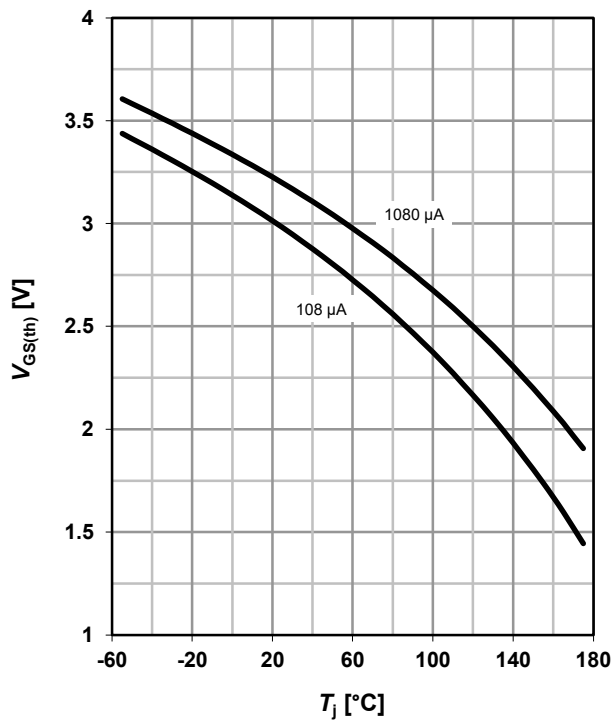


5 Typ. output characteristics
 $I_D = f(V_{DS}); T_j = 25\text{ °C}$
parameter: V_{GS} **6 Typ. drain-source on-state resistance**
 $R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$
parameter: V_{GS} **7 Typ. transfer characteristics**
 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$
parameter: T_j **8 Typ. drain-source on-state resistance**
 $R_{DS(on)} = f(T_j); I_D = 80\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

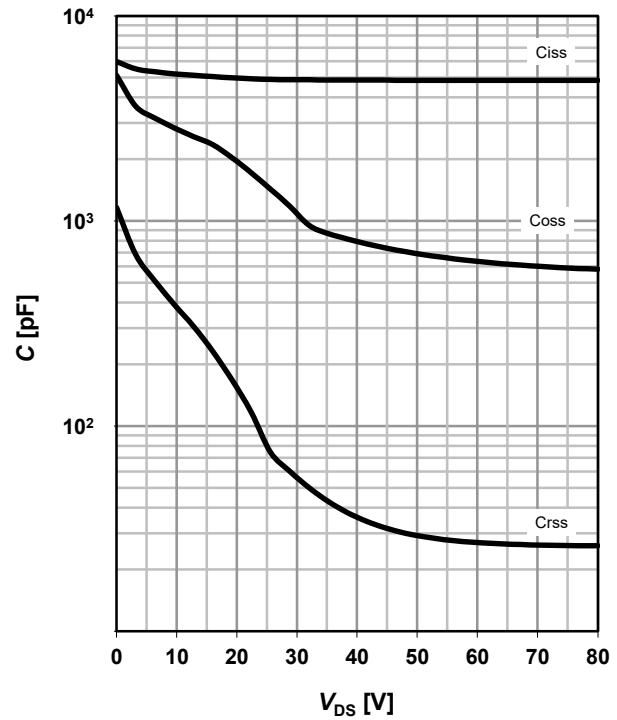
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

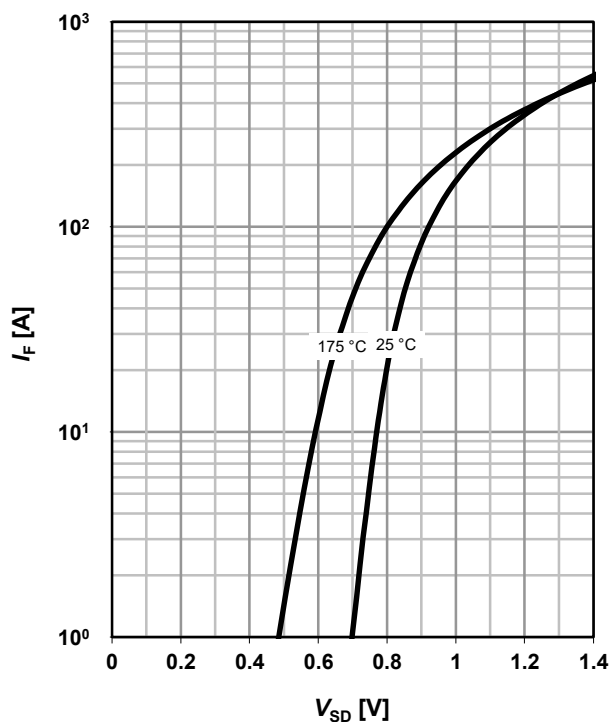
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

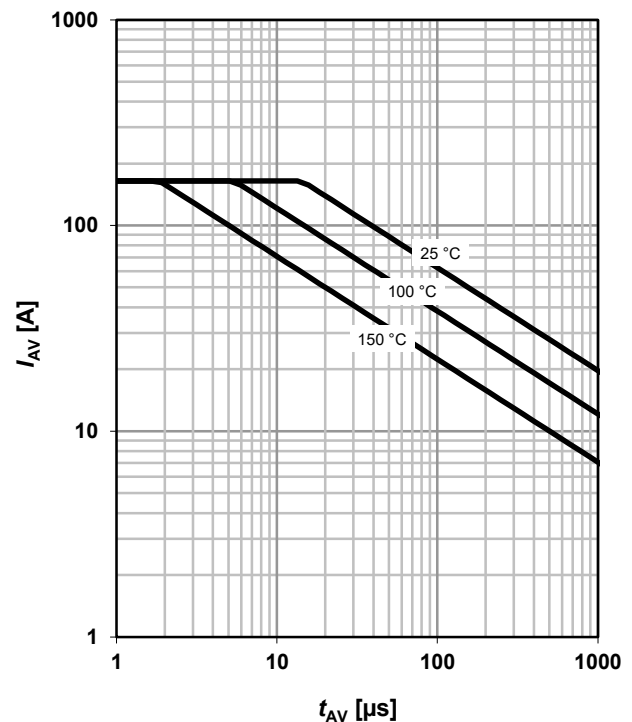
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$



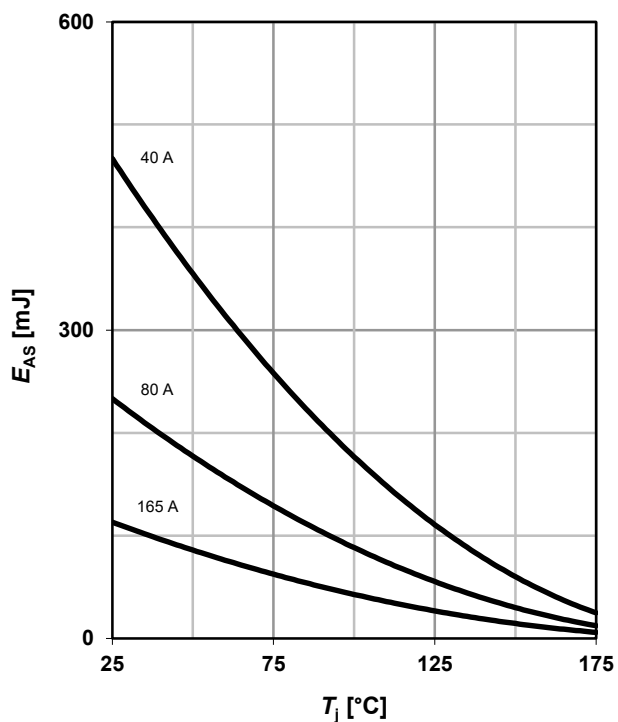


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13 Typical avalanche energy

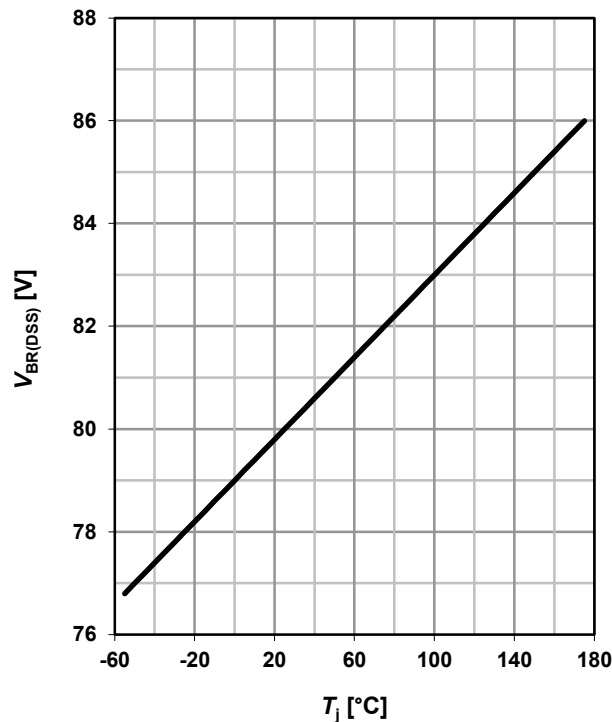
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

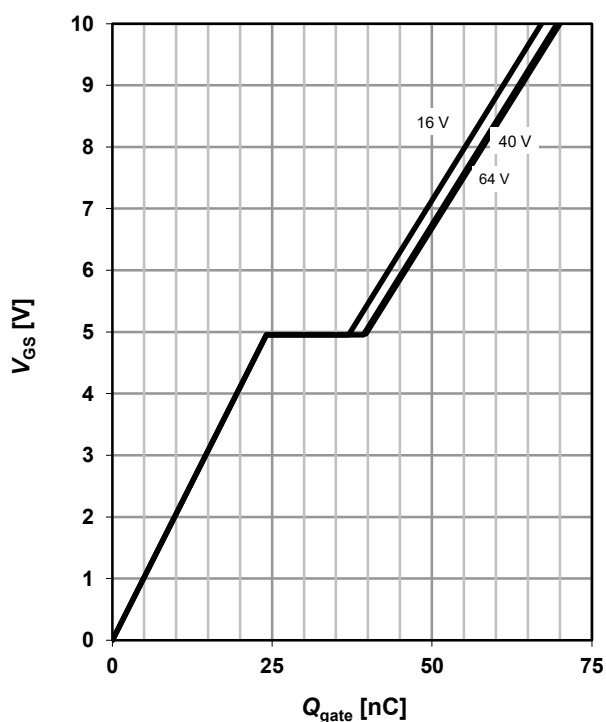
$$V_{BR(DSS)} = f(T_j); I_{D_typ} = 1 \text{ mA}$$



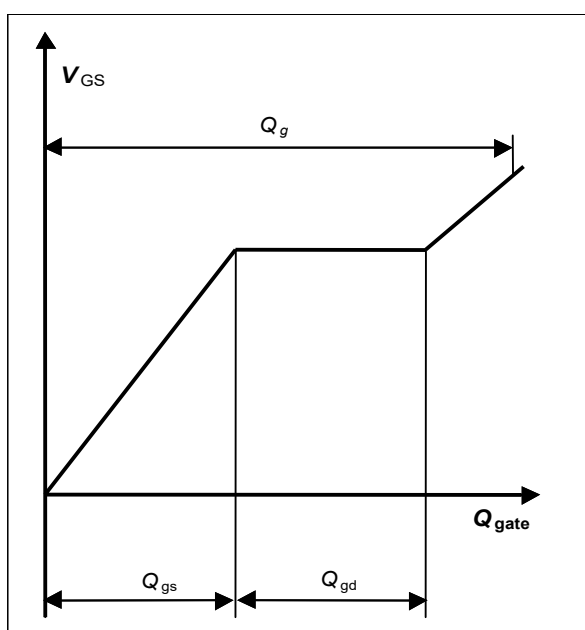
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 100 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Version 1.0	29.11.2016	Final Data Sheet
Version 1.1	26.04.2023	Clarified naming