



IAUZ20N08S5L300

OptiMOS™-5 Power-Transistor



Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Quality Features

- Infineon Automotive Quality
- Extended qualification beyond AEC Q101
- Enhanced testing
- Advanced adhesion against delamination
- Complementary testing for board level reliability

Advanced
adhesion

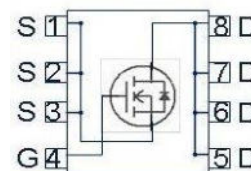
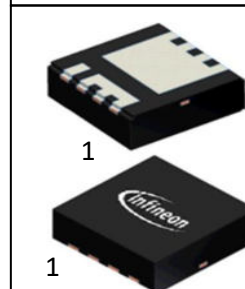
Robust

Enhanced
tested

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	30	mΩ
I_D	20	A

PG-TSDSON-8



Type	Package	Marking
IAUZ20N08S5L300	PG-TSDSON-8	5N8L300

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	20	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	14	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	80	
Avalanche energy, single pulse ¹⁾	E_{AS}	$I_D=10\text{ A}$	20	mJ
Avalanche current, single pulse	I_{AS}	-	10	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	30	W
Operating and storage temperature	T_J , T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics¹⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	5	K/W
Thermal resistance, junction - ambient ²⁾	R_{thJA}	-	-	40	-	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=8\text{ }\mu\text{A}$	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	-	1	μA
		$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=85\text{ °C}^{1)}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=10\text{ A}$	-	29.8	41.0	m Ω
		$V_{GS}=10\text{ V}, I_D=10\text{ A}$	-	22.4	30	
Gate resistance ¹⁾	R_G		-	0.9	-	Ω



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	461	599	pF
Output capacitance	C_{oss}		-	83	108	
Reverse transfer capacitance	C_{rss}		-	7.7	11.6	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=3.5\ \Omega$	-	2	-	ns
Rise time	t_r		-	1	-	
Turn-off delay time	$t_{d(off)}$		-	5	-	
Fall time	t_f		-	3	-	

Gate Charge characteristics¹⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=10\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	1.5	1.9	nC
Gate to drain charge	Q_{gd}		-	1.8	2.7	
Gate charge total	Q_g		-	8.1	10.5	
Gate plateau voltage	$V_{plateau}$		-	3.2	-	V

Reverse Diode

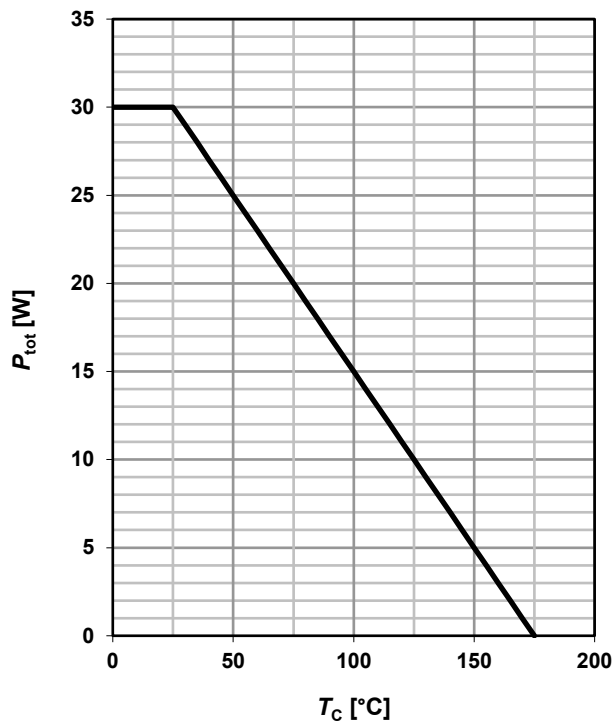
Diode continuous forward current ¹⁾	I_S	$T_C=25\text{ °C}$	-	-	20	A
Diode pulse current ¹⁾	$I_{S,pulse}$		-	-	43	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=10\text{ A},$ $T_J=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=40\text{ V}, I_F=20\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	29	-	ns
Reverse recovery charge ¹⁾	Q_{rr}		-	20	-	nC

¹⁾ The parameter is not subject to production test - verified by design/characterization.

²⁾ Device on four layer 2s2p PCB defined in accordance with JEDEC standards (JESD51-5-7).
PCB is vertical in still air.

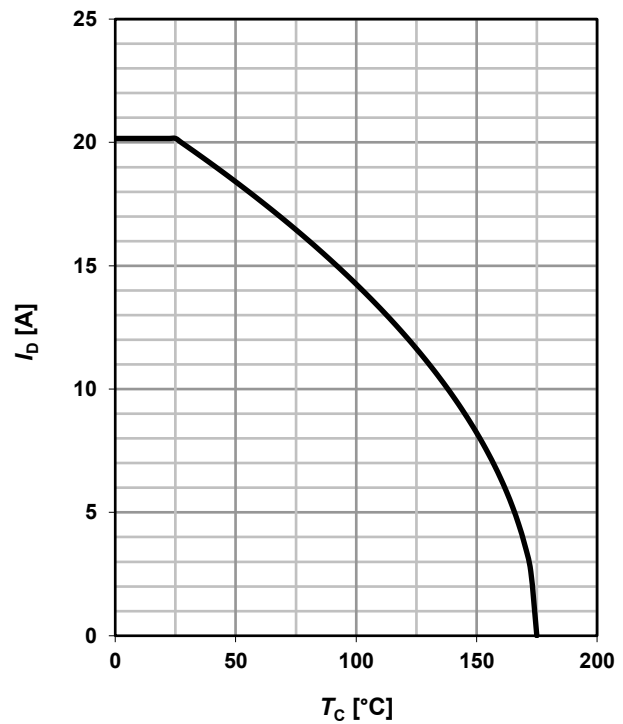
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

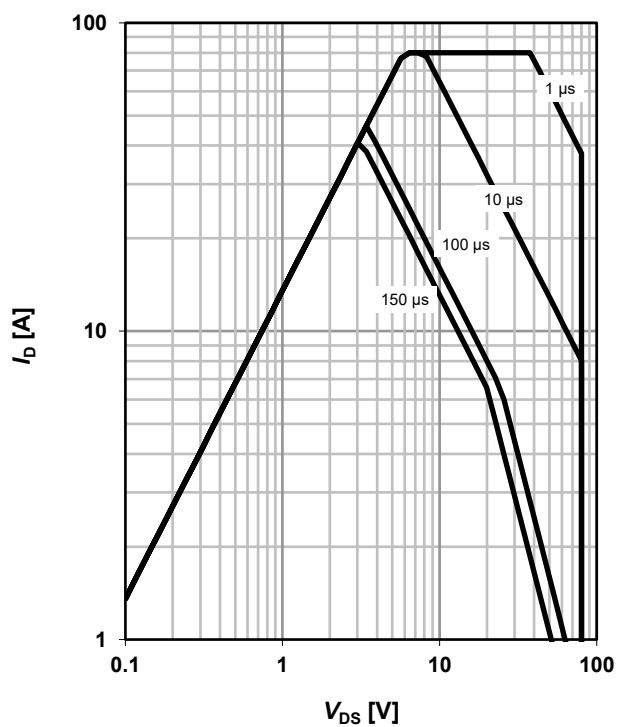
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

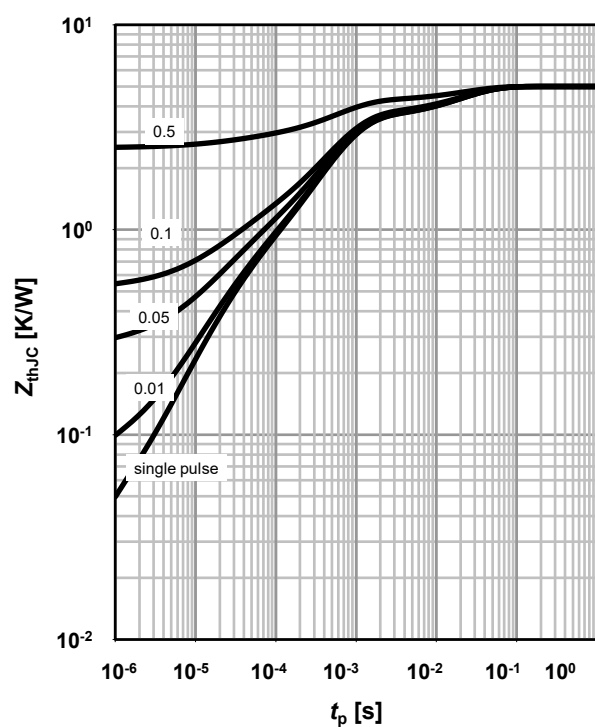
parameter: t_p

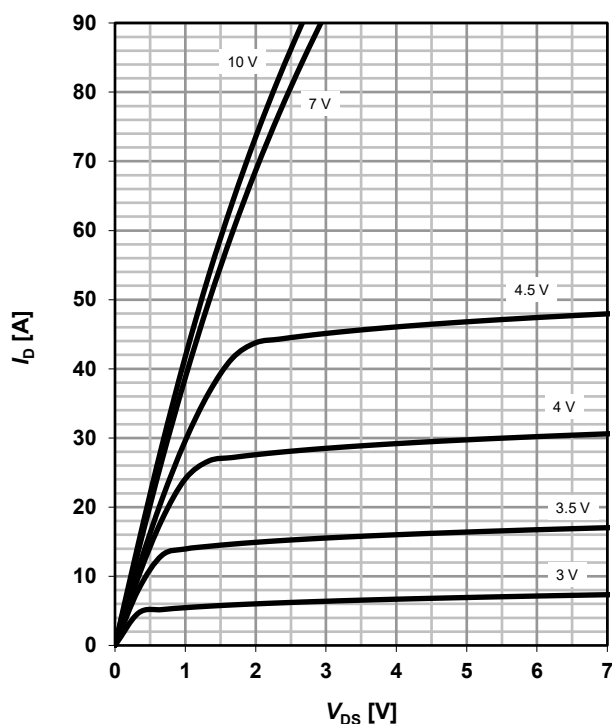
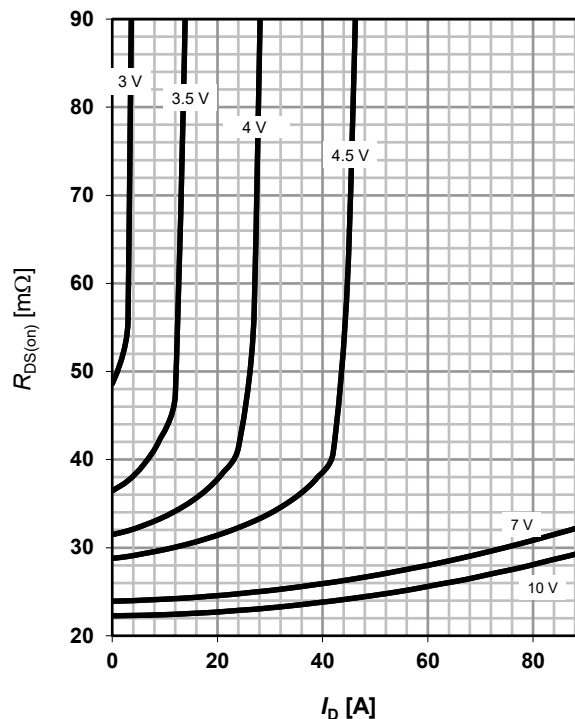
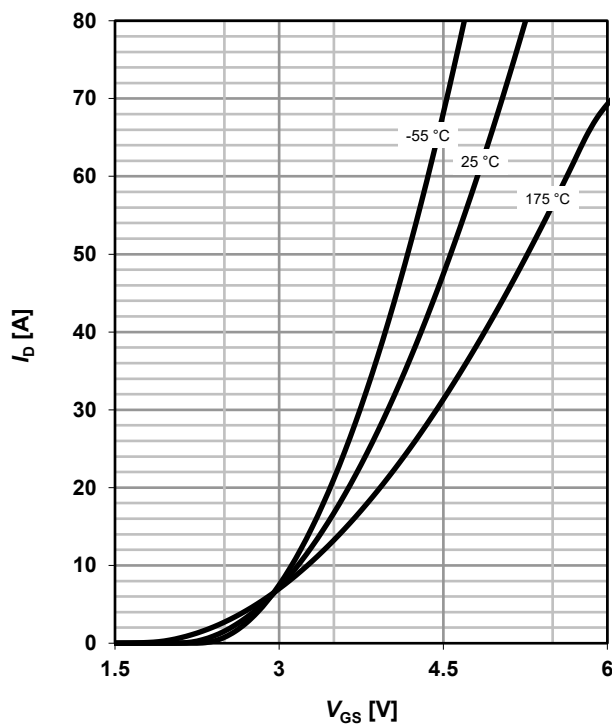
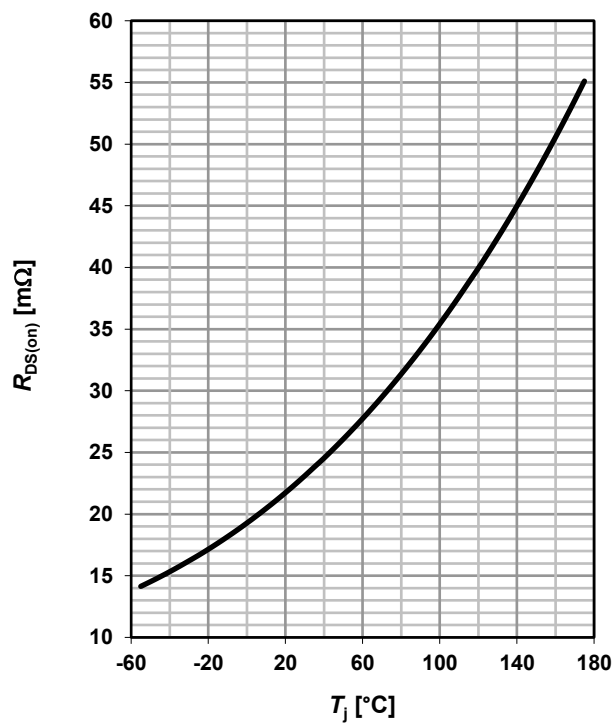


4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$

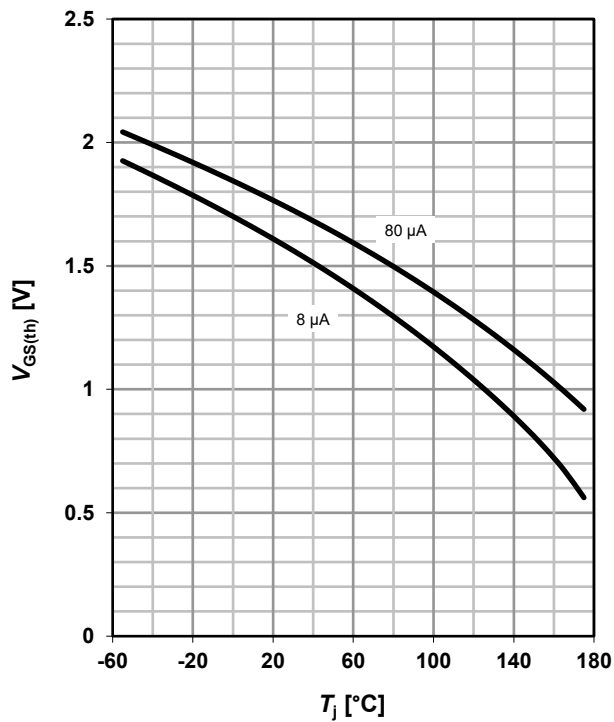


5 Typ. output characteristics
 $I_D = f(V_{DS}); T_j = 25\text{ °C}$
parameter: V_{GS} **6 Typ. drain-source on-state resistance**
 $R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$
parameter: V_{GS} **7 Typ. transfer characteristics**
 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$
parameter: T_j **8 Typ. drain-source on-state resistance**
 $R_{DS(on)} = f(T_j); I_D = 10\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

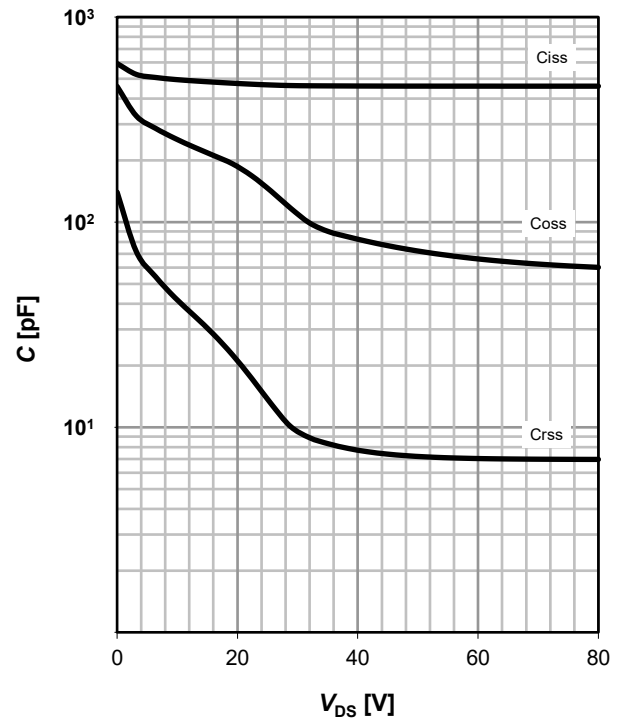
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

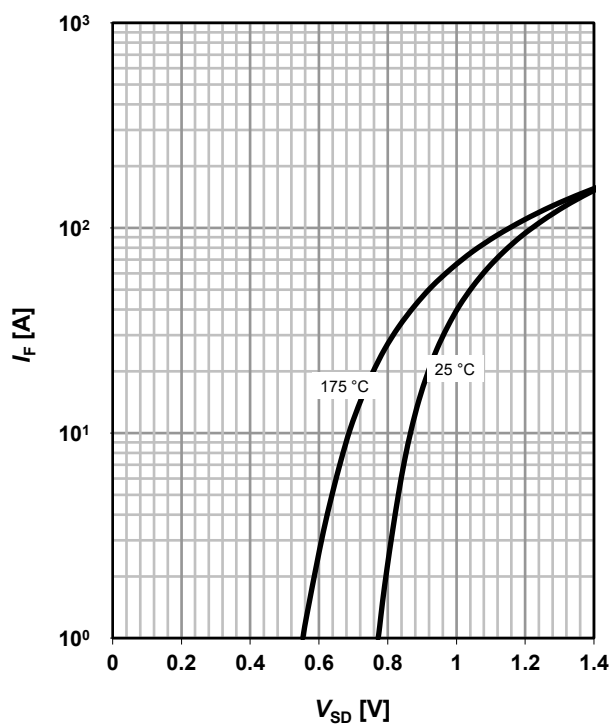
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

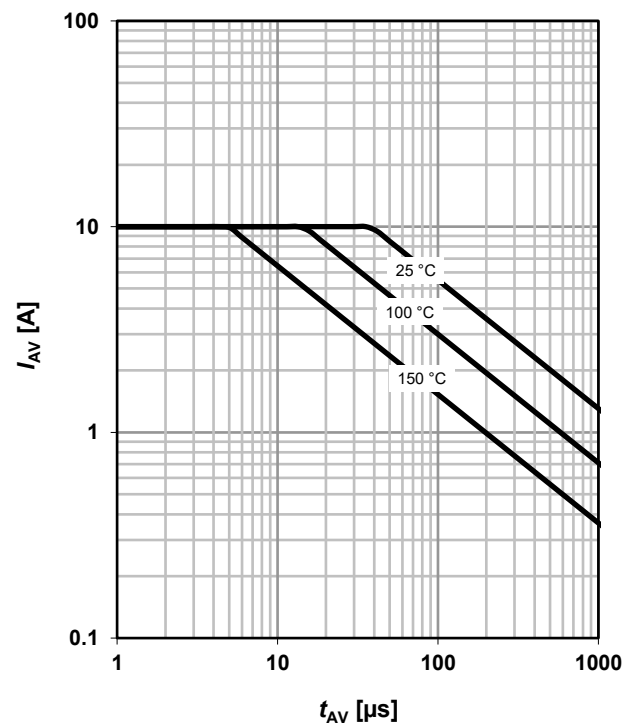
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$



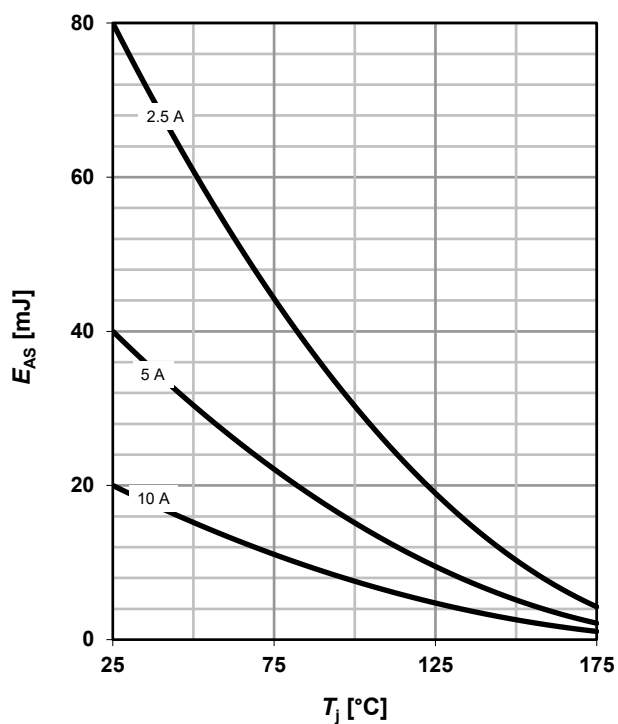


IAUZ20N08S5L300

13 Typical avalanche energy

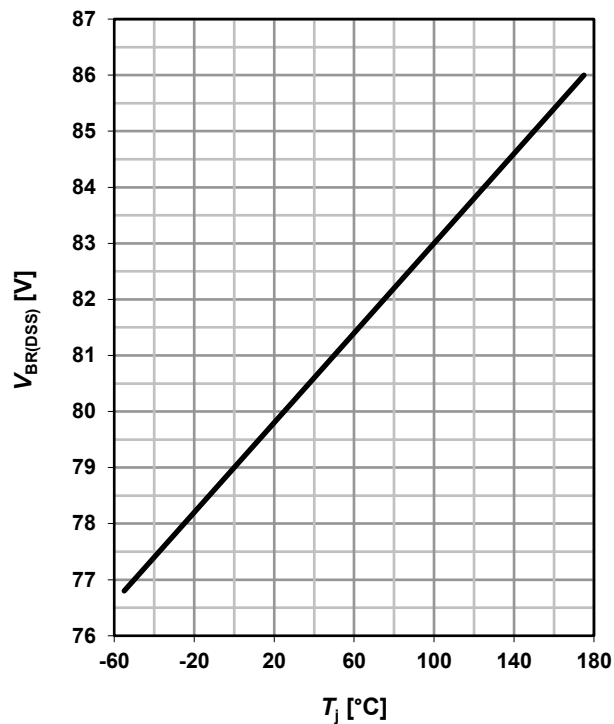
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

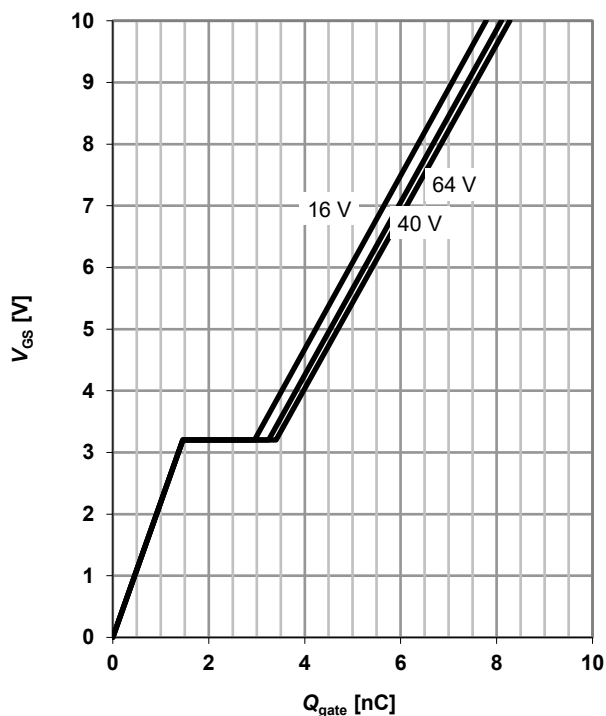
$$V_{BR(DSS)} = f(T_j); I_{D_typ} = 1 \text{ mA}$$



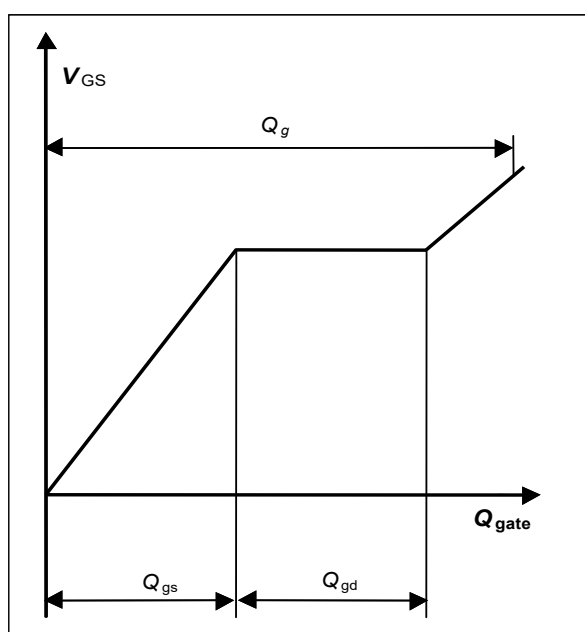
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 10 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



Technical drawing of a 3x3 LED array package showing top, side, and detail views with dimensions and tolerances.

Top View:

- Overall width: 3.3 ± 0.1
- Overall height: 3.3 ± 0.1
- Pin 1 Marking: Indicated by a circle and leader line.
- LED Array: 3x3 grid of LEDs.

Side View:

- Overall height: 1.85 ± 0.1
- LED Array Height: 0.25 ± 0.1
- Stand Off: $0 \dots 0.05$
- Pin Height: 0.1
- Pin Diameter: 0.05
- Pin Spacing: 1.15 MAX.

Detail View (LED Array):

- LED Array Width: 2.29 ± 0.1
- LED Array Height: 2.11 ± 0.1
- LED Array Pitch: 0.65
- LED Array Spacing: 0.34 ± 0.1
- LED Array Count: $3 \times 0.65 = 1.95$
- LED Array Pitch: 0.65
- LED Array Spacing: 0.34 ± 0.1
- LED Array Count: $3 \times 0.65 = 1.95$

Detail View (Pin):

- Pin Diameter: 0.05 MIN.
- Pin Length: 0.07 MIN.
- Pin Tip: $Z, 3x; \text{ LEAD TIP}$

Technical drawing of a rectangular plate with the following dimensions and features:

- Overall width: 8
- Overall height: 2
- Top edge thickness: 0.2
- Bottom edge thickness: 1.2
- Three circular holes along the top edge, each with a diameter of 0.6.
- Three rectangular cutouts along the bottom edge, each with a width of 3.6 and a height of 0.6.
- A dimension of 3.6 is indicated for the distance between the centers of the first and second rectangular cutouts.
- A dimension of 3.6 is indicated for the distance between the center of the second rectangular cutout and the center of the second circular hole.
- A dimension of 3.6 is indicated for the distance between the center of the third rectangular cutout and the center of the third circular hole.
- A feature labeled "PIN 1 INDEX MARKING" is shown on the first rectangular cutout.



Published by
Infineon Technologies AG
85579 Neubiberg, Germany

© Infineon Technologies AG 2019
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances.

For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life.

If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.