

OptiMOS™ -5 Power Transistor



RoHS

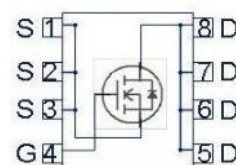
Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic level
- MSL1 up to 260°C peak reflow
- 175 °C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	60	V
$R_{DS(on),max}$	14	mΩ
I_D	30	A

PG-TSDSON-8-32



Type	Package	Marking
IAUZ30N06S5L140	PG-TSDSON-8-32	5N6L140

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	30	A
		$V_{GS}=10\text{ V}$, DC current	30	
		$T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,3)}	8	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$	85	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=15\text{ A}$	27	mJ
Avalanche current, single pulse	I_{AS}	-	30	A
Gate source voltage	V_{GS}	-	± 16	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	33	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	4.6	K/W
Thermal resistance, junction - ambient ³⁾	R_{thJA}	-	-	37.2	-	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=10\mu A$	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=60V, V_{GS}=0V, T_j=125^\circ\text{C}^{1)}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=16V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=15A$	-	16.3	19.6	$m\Omega$
		$V_{GS}=10V, I_D=15A$	-	11.2	14	
Gate resistance ²⁾	R_G	-	-	1.4	-	Ω



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=30V,$ $f=1MHz$	-	683	888	pF
Output capacitance	C_{oss}		-	136	177	
Reverse transfer capacitance	C_{rss}		-	10	15	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V,$ $I_D=15A, R_{G,ext}=3.5\Omega$	-	1.6	-	ns
Turn-off delay time	$t_{d(off)}$		-	4.1	-	
Rise time	t_r		-	1.0	-	
Fall time	t_f		-	1.8	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=30V, I_D=15A,$ $V_{GS}=0 \text{ to } 10V$	-	2.3	2.9	nC
Gate to drain charge	Q_{gd}		-	1.6	2.4	
Gate charge total	Q_g		-	9.4	12.2	
Gate plateau voltage	$V_{plateau}$		-	3.3	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	30	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25^\circ C, t_p=100 \mu s$	-	-	85	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=15A,$ $T_j=25^\circ C$	-	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=30V, I_F=30A,$ $di_F/dt=100A/\mu s$	-	26	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	18	-	nC

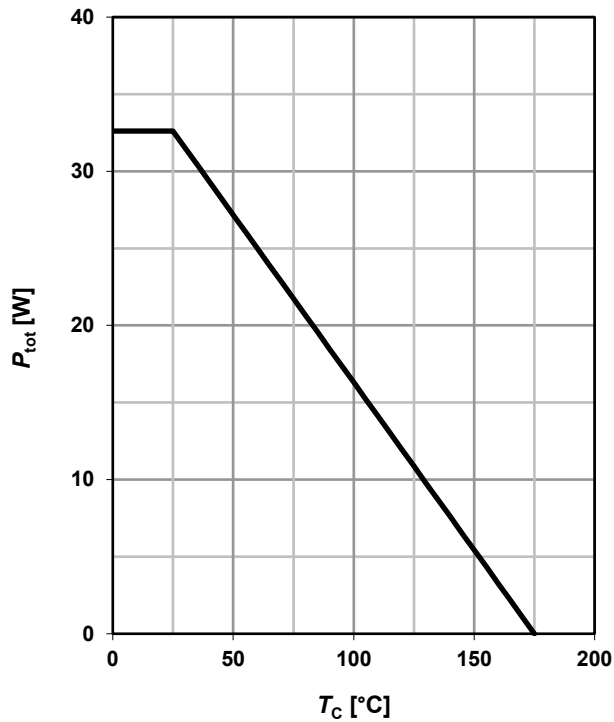
¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production test - verified by design/characterization.

³⁾ Device on a four-layer 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5-7). PCB is vertical in still air.

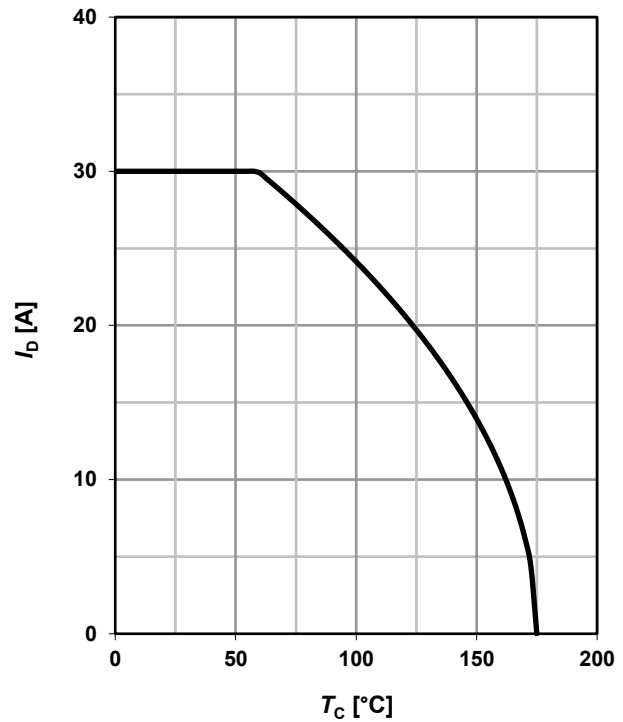
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



2 Drain current

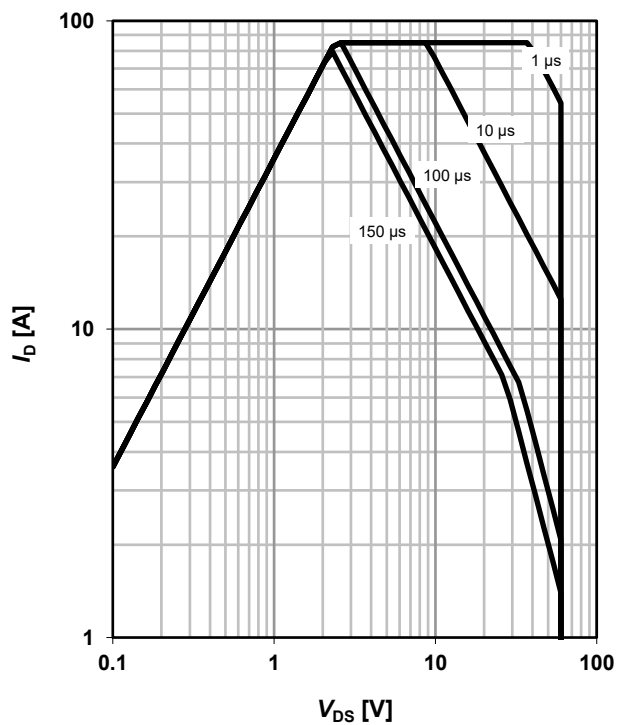
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

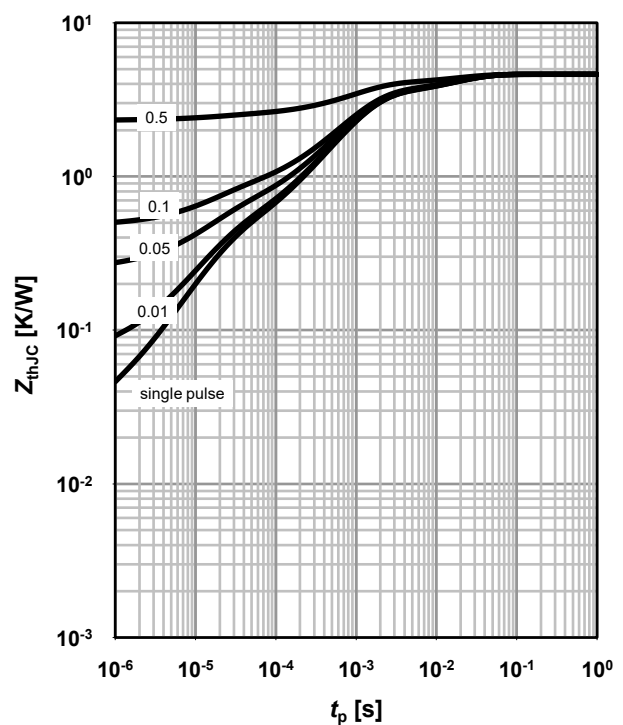
parameter: t_p

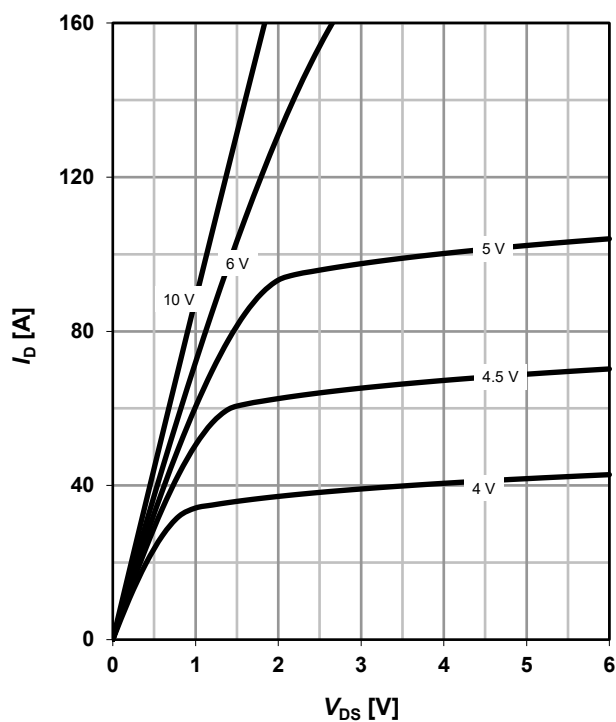
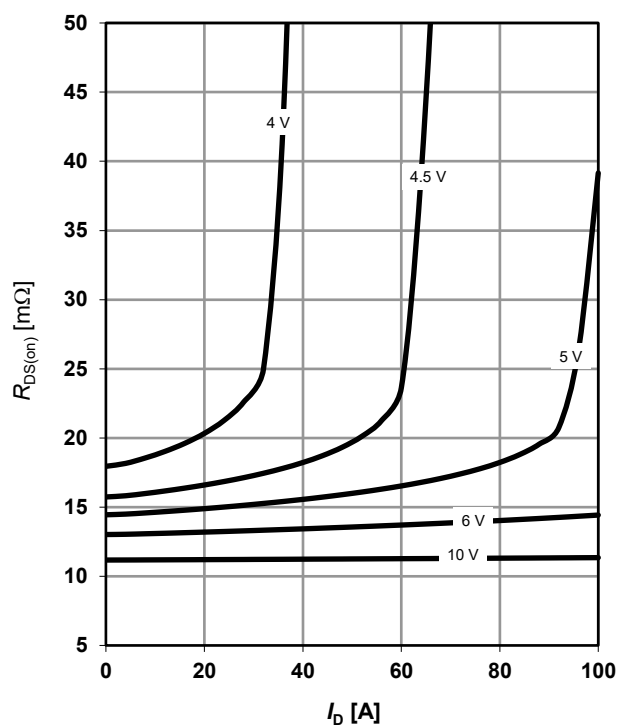
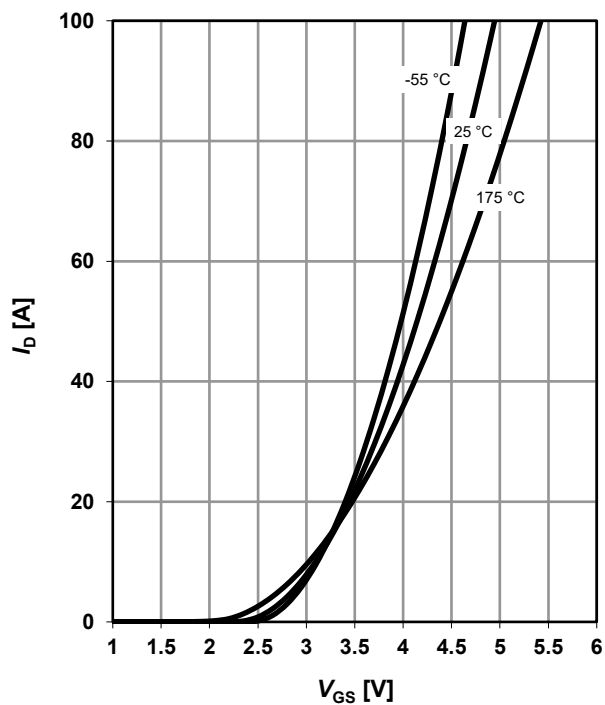
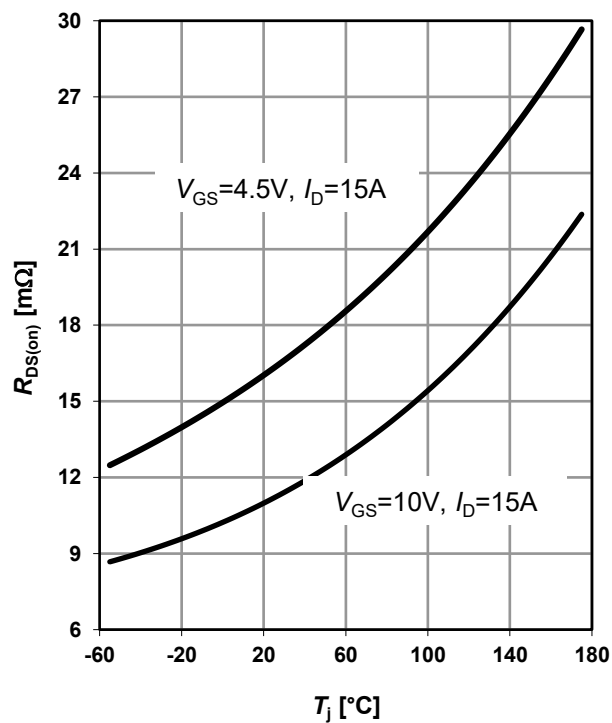


4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$

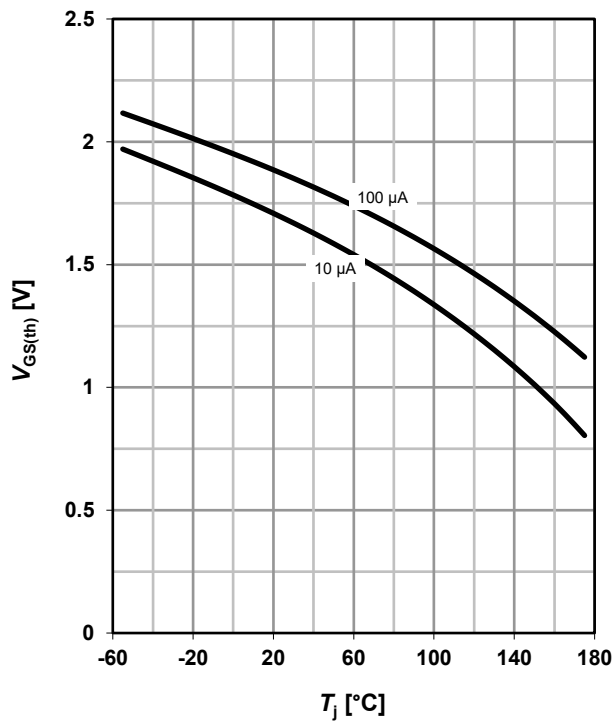


5 Typ. output characteristics
 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$
parameter: V_{GS} **6 Typ. drain-source on-state resistance**
 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$
parameter: V_{GS} **7 Typ. transfer characteristics**
 $I_D = f(V_{GS}); V_{DS} = 6\text{V}$
parameter: T_j **8 Typ. drain-source on-state resistance**
 $R_{DS(on)} = f(T_j);$
parameter: I_D, V_{GS} 

9 Typ. gate threshold voltage

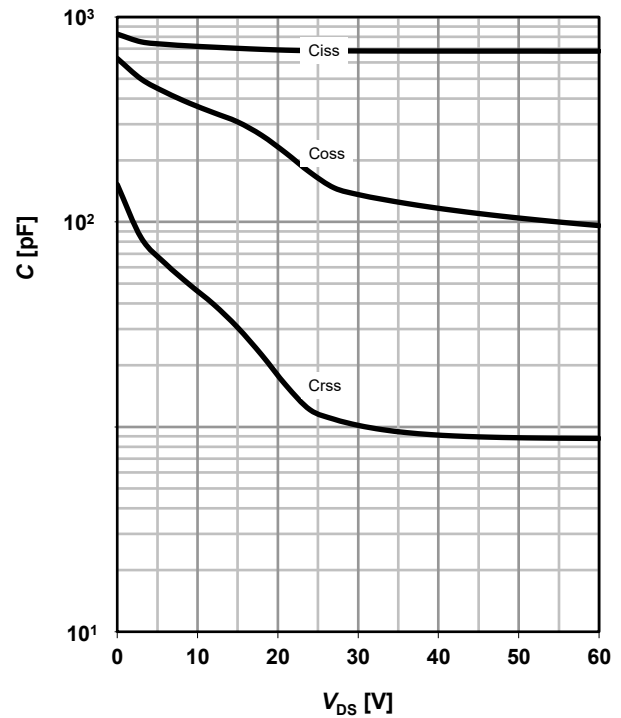
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

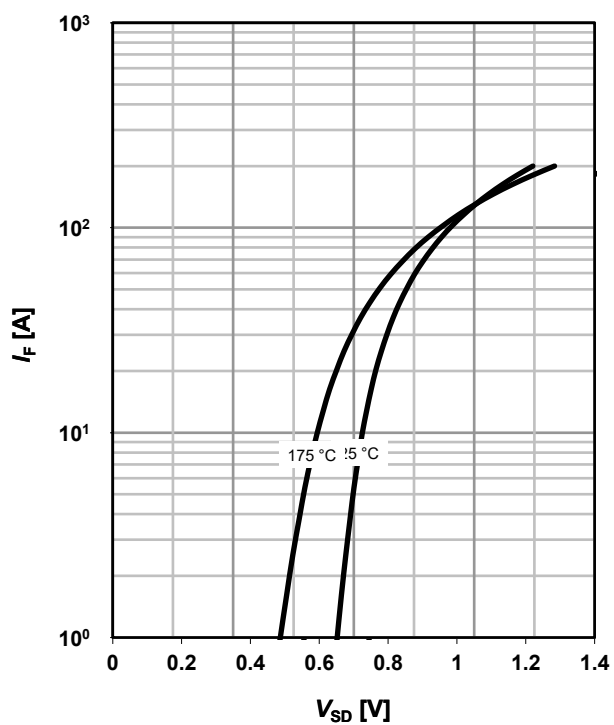
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

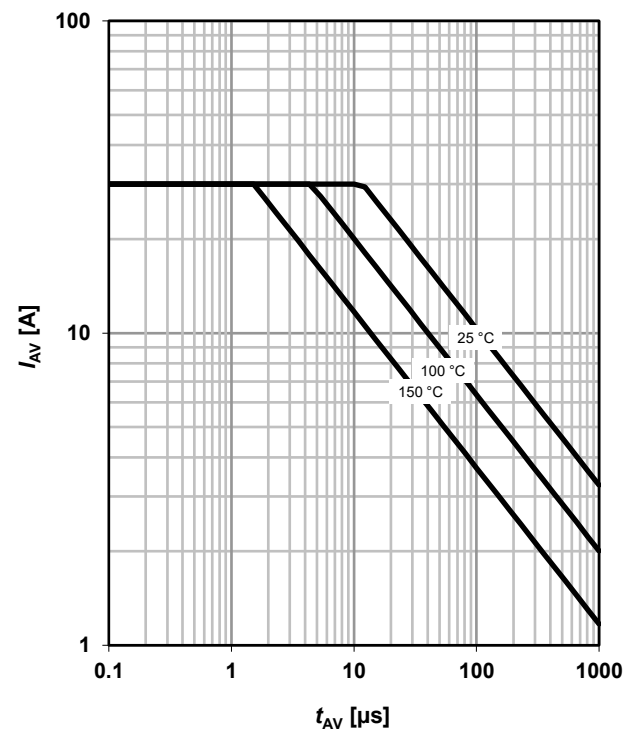
parameter: T_j



12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

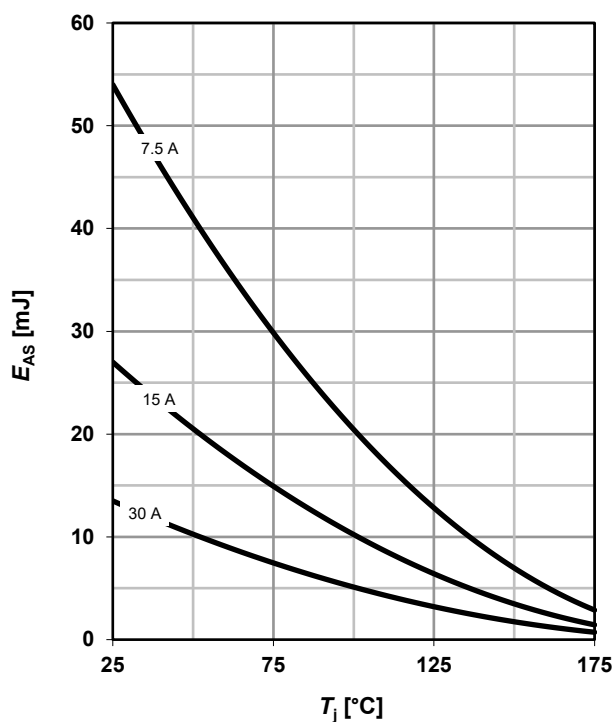
parameter: $T_{j(start)}$



13 Avalanche energy

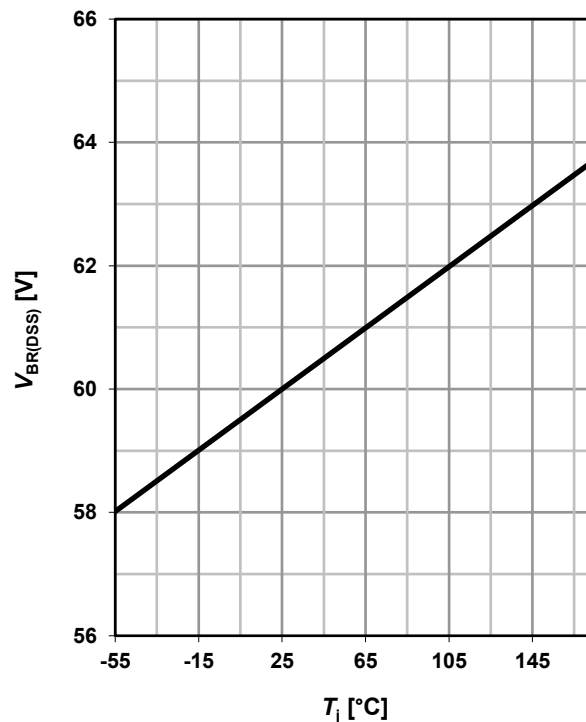
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

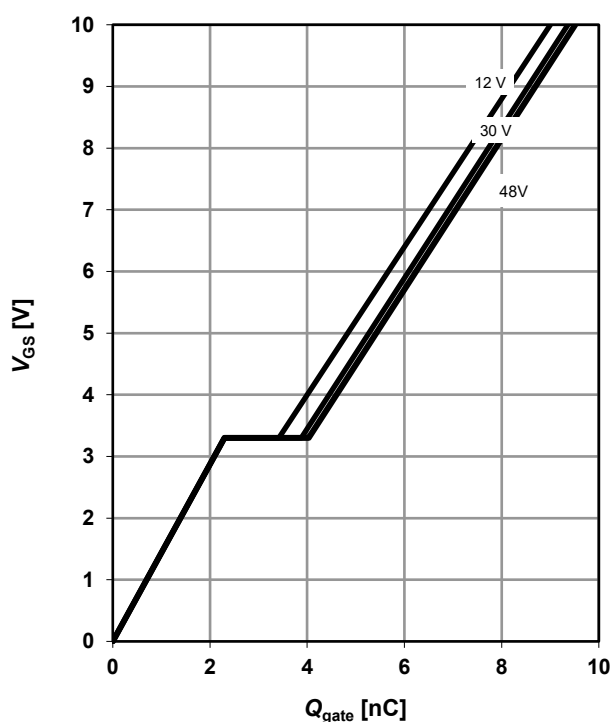
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



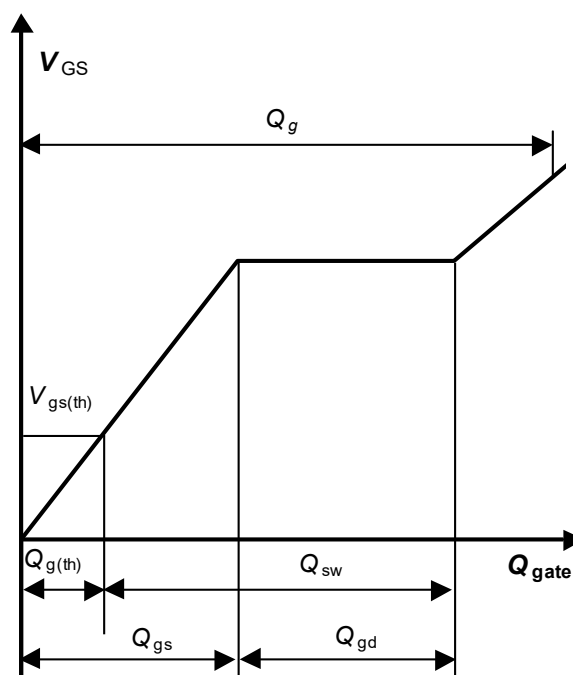
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 15 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



Technical drawing of a PCB showing top, bottom, and side views with dimensions and tolerances.

Top View: A square shape with dimensions 3.3 by 3.3.

Bottom View: A square shape with dimensions 2.29 by 2.11. It shows a central square area with a width of 0.4 and a height of 0.65. The bottom edge has a width of 0.65 and a height of 0.34. The bottom edge is labeled "Pin 1".

Side View: A cross-section showing the thickness of the PCB. The total thickness is 0.2. The top layer thickness is 0.05, and the bottom layer thickness is 0.00. The distance from the top layer to the bottom layer is 1. The distance from the bottom layer to the bottom edge is 0.07 Min.

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Infineon Technologies AG
81726 Munich, Germany

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Revision History

Version	Date	Changes
Revision 1.0	07.05.2020	Final Data Sheet
Revision 1.1	18.03.2021	Modified package outline and footprint