

Final datasheet
CoolSiC™ 1700 V SiC Trench MOSFET : Silicon Carbide MOSFET

Features

- $V_{DS} = 1700\text{ V}$ at $T_{vj} = 25^{\circ}\text{C}$
- $I_{DC} = 5.4\text{ A}$ at $T_C = 25^{\circ}\text{C}$
- $R_{DS(on)} = 1000\text{ m}\Omega$ at $V_{GS} = 12\text{ V}$, $T_{vj} = 25^{\circ}\text{C}$
- Optimized for fly-back topologies
- 12 V / 0 V gate-source voltage compatible with most fly-back controllers
- Very low switching losses
- Benchmark gate threshold voltage, $V_{GS(th)} = 4.5\text{ V}$
- Fully controllable dv/dt for EMI optimization
- .XT interconnection technology for best-in-class thermal performance

Potential applications

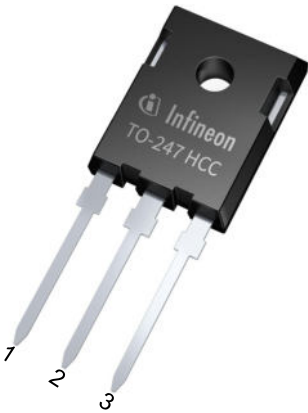
- General purpose drives (GPD)
- EV-Charging
- Energy Storage Systems (ESS)
- String inverter
- Uninterruptible power supplies

Product validation

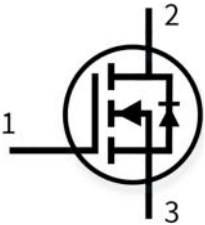
- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

- 1 – gate
2 – drain
3 – source



- Halogen-free
- Green
- Lead-free
- RoHS



Type	Package	Marking
IMWH170R1K0M1	PG-TO247-3-STD-NN4.8	170M11K0



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1 Package

1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Internal source inductance measured 5 mm (0.197 in.) from case	L_S			13		nH
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	wave soldering 1.6 mm (0.063 in.) from case for 10 s			260	°C
Mounting torque	M	M3 screw, Maximum of mounting processes: 3			0.6	Nm
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			1.64	2.13	K/W

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25\text{ °C}$		1700	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 12\text{ V}$	$T_c = 25\text{ °C}$	5.4	A
			$T_c = 100\text{ °C}$	3.8	
Peak drain current, t_p limited by $T_{vj(max)}$	I_{DM}	$V_{GS} = 12\text{ V}$		13.7	A
Gate-source voltage, max. transient voltage ¹⁾	V_{GS}	$t_p \leq 0.5\text{ }\mu\text{s}$, $D < 0.01$		-10/20	V
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25\text{ °C}$	70	W
			$T_c = 100\text{ °C}$	35	

1) Important note: The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		12...15	V
Recommended turn-off gate voltage	$V_{GS(off)}$		0	V

Table 4 **Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	$I_D = 1 \text{ A}$	$T_{vj} = 25 \text{ °C}$, $V_{GS(on)} = 12 \text{ V}$		1000		mΩ
			$T_{vj} = 100 \text{ °C}$, $V_{GS(on)} = 12 \text{ V}$		1416		
			$T_{vj} = 175 \text{ °C}$, $V_{GS(on)} = 12 \text{ V}$		2037		
			$T_{vj} = 25 \text{ °C}$, $V_{GS(on)} = 15 \text{ V}$		809	880	
Gate-source threshold voltage	$V_{GS(th)}$	$I_D = 1.2 \text{ mA}$, $V_{DS} = V_{GS}$ (tested after 1 ms pulse at $V_{GS} = 20 \text{ V}$)	$T_{vj} = 25 \text{ °C}$	3.5	4.5	5.7	V
			$T_{vj} = 175 \text{ °C}$		3.6		
Zero gate-voltage drain current	I_{DSS}	$V_{DS} = 1700 \text{ V}$, $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ °C}$		0.4	11	μA
			$T_{vj} = 175 \text{ °C}$		6		
Gate leakage current	I_{GSS}	$V_{DS} = 0 \text{ V}$	$V_{GS} = 20 \text{ V}$			100	nA
			$V_{GS} = -10 \text{ V}$			-100	
Forward transconductance	g_{fs}	$I_D = 1 \text{ A}$, $V_{DS} = 20 \text{ V}$			0.42		S
Internal gate resistance	$R_{G,int}$	$f = 1 \text{ MHz}$, $V_{AC} = 25 \text{ mV}$			35		Ω
Input capacitance	C_{iss}	$V_{DD} = 1000 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 100 \text{ kHz}$, $V_{AC} = 25 \text{ mV}$			233		pF
Output capacitance	C_{oss}	$V_{DD} = 1000 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 100 \text{ kHz}$, $V_{AC} = 25 \text{ mV}$			10		pF
Reverse transfer capacitance	C_{rss}	$V_{DD} = 1000 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 100 \text{ kHz}$, $V_{AC} = 25 \text{ mV}$			0.8		pF
C_{oss} stored energy	E_{oss}	$V_{DD} = 1000 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 100 \text{ kHz}$, $V_{AC} = 25 \text{ mV}$			1.8		μJ
Total gate charge	Q_G	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, turn-on pulse			5.5		nC
Plateau gate charge	$Q_{GS(pl)}$	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, turn-on pulse			2		nC
Gate-to-drain charge	Q_{GD}	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, turn-on pulse			1.4		nC
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, $R_{G,ext} = 6.9 \text{ Ω}$, $L_\sigma = 40 \text{ nH}$, diode: body diode at $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ °C}$		15		ns
			$T_{vj} = 175 \text{ °C}$		13		

(table continues...)

Table 4 (continued) **Characteristic values**

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Rise time	t_r	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, $R_{G,ext} = 6.9 \text{ } \Omega$, $L_\sigma = 40 \text{ nH}$, diode: body diode at $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ } ^\circ\text{C}$	9		ns
			$T_{vj} = 175 \text{ } ^\circ\text{C}$	8		
Turn-off delay time	$t_{d(off)}$	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, $R_{G,ext} = 6.9 \text{ } \Omega$, $L_\sigma = 40 \text{ nH}$, diode: body diode at $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ } ^\circ\text{C}$	19		ns
			$T_{vj} = 175 \text{ } ^\circ\text{C}$	21		
Fall time	t_f	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, $R_{G,ext} = 6.9 \text{ } \Omega$, $L_\sigma = 40 \text{ nH}$, diode: body diode at $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ } ^\circ\text{C}$	23		ns
			$T_{vj} = 175 \text{ } ^\circ\text{C}$	23		
Turn-on energy	E_{on}	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, $R_{G,ext} = 6.9 \text{ } \Omega$, $L_\sigma = 40 \text{ nH}$, diode: body diode at $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ } ^\circ\text{C}$	48		μJ
			$T_{vj} = 175 \text{ } ^\circ\text{C}$	51		
Turn-off energy	E_{off}	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, $R_{G,ext} = 6.9 \text{ } \Omega$, $L_\sigma = 40 \text{ nH}$, diode: body diode at $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ } ^\circ\text{C}$	13		μJ
			$T_{vj} = 175 \text{ } ^\circ\text{C}$	15		
Total switching energy	E_{tot}	$V_{DD} = 1000 \text{ V}$, $I_D = 1 \text{ A}$, $V_{GS} = 0/12 \text{ V}$, $R_{G,ext} = 6.9 \text{ } \Omega$, $L_\sigma = 40 \text{ nH}$, diode: body diode at $V_{GS} = 0 \text{ V}$	$T_{vj} = 25 \text{ } ^\circ\text{C}$	61		μJ
			$T_{vj} = 175 \text{ } ^\circ\text{C}$	66		
Virtual junction temperature	T_{vj}		-55		175	$^\circ\text{C}$

Note: For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

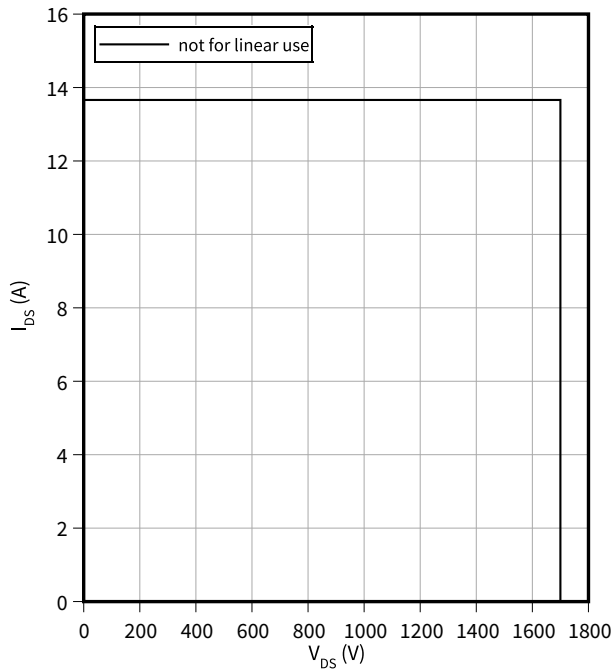
The chip technology was characterized up to 200 kV/ μs . The measured dV/dt was limited by measurement test setup and package.

Dynamic test circuit see Fig. F.

3 Characteristics diagrams

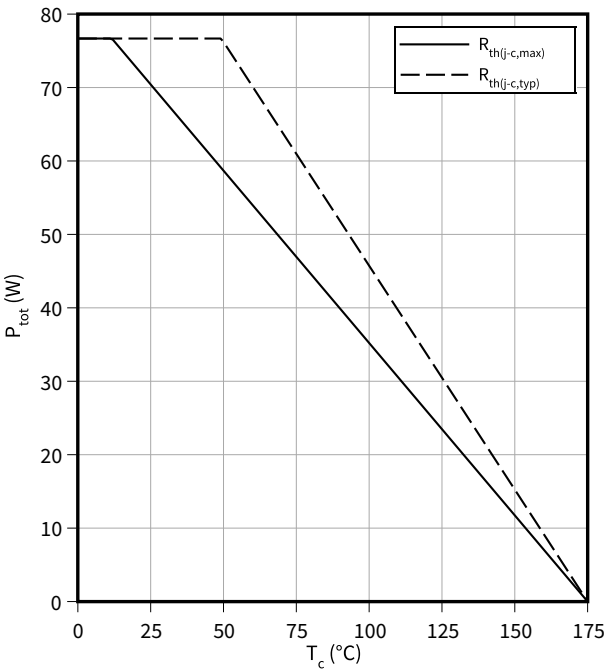
Reverse bias safe operating area (RBSOA)

$I_{DS} = f(V_{DS})$
 $T_{vj} \leq 175\text{ °C}$, $V_{GS} = 0/12\text{ V}$, $T_c = 25\text{ °C}$



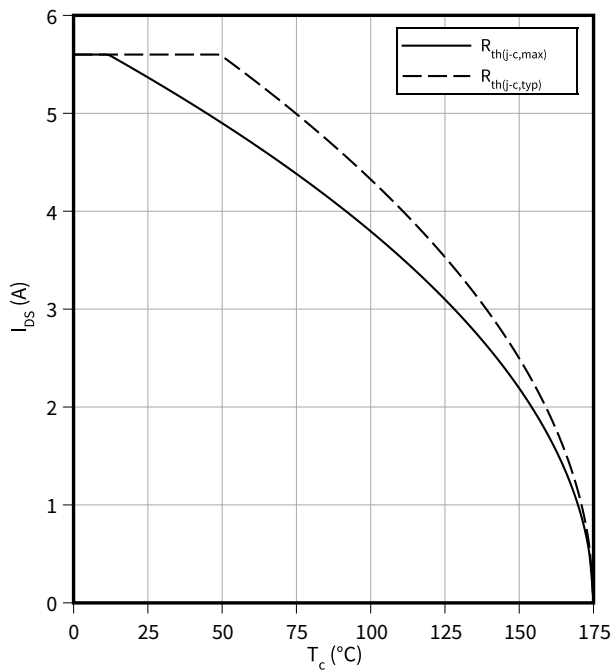
Power dissipation as a function of case temperature limited by bond wire

$P_{tot} = f(T_c)$



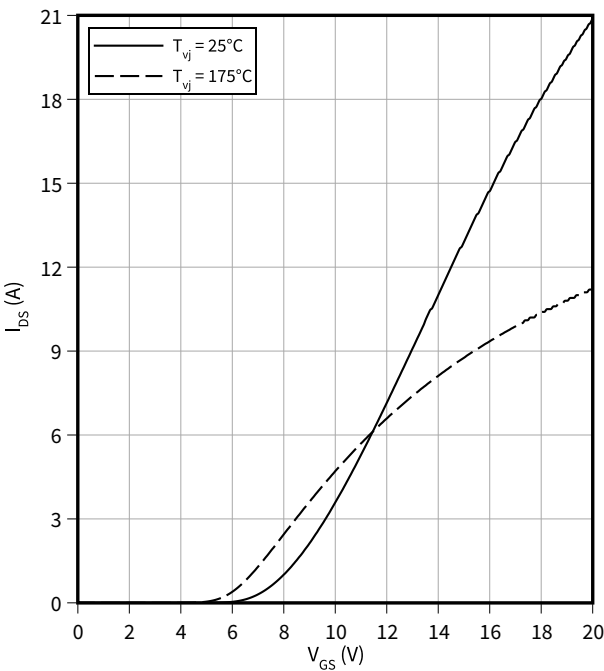
Maximum DC drain to source current as a function of case temperature limited by bond wire

$I_{DS} = f(T_c)$



Typical transfer characteristic

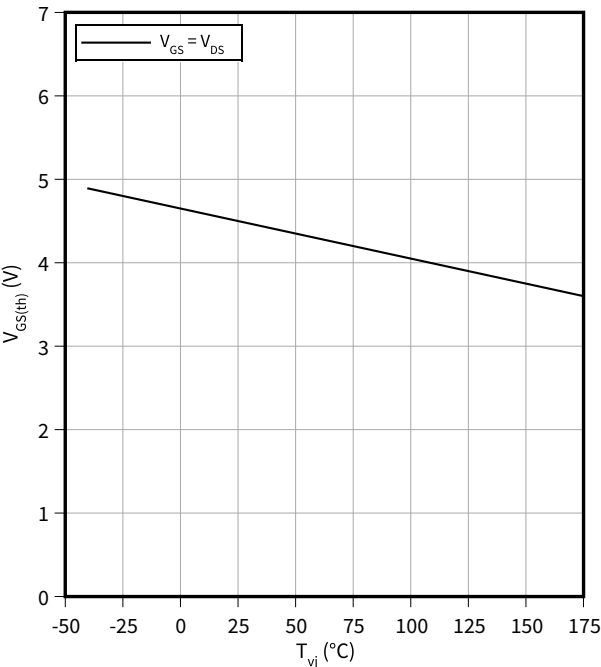
$I_{DS} = f(V_{GS})$
 $V_{DS} = 20\text{ V}$, $t_p = 20\text{ }\mu\text{s}$



3 Characteristics diagrams

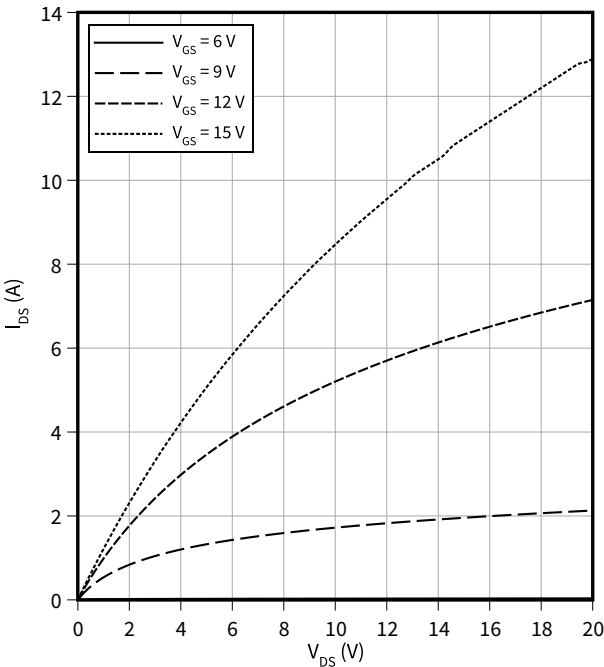
Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$
 $I_D = 1.2 \text{ mA}$



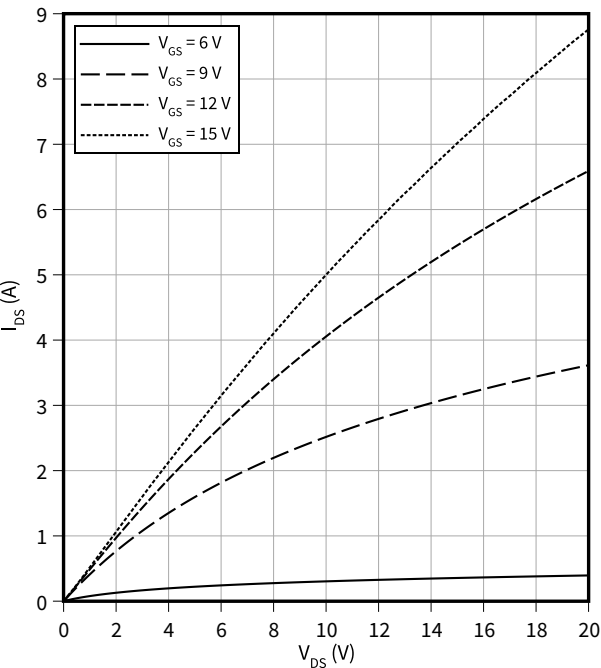
Typical output characteristic, V_{GS} as parameter

$I_{DS} = f(V_{DS})$
 $T_{vj} = 25 \text{ °C}$, $t_p = 20 \text{ }\mu\text{s}$



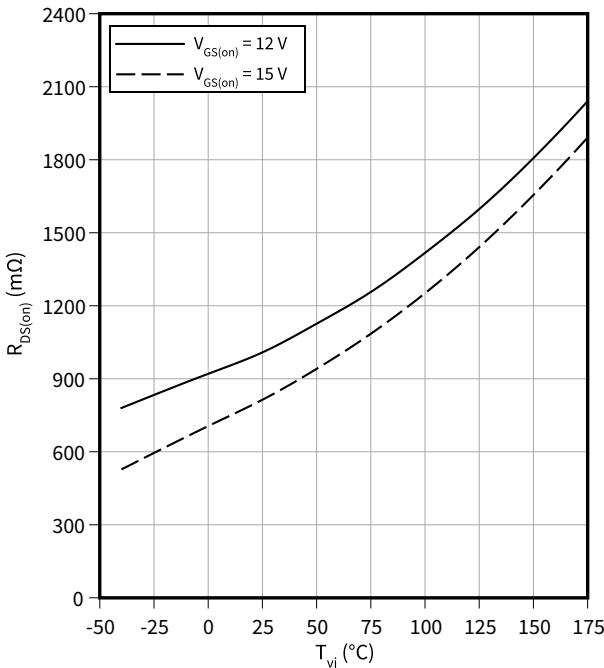
Typical output characteristic, V_{GS} as parameter

$I_{DS} = f(V_{DS})$
 $T_{vj} = 175 \text{ °C}$, $t_p = 20 \text{ }\mu\text{s}$



Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$
 $I_D = 1 \text{ A}$

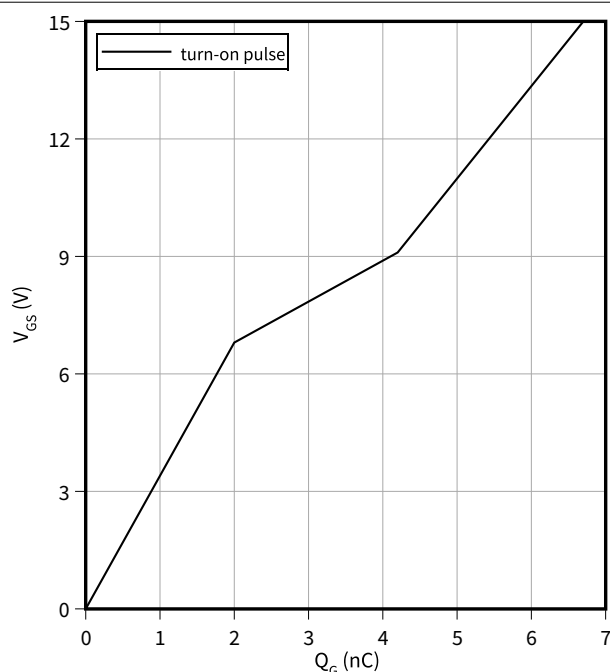


3 Characteristics diagrams

Typical gate charge

$$V_{GS} = f(Q_G)$$

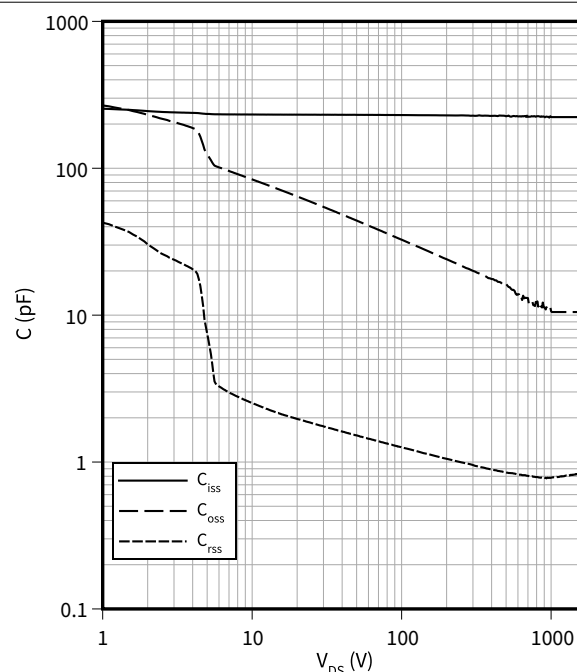
$$I_D = 1 \text{ A}, V_{DS} = 1000 \text{ V}$$



Typical capacitance as a function of drain-source voltage

$$C = f(V_{DS})$$

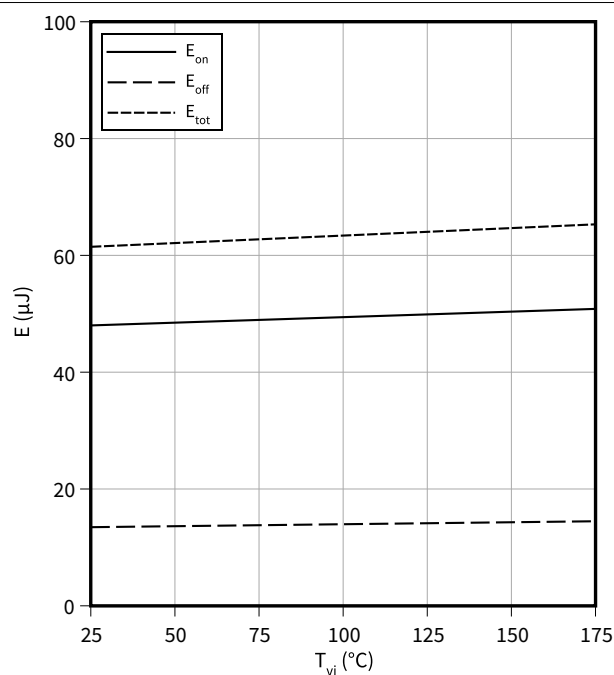
$$f = 100 \text{ kHz}, V_{GS} = 0 \text{ V}$$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0 \text{ V}$

$$E = f(T_{vj})$$

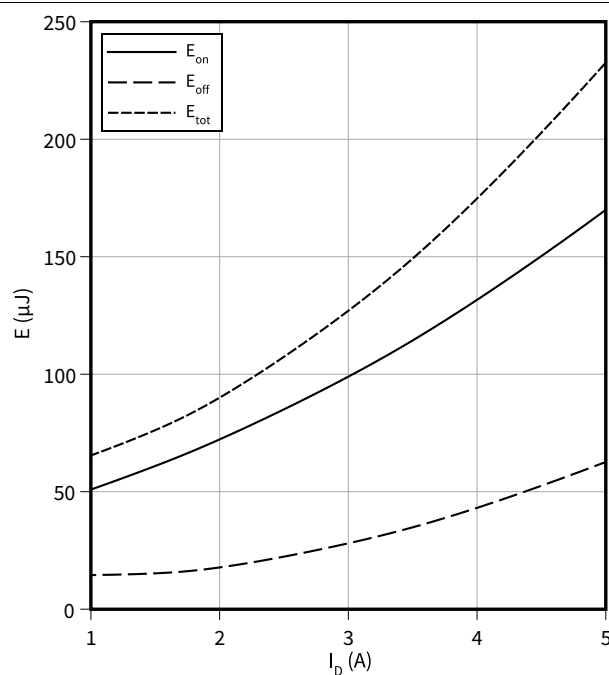
$$V_{GS} = 0/12 \text{ V}, I_D = 1 \text{ A}, R_{G,ext} = 6.9 \Omega, V_{DD} = 1000 \text{ V}$$



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0 \text{ V}$

$$E = f(I_D)$$

$$V_{GS} = 0/12 \text{ V}, T_{vj} = 175 \text{ °C}, R_{G,ext} = 6.9 \Omega, V_{DD} = 1000 \text{ V}$$

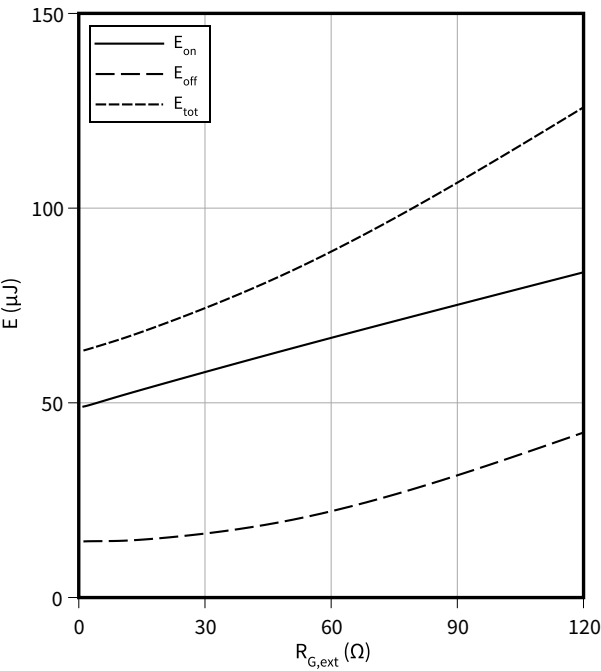


3 Characteristics diagrams

Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\text{ V}$

$E = f(R_{G,ext})$

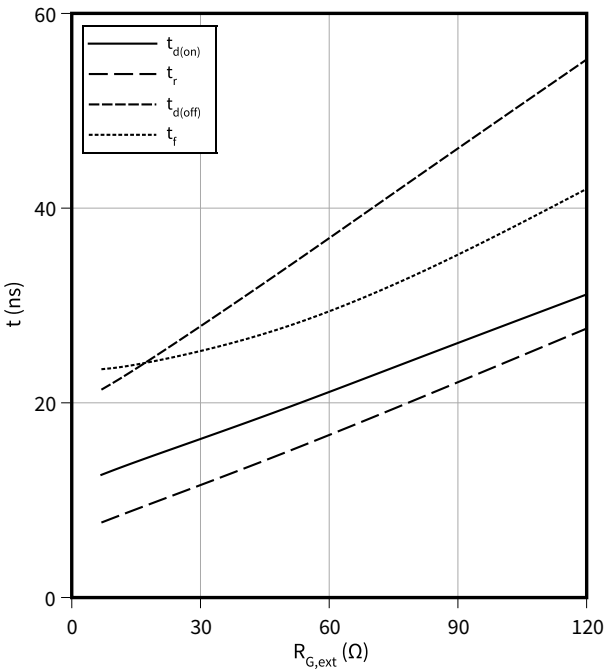
$V_{GS} = 0/12\text{ V}$, $I_D = 1\text{ A}$, $T_{vj} = 175\text{ °C}$, $V_{DD} = 1000\text{ V}$



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\text{ V}$

$t = f(R_{G,ext})$

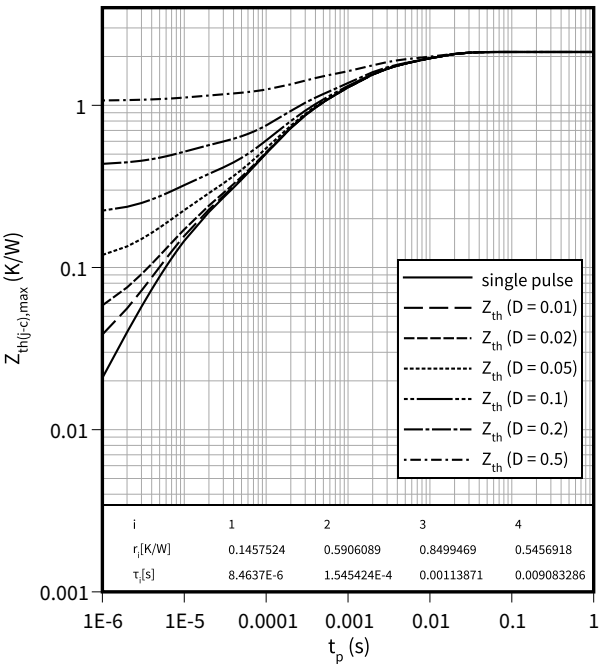
$V_{GS} = 0/12\text{ V}$, $I_D = 1\text{ A}$, $T_{vj} = 175\text{ °C}$, $V_{DD} = 1000\text{ V}$



Max. transient thermal impedance (MOSFET/diode)

$Z_{th(j-c),max} = f(t_p)$

$D = t_p/T$



4 Package outlines

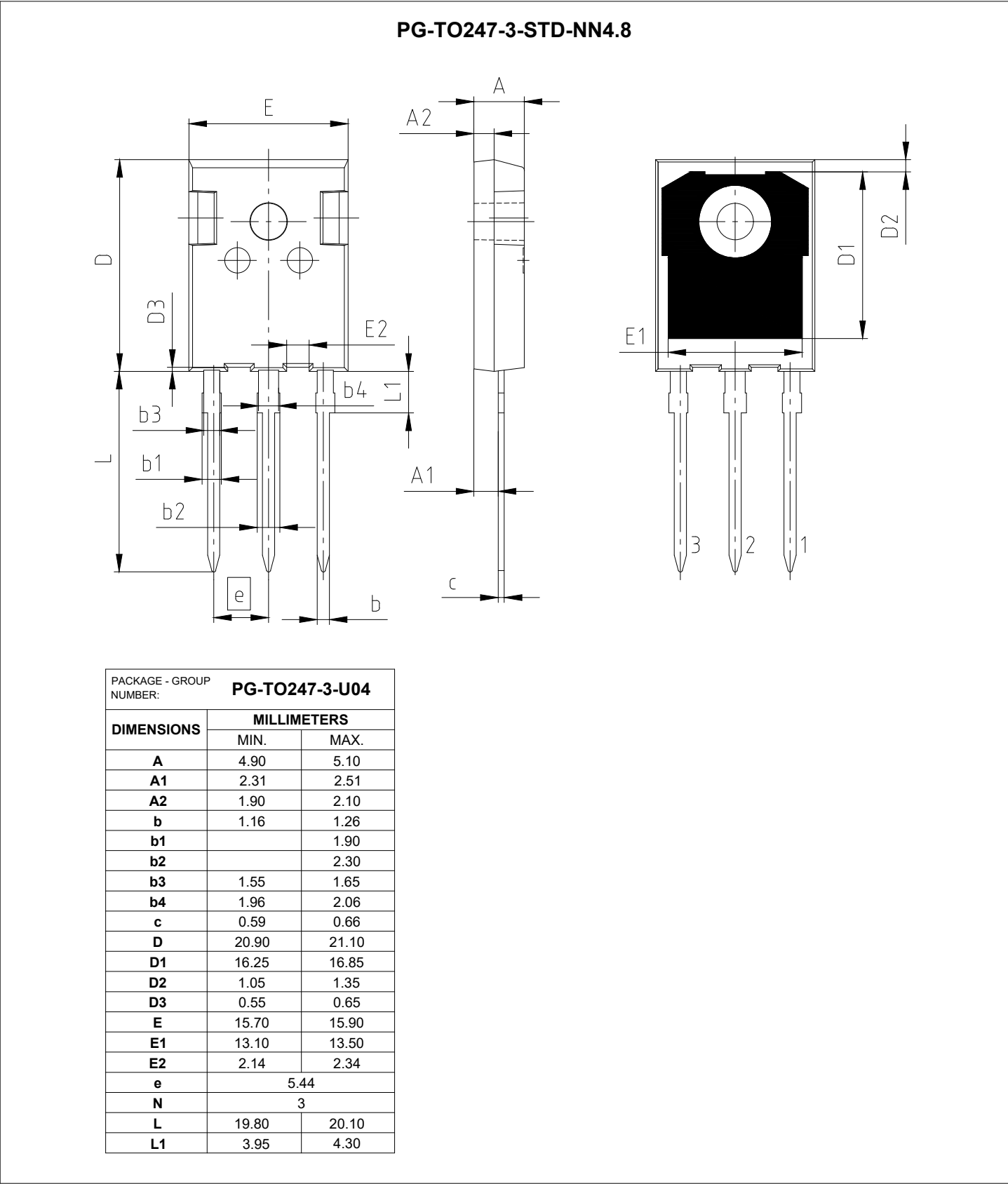


Figure 1

5 Testing conditions

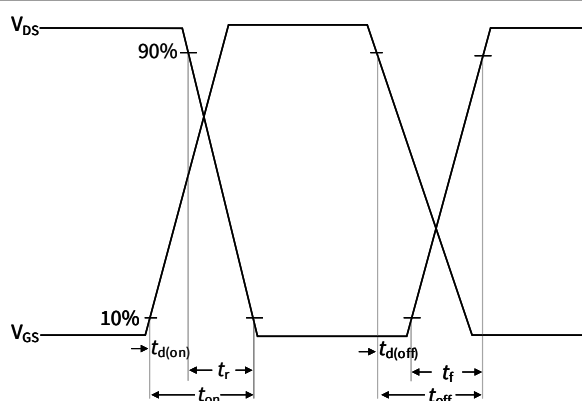


Figure A. Definition of switching times

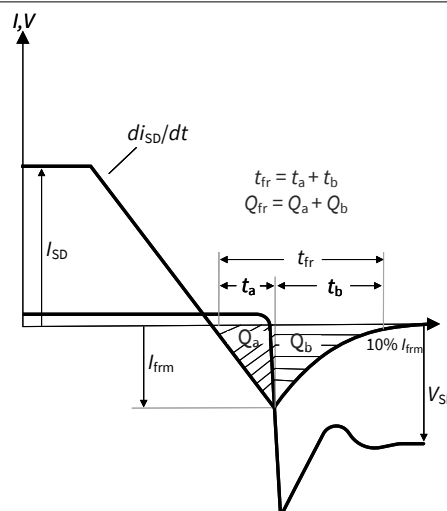


Figure B. Definition of body diode switching characteristics

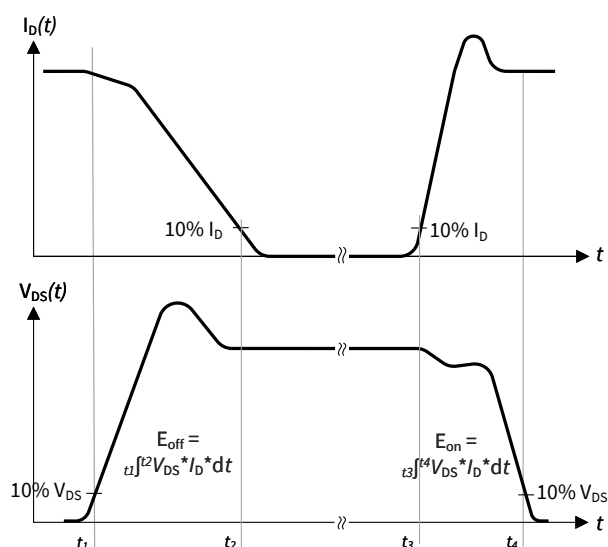


Figure C. Definition of switching losses

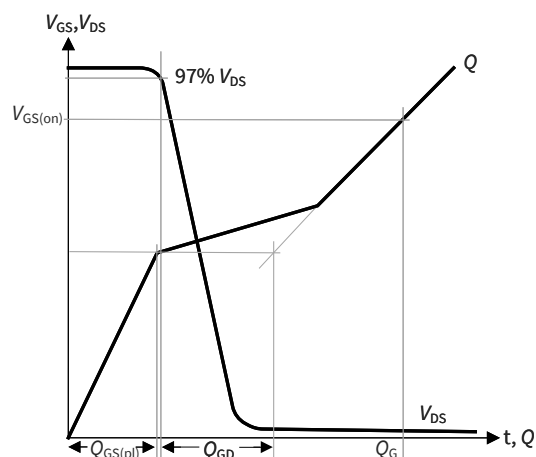


Figure D. Definition of QGD

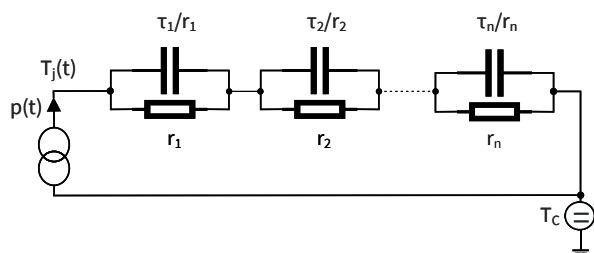


Figure E. Thermal equivalent circuit

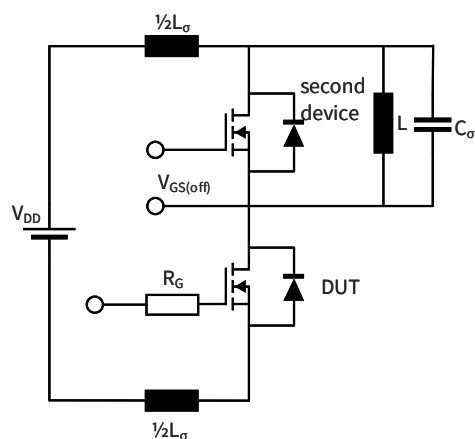


Figure F. Dynamic test circuit

Parasitic inductance L_{σ} ,
Parasitic capacitor C_{σ} ,

Figure 2



Revision history

Revision history

Document revision	Date of release	Description of changes
1.00	2024-03-25	Final datasheet

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