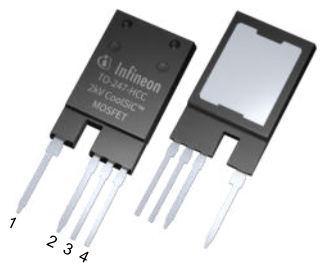
CoolSiC™ 2000 V SiC Trench MOSFET : Silicon Carbide MOSFET with .XT interconnection technology



Halogen-free
Green
Lead-free
RoHS

Features

- V_{DSS} = 2000 V at T_{vj} = 25°C
- I_{DCC} = 26 A at T_c = 25°C
- $R_{DS(on)}$ = 100 mΩ at V_{GS} = 18 V, T_{vj} = 25°C
- Very low switching losses
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.5 V
- Robust body diode for hard commutation
- .XT interconnection technology for best-in-class thermal performance

Potential applications

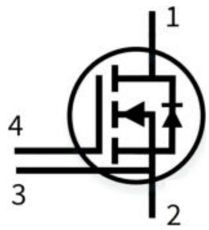
- String inverter
- Solar power optimizer
- EV-Charging

Product validation

- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22
- Please also note the application note AN2019-05 for power and thermal cycling

Description

1 – drain
2 – source
3 – Kelvin sense contact
4 – gate
Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction (only for 4pin, TO263-7L)



Type	Package	Marking
IMYH200R100M1H	PG-TO247-4-PLUS-NT14	20M1H100

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1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	wave soldering 1.6 mm (0.063 in.) from case for 10 s			260	°C
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			0.53	0.69	K/W

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		2000	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 18$ V	$T_c = 25$ °C	26	A
			$T_c = 100$ °C	19	
Peak drain current, t_p limited by $T_{vj(max)}$	I_{DM}	$V_{GS} = 18$ V		57	A
Gate-source voltage, max. transient voltage[1)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10/23	V
Gate-source voltage, max. static voltage	V_{GS}			-7/20	V
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	217	W
			$T_c = 100$ °C	108	

1) **Important note:** The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Table 4 **Characteristic values**

Parameter	Symbol	Note or test condition		Values Min.	Typ.	Max.	Unit
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 10 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		100	131	mΩ
			T_{vj} = 100 °C, $V_{GS(on)}$ = 18 V		170		
			T_{vj} = 175 °C, $V_{GS(on)}$ = 18 V		300		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		108	142	
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 6 mA, V_{DS} = V_{GS} (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.5	5.5	V
			T_{vj} = 175 °C		3.6		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 2000 V, V_{GS} = 0 V	T_{vj} = 25 °C			200	µA
			T_{vj} = 175 °C		10		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 23 V			100	nA
			V_{GS} = -10 V			-100	
Forward transconductance	g_{fs}	I_D = 10 A, V_{DS} = 20 V			5		S
Internal gate resistance	$R_{G,int}$	f = 100 kHz, V_{AC} = 25 mV			6.4		Ω
Input capacitance	C_{iss}	V_{DD} = 1200 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			1215		pF
Output capacitance	C_{oss}	V_{DD} = 1200 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			40		pF
Reverse transfer capacitance	C_{rss}	V_{DD} = 1200 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			3		pF
C_{oss} stored energy	E_{oss}	V_{DD} = 1200 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			30		µJ
Total gate charge	Q_G	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, turn-on pulse			55		nC
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, turn-on pulse			14		nC
Gate-to-drain charge	Q_{GD}	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, turn-on pulse			5.6		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -2 V	T_{vj} = 25 °C		2		ns
			T_{vj} = 175 °C		3		

(table continues...)

Table 4 **(continued) Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Rise time	t_r	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -2 V	T_{vj} = 25 °C		3		ns
			T_{vj} = 175 °C		4		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -2 V	T_{vj} = 25 °C		21		ns
			T_{vj} = 175 °C		28		
Fall time	t_f	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -2 V	T_{vj} = 25 °C		5		ns
			T_{vj} = 175 °C		5		
Turn-on energy	E_{on}	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -2 V	T_{vj} = 25 °C		280		µJ
			T_{vj} = 175 °C		570		
Turn-off energy	E_{off}	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -2 V	T_{vj} = 25 °C		50		µJ
			T_{vj} = 175 °C		50		
Total switching energy	E_{tot}	V_{DD} = 1200 V, I_D = 10 A, V_{GS} = -2/18 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -2 V	T_{vj} = 25 °C		470		µJ
			T_{vj} = 175 °C		900		
Virtual junction temperature	T_{vj}			-55		175	°C

Note: *The chip technology was characterized up to 100 kV/µs. The measured dV/dt was limited by measurement test setup and package.*

Dynamic test circuit see Fig. F.

3 Body diode (MOSFET)

Table 5 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		2000	V
Continuous reverse drain current for $R_{th(j\text{-}c,max)}$, limited by $T_{vj(max)}$	I_{SDC}	$V_{GS} = 0$ V	$T_c = 25$ °C	27	A
			$T_c = 100$ °C	21	
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	$V_{GS} = 0$ V		31	A

Table 6 Characteristic values

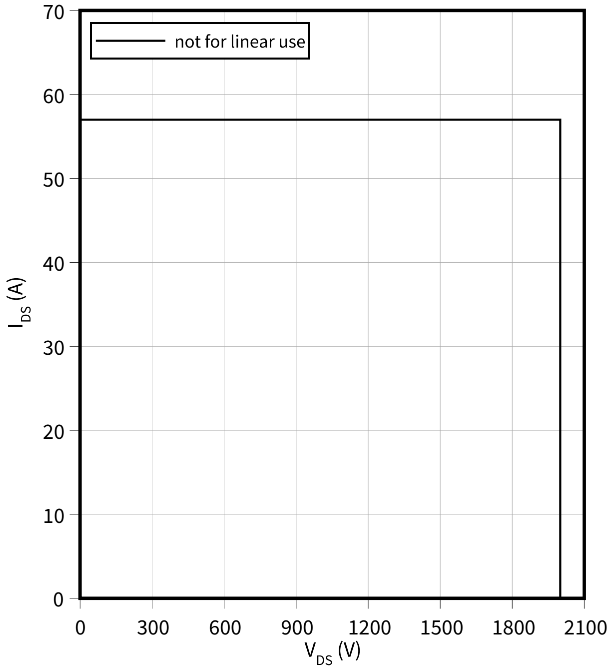
Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	$I_{SD} = 10$ A, $V_{GS} = 0$ V	$T_{vj} = 25$ °C		3.7	5.5	V
			$T_{vj} = 100$ °C		3.6		
			$T_{vj} = 175$ °C		3.5		
MOSFET forward recovery charge	Q_{fr}	$V_{DD} = 1200$ V, $I_{SD} = 10$ A, V_{GS}=-2 V, $R_{GS(on)} = 2\ \Omega$, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		250		nC
			$T_{vj} = 175$ °C		247		
MOSFET peak forward recovery current	I_{frm}	$V_{DD} = 1200$ V, $I_{SD} = 10$ A, V_{GS}=-2 V, di_{SD}/dt = 380 A/µs, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		7		A
			$T_{vj} = 175$ °C		8		
MOSFET forward recovery energy	E_{fr}	$V_{DD} = 1200$ V, $I_{SD} = 10$ A, V_{GS}=-2 V, $R_{GS(on)} = 2\ \Omega$, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		140		µJ
			$T_{vj} = 175$ °C		280		
Virtual junction temperature	T_{vj}			-55		175	°C

4 Characteristics diagrams

Reverse bias safe operating area (RBSOA)

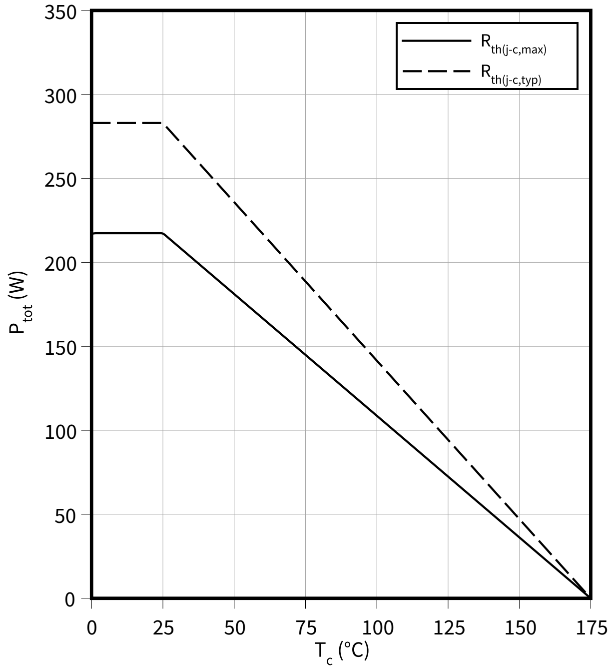
$I_{DS} = f(V_{DS})$

$T_{vj} \leq 175\ °C$, $V_{GS} = 0/18\ V$, $T_c = 25\ °C$



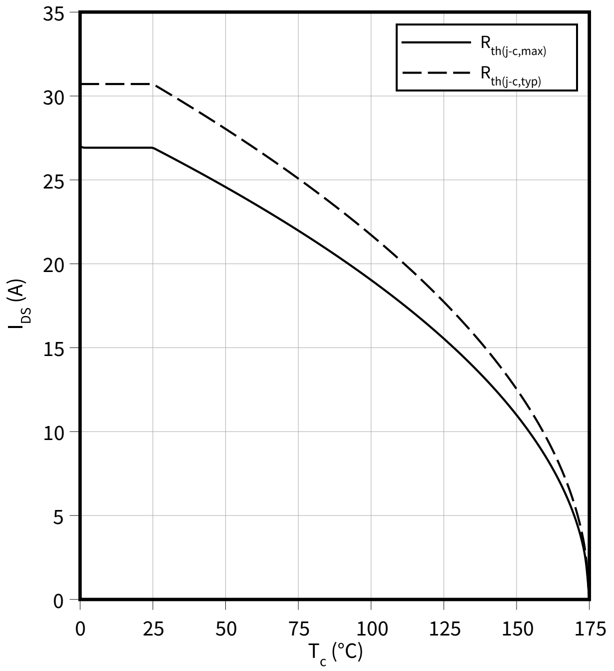
Power dissipation as a function of case temperature limited by bond wire

$P_{tot} = f(T_c)$



Maximum DC drain to source current as a function of case temperature limited by bond wire

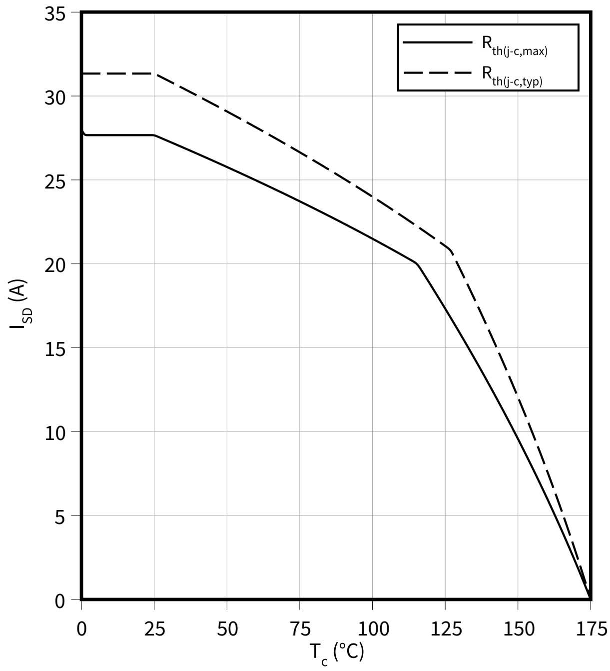
$I_{DS} = f(T_c)$

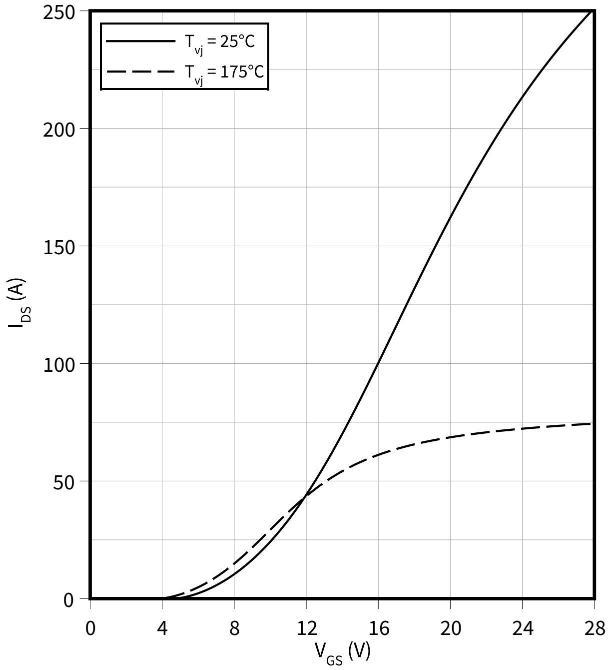
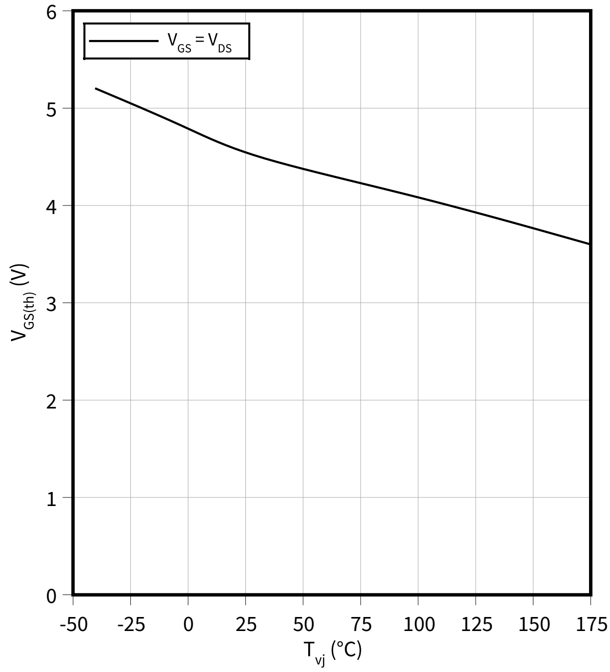
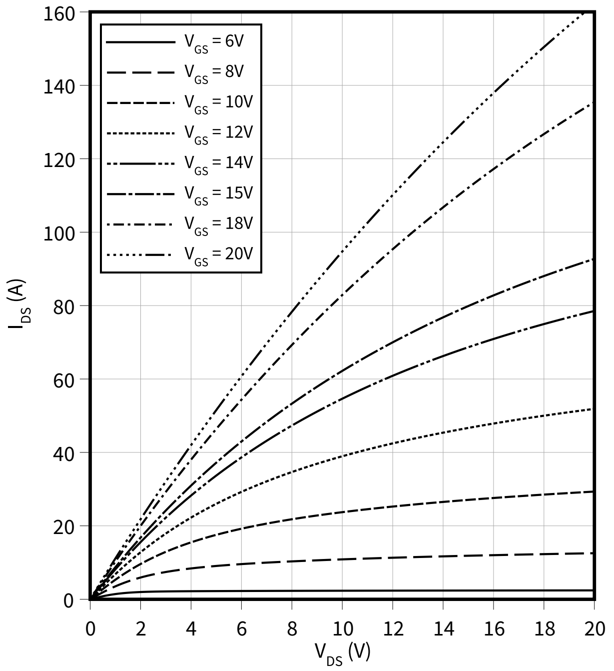
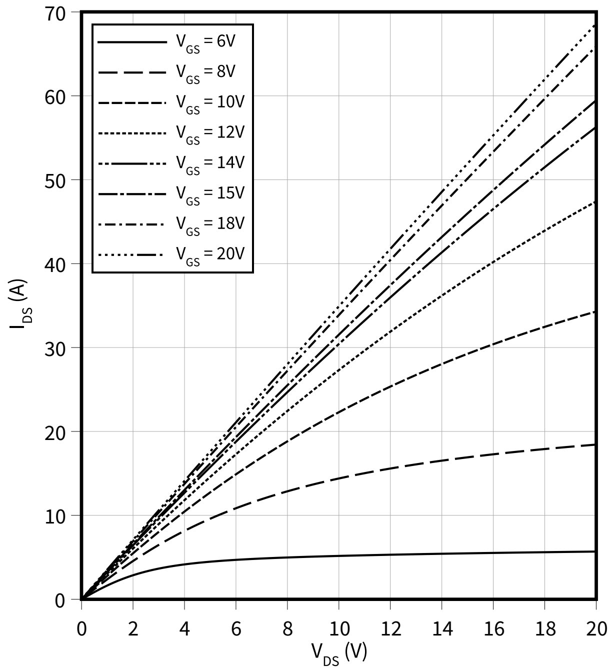


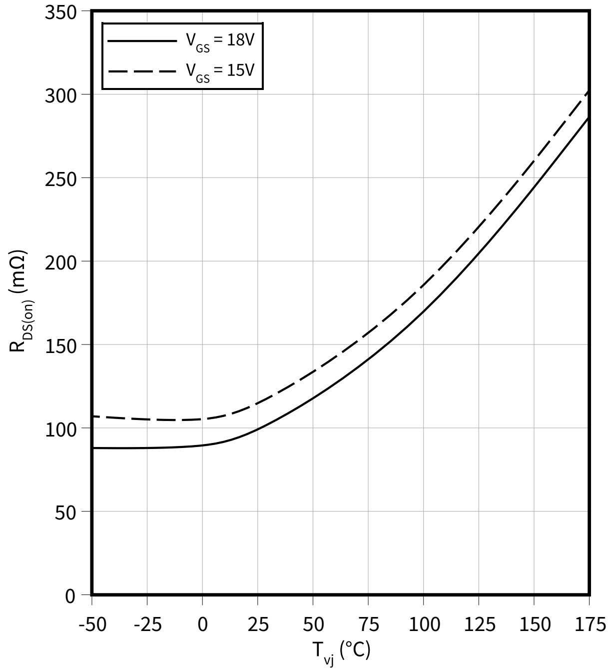
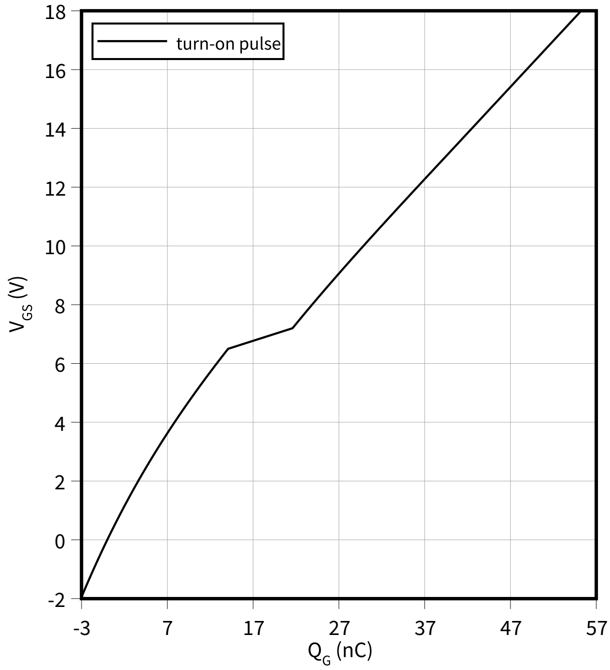
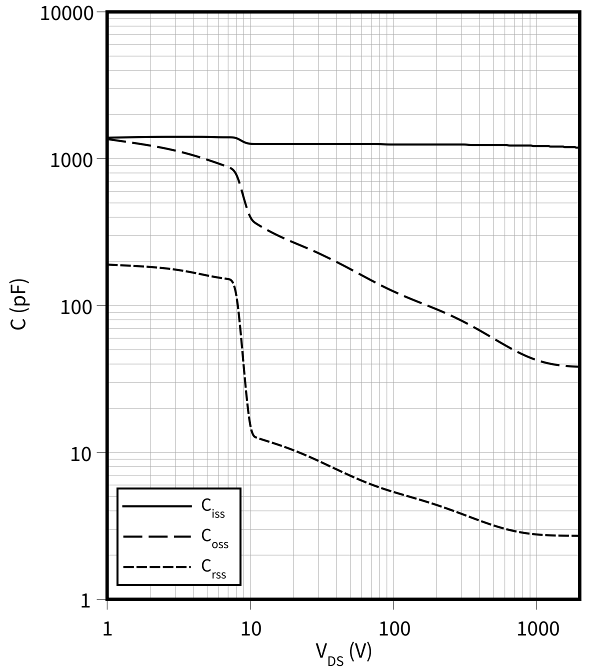
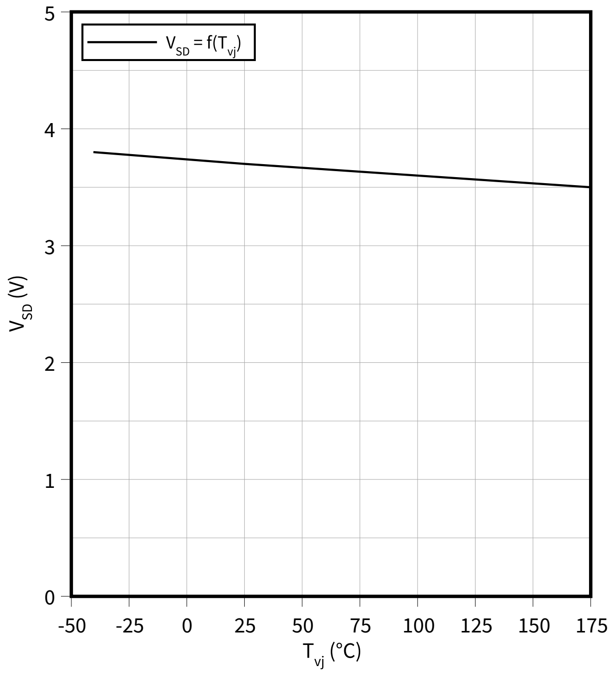
Maximum source to drain current as a function of case temperature limited by bond wire

$I_{SD} = f(T_c)$

$V_{GS} = 0\ V$



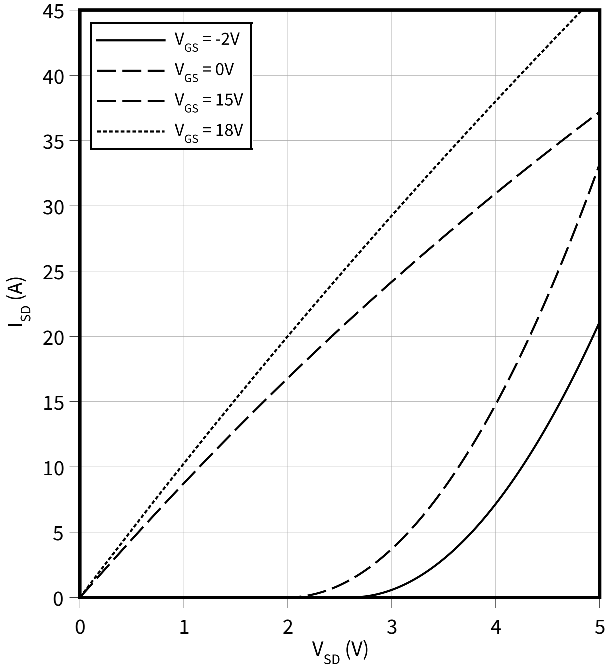
Typical transfer characteristic $I_{DS} = f(V_{GS})$ $V_{DS} = 20$ V, $t_p = 20$ µs	**Typical gate-source threshold voltage as a function of junction temperature** $V_{GS(th)} = f(T_{vj})$ $I_D = 6$ mA
	
Typical output characteristic, V_{GS} as parameter $I_{DS} = f(V_{DS})$ $T_{vj} = 25$ °C, $t_p = 20$ µs	**Typical output characteristic, V_{GS} as parameter** $I_{DS} = f(V_{DS})$ $T_{vj} = 175$ °C, $t_p = 20$ µs
	

Typical on-state resistance as a function of junction temperature $R_{DS(on)} = f(T_{vj})$ $I_D = 10$ A	**Typical gate charge** $V_{GS} = f(Q_G)$ $I_D = 10$ A, $V_{DS} = 1200$ V
	
Typical capacitance as a function of drain-source voltage $C = f(V_{DS})$ $f = 100$ kHz, $V_{GS} = 0$ V	**Typical reverse drain voltage as function of junction temperature** $V_{SD} = f(T_{vj})$ $I_{SD} = 10$ A, $V_{GS} = 0$ V
	

Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$I_{SD} = f(V_{SD})$

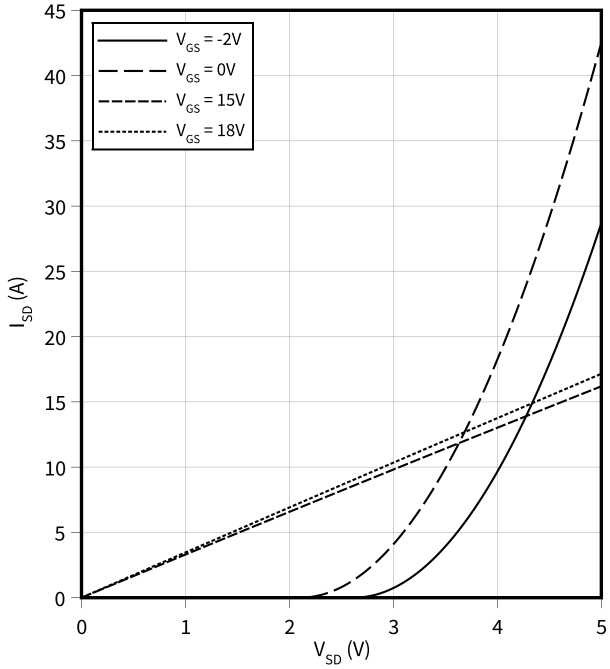
$T_{vj} = 25\ °C$, $t_p = 20\ µs$



Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$I_{SD} = f(V_{SD})$

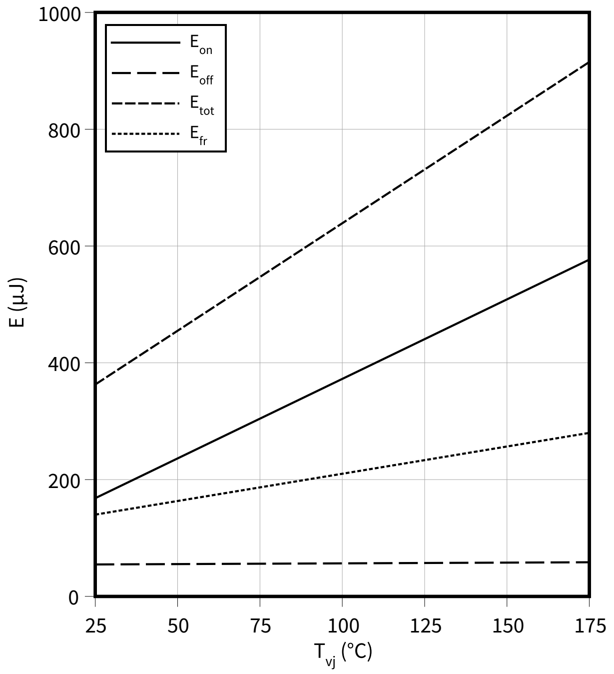
$T_{vj} = 175\ °C$, $t_p = 20\ µs$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -2 V

$E = f(T_{vj})$

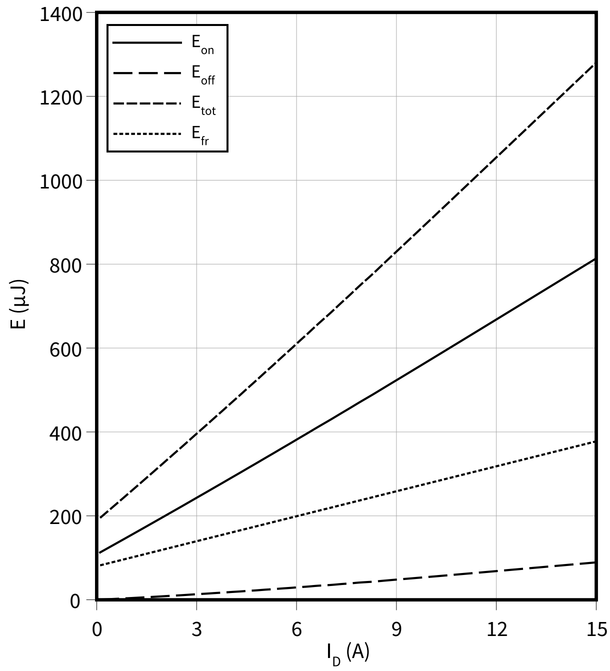
$V_{GS} = -2/18\ V$, $I_D = 10\ A$, $R_{G,ext} = 2\ Ω$, $V_{DD} = 1200\ V$



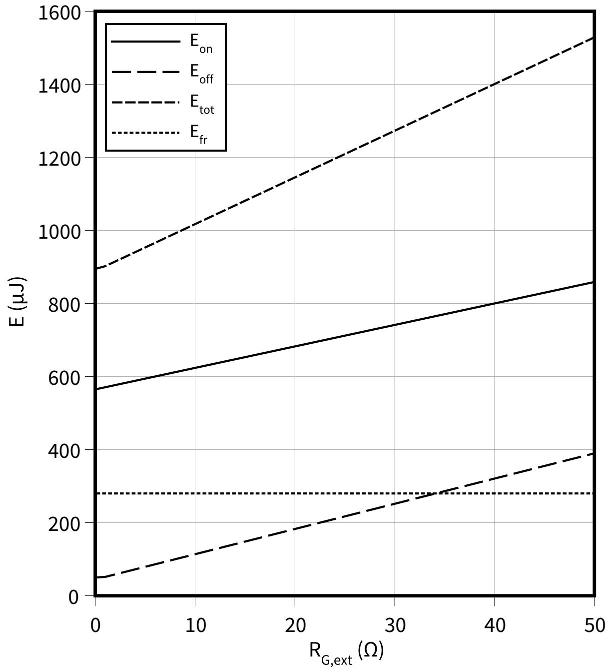
Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -2 V

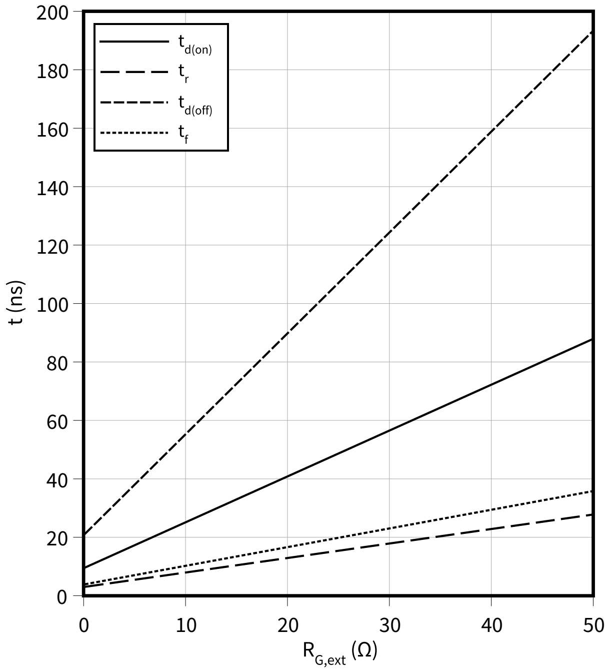
$E = f(I_D)$

$V_{GS} = -2/18\ V$, $T_{vj} = 175\ °C$, $R_{G,ext} = 2\ Ω$, $V_{DD} = 1200\ V$

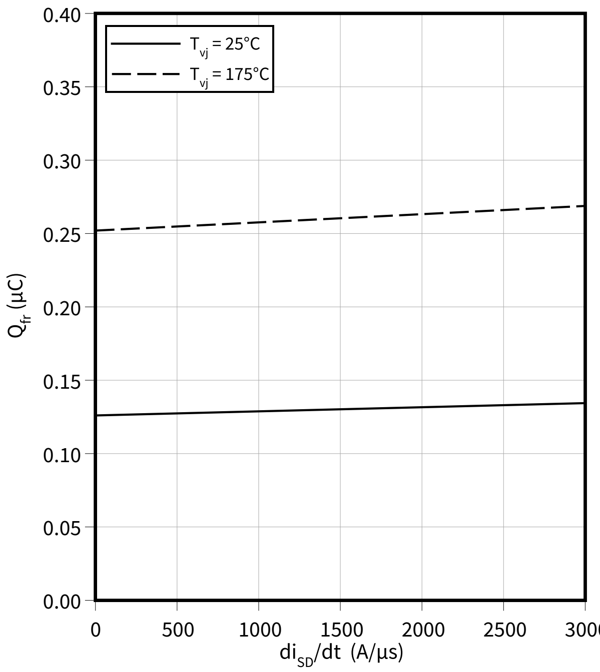


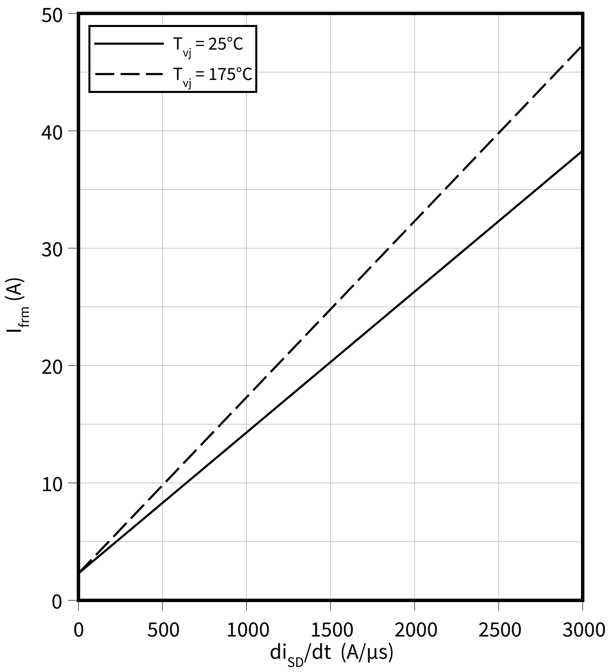
Typical switching energy losses as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -2 V	**Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -2 V**
$E = f(R_{G,ext})$	$t = f(R_{G,ext})$
V_{GS} = -2/18 V, I_D = 10 A, T_{vj} = 175 °C, V_{DD} = 1200 V	V_{GS} = -2/18 V, I_D = 10 A, T_{vj} = 175 °C, V_{DD} = 1200 V

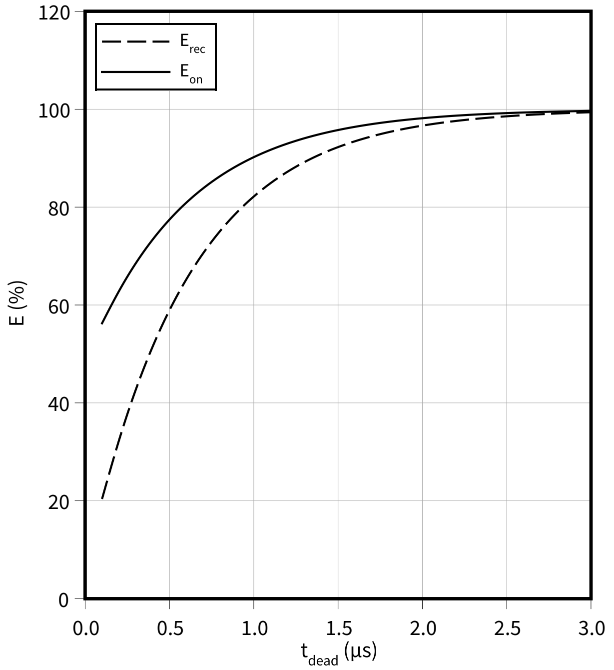
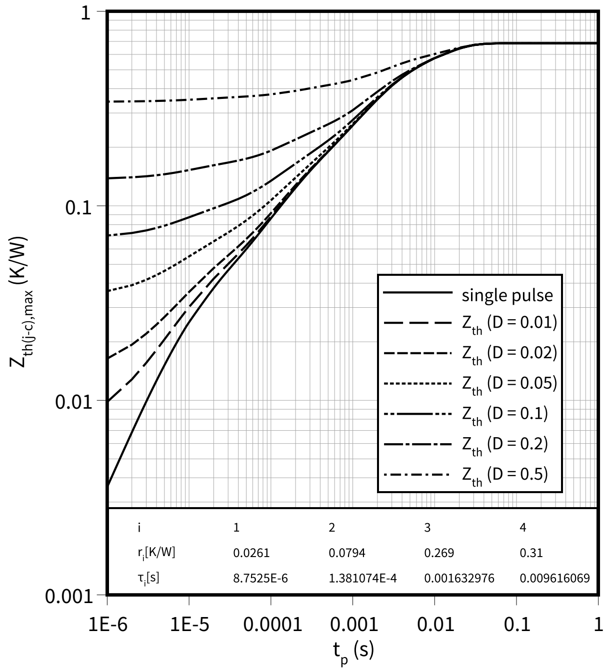




Typical reverse recovery charge as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -2 V	**Typical reverse recovery current as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -2 V**
$Q_{fr} = f(di_{SD}/dt)$	$I_{frm} = f(di_{SD}/dt)$
V_{GS} = -2/18 V, I_{SD} = 10 A, V_{DD} = 1200 V	V_{GS} = -2/18 V, I_{SD} = 10 A, V_{DD} = 1200 V



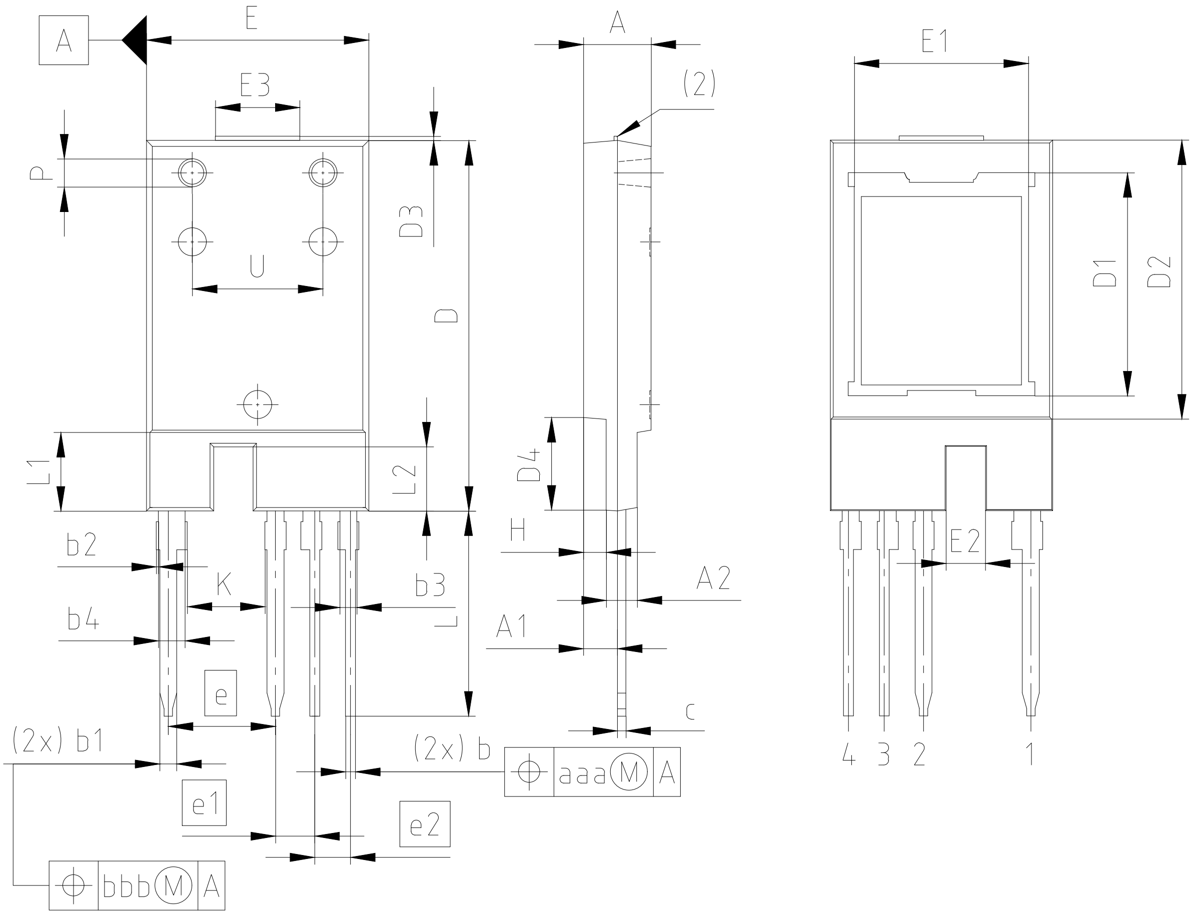


Typical switching energy losses as a function of dead time / blanking time, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V $E = f(t_{dead})$ I_D = 10 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2 Ω, V_{DD} = 1200 V	**Max. transient thermal impedance (MOSFET/diode)** $Z_{th(j-c),max} = f(t_p)$ $D = t_p/T$
	

i	1	2	3	4
r_i[K/W]	0.0261	0.0794	0.269	0.31
τ_i[s]	8.7525E-6	1.381074E-4	0.001632976	0.009616069

5 Package outlines

PG-TO247-4-PLUS-NT14



NOTES:
(1) ALL METAL SURFACES TIN PLATED EXPECT AREA OF CUT
(2) MOLD GATE PROTRUSION AFTER DEGATING

PACKAGE - GROUP NUMBER:	PG-TO247-4-U04				
DIMENSIONS	**MILLIMETERS**		**DIMENSIONS**	**MILLIMETERS**	
	MIN.	MAX.		MIN.	MAX.
A	4.65	4.95	**E1**	12.00	12.80
A1	2.16	2.66	**E2**	2.60	3.00
A2	2.00	2.40	**E3**	5.00	7.00
b	0.60	0.80	**e**	7.62	
b1	1.10	1.30	**e1**	2.79	
b2	---	0.15	**e2**	2.54	
b3	1.10	1.30	**H**	1.51	1.71
b4	1.70	2.10	**K**	5.50	---
c	0.50	0.70	**N**	4	
D	26.00	26.70	**L**	14.30	14.90
D1	15.50	16.30	**L1**	5.40	5.70
D2	19.40	20.20	**L2**	5.40	5.70
D3	---	0.50	**ØP**	1.75	2.25
D4	6.35	6.65	**U**	9.00	9.50
E	15.60	16.00	**aaa**	0.25	
			bbb	0.25	

Figure 1

6 Testing conditions

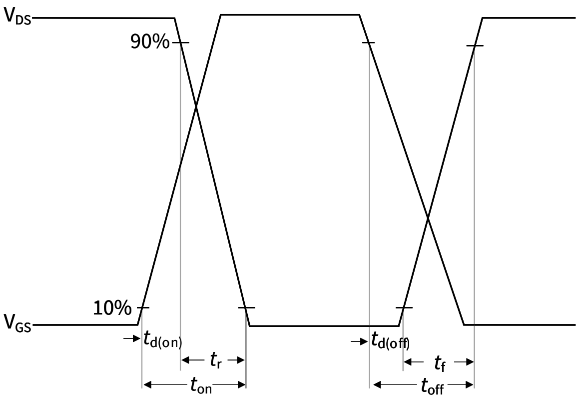


Figure A. **Definition of switching times**

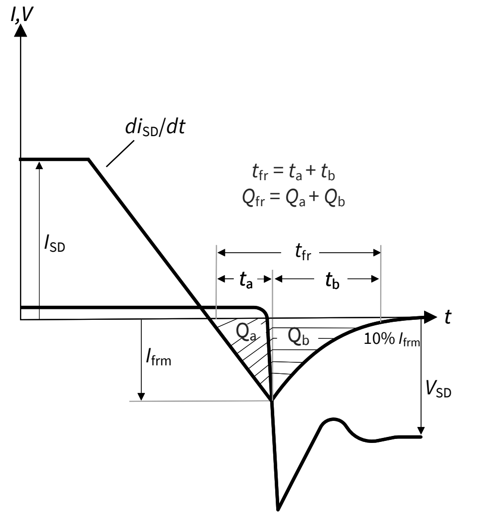


Figure B. **Definition of body diode switching characteristics**

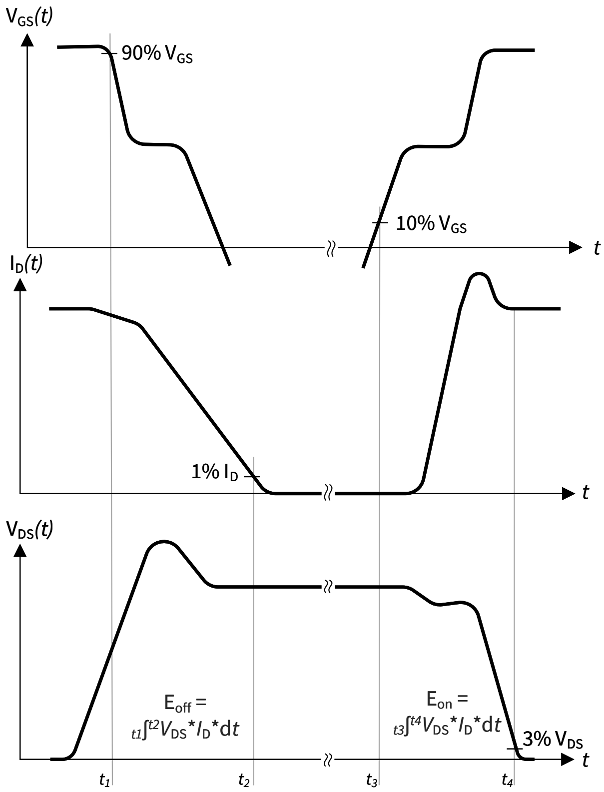


Figure C. **Definition of switching losses**

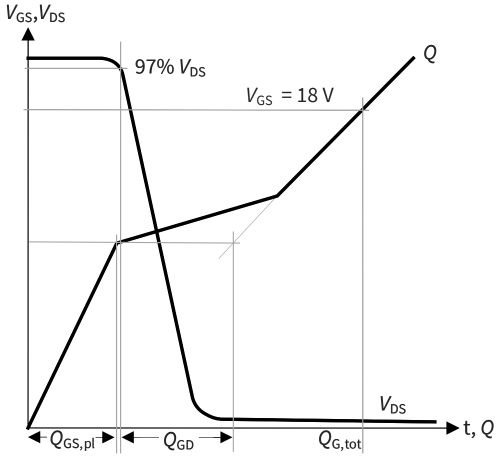


Figure D. **Definition of QGD**

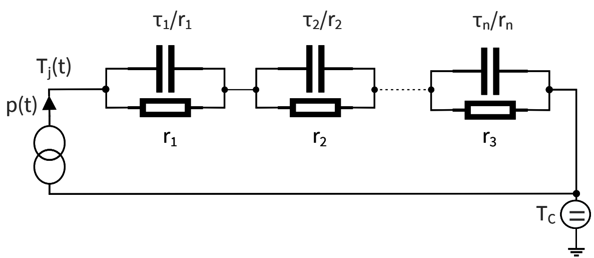


Figure E. **Thermal equivalent circuit**

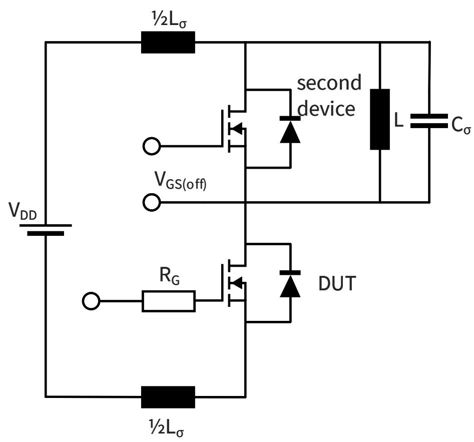


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

Figure 2

Revision history

Document revision	Date of release	Description of changes
0.10	2022-03-08	Preliminary datasheet
1.00	2022-10-04	Final datasheet
1.01	2022-10-06	Editorial changes
1.10	2023-01-16	Change of picture on page 1 Change of product outline drawing on page 13 Editorial changes

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Edition 2023-01-16

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-ABD266-004