



IPB100N10S3-05

IPI100N10S3-05, IPP100N10S3-05

OptiMOS™ -T Power-Transistor



Features

- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

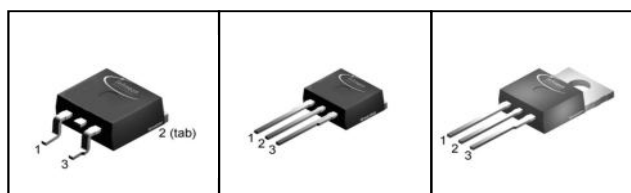
Product Summary

V_{DS}	100	V
$R_{DS(on),max}$ (SMD version)	4.8	mΩ
I_D	100	A

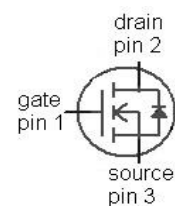
PG-TO263-3-2

PG-TO262-3-1

PG-TO220-3-1



Type	Package	Marking
IPB100N10S3-05	PG-TO263-3-2	3PN1005
IPI100N10S3-05	PG-TO262-3-1	3PN1005
IPP100N10S3-05	PG-TO220-3-1	3PN1005



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	100	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	100	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	400	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=50\text{ A}$	1445	mJ
Avalanche current, single pulse	I_{AS}		100	A
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	300	W
Operating and storage temperature	T_j , T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}		-	-	0.5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=240\mu\text{A}$	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=100\text{ A}$	-	4.3	5.1	m Ω
		$V_{GS}=10\text{ V}, I_D=100\text{ A},$ SMD version	-	4.0	4.8	



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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	8900	11570	pF
Output capacitance	C_{oss}		-	2520	3276	
Reverse transfer capacitance	C_{rss}		-	220	330	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=80A, R_G=3.5\Omega$	-	34	-	ns
Rise time	t_r		-	17	-	
Turn-off delay time	$t_{d(off)}$		-	60	-	
Fall time	t_f		-	20	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=80V, I_D=100A,$ $V_{GS}=0 \text{ to } 10V$	-	47	61	nC
Gate to drain charge	Q_{gd}		-	34	51	
Gate charge total	Q_g		-	135	176	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	100	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=80A,$ $T_j=25^\circ C$	0.6	1	1.2	V
Reverse recovery time ²⁾	t_{rr}	$V_R=50V, I_F=I_S,$ $di_F/dt=100A/\mu s$	-	108	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	380	-	nC

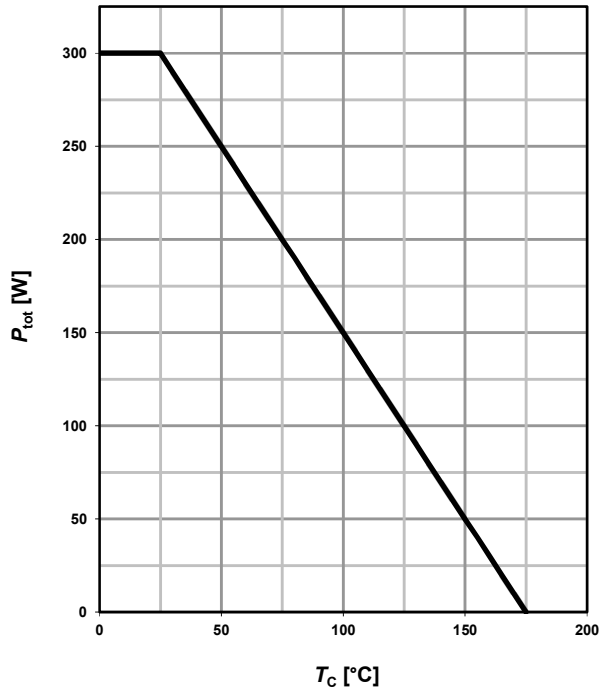
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.5K/W$ the chip is able to carry 165A at 25°C. For detailed information see Application Note ANPS071E

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

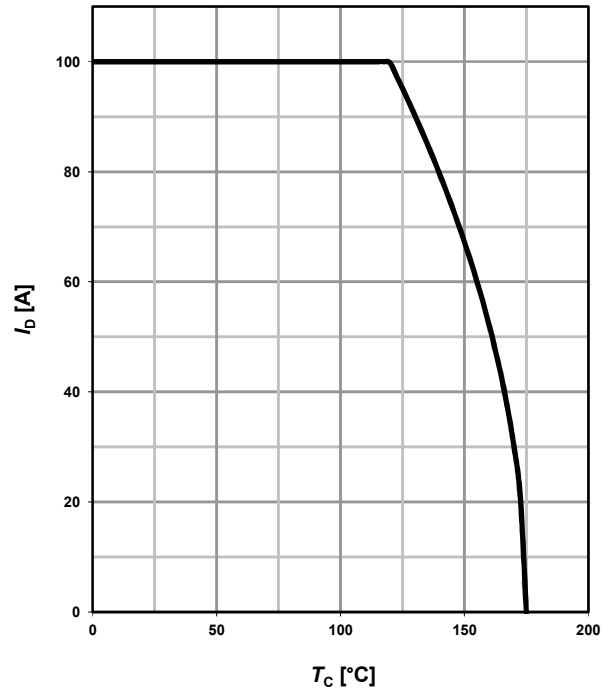
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

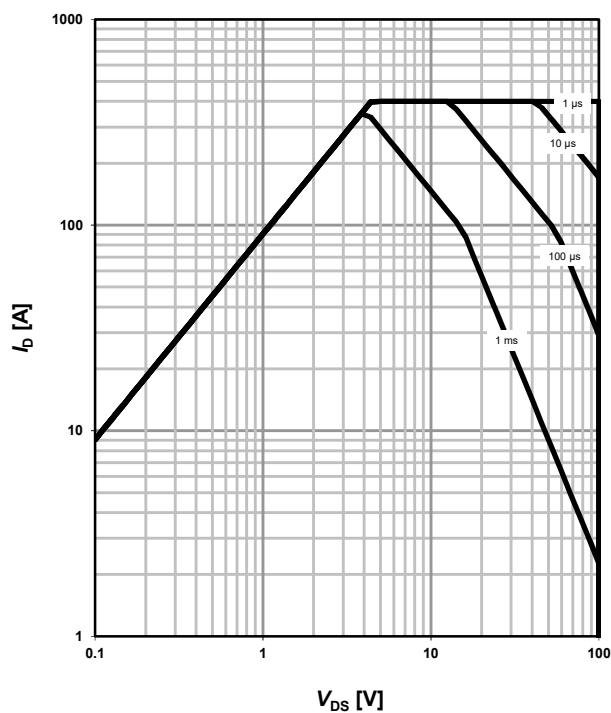
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}; \text{SMD}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0; \text{SMD}$$

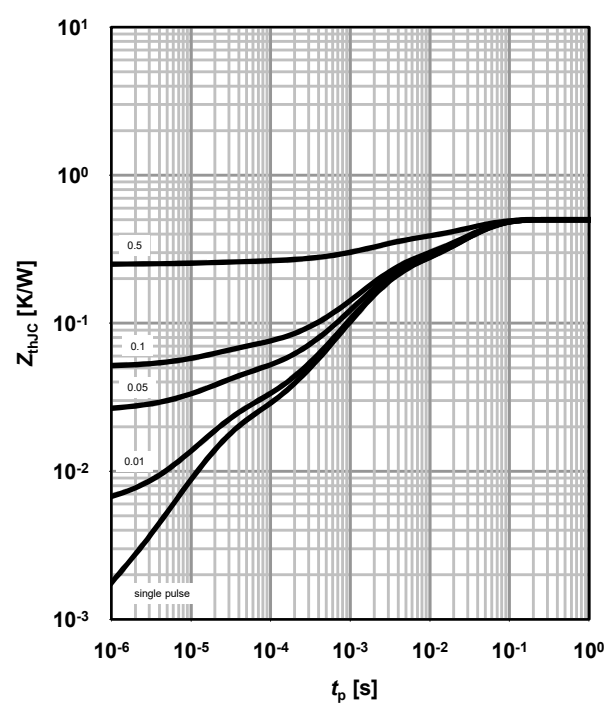
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$





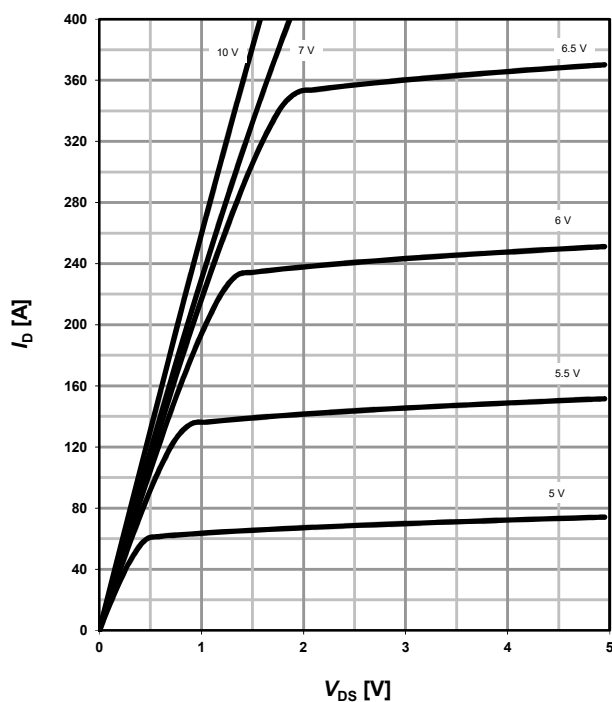
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5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; SMD

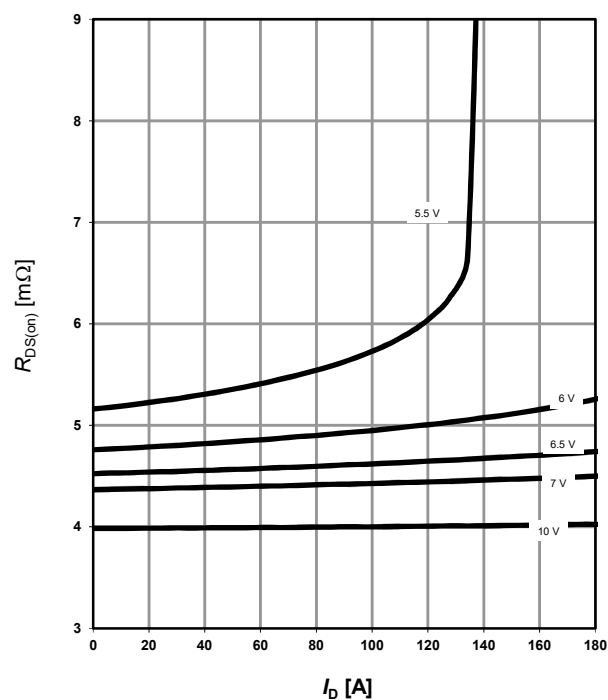
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25\text{ °C}$; SMD

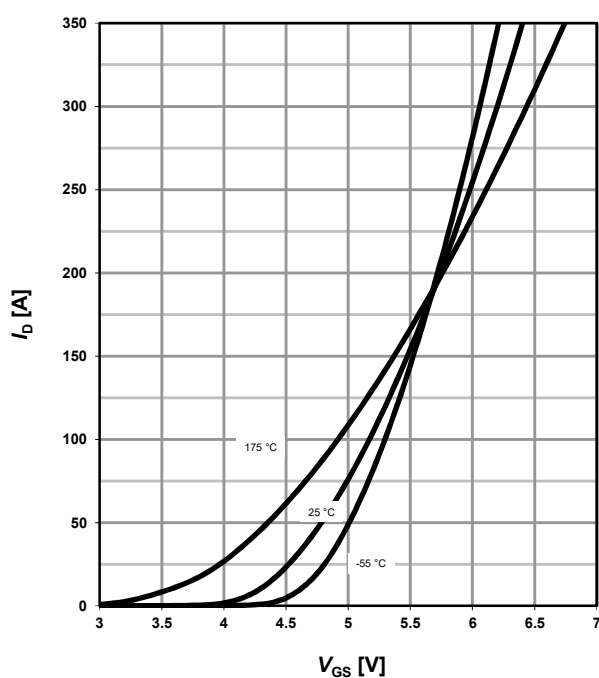
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6\text{ V}$

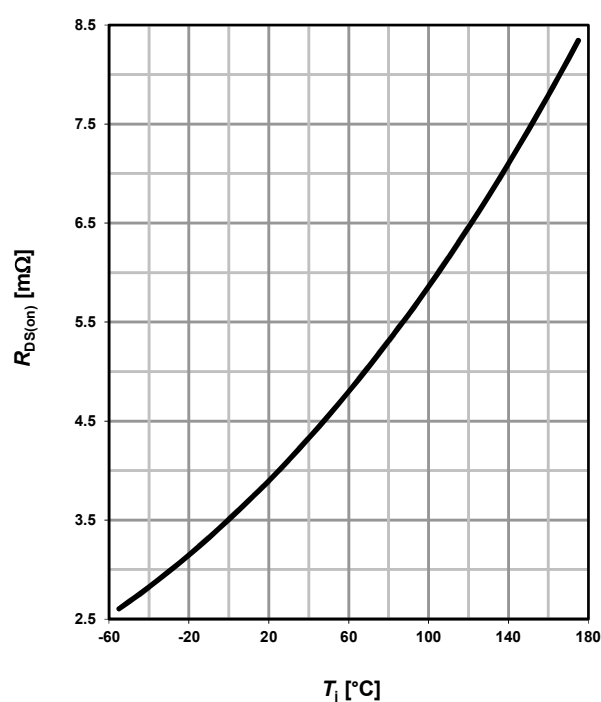
parameter: T_j



8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; $I_D = 100\text{ A}$; $V_{GS} = 10\text{ V}$; SMD

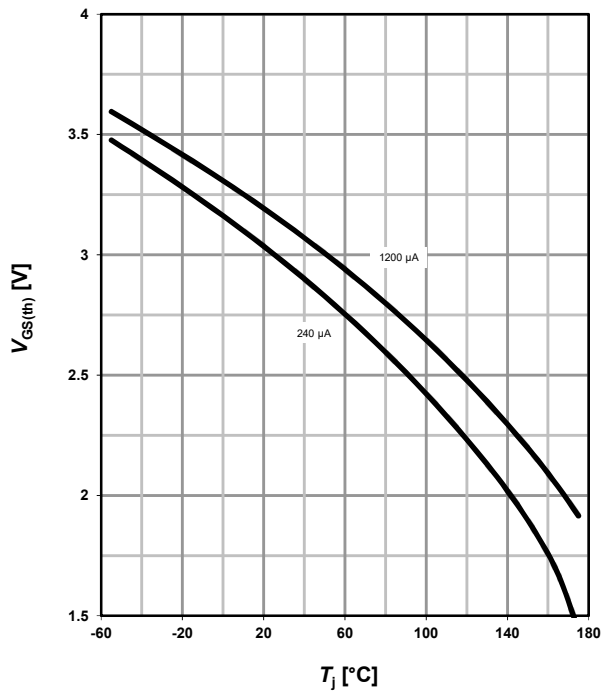
$\alpha = 0.56$



9 Typ. gate threshold voltage

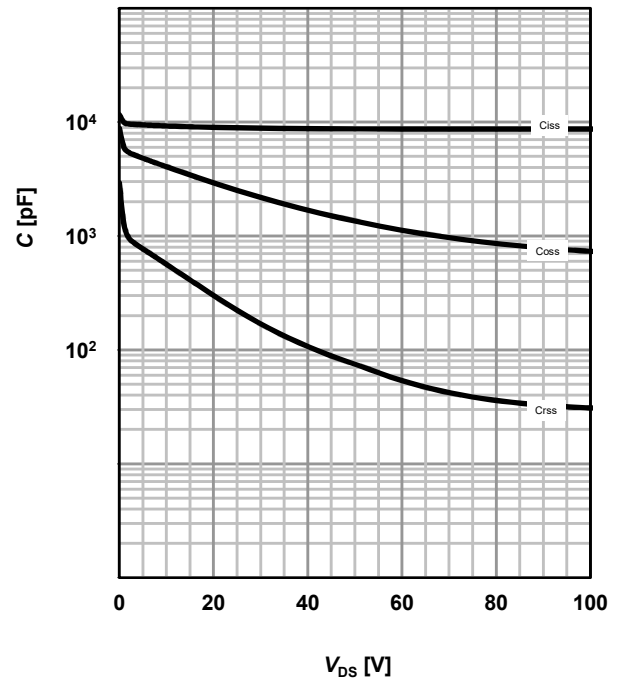
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

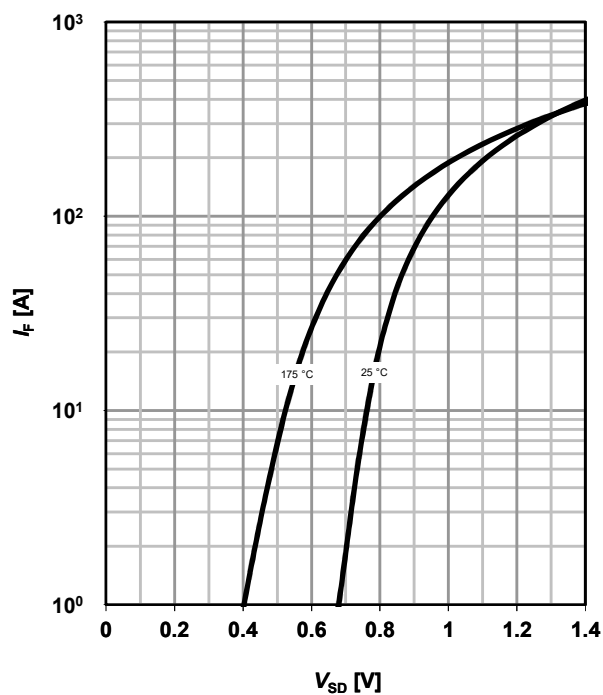
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

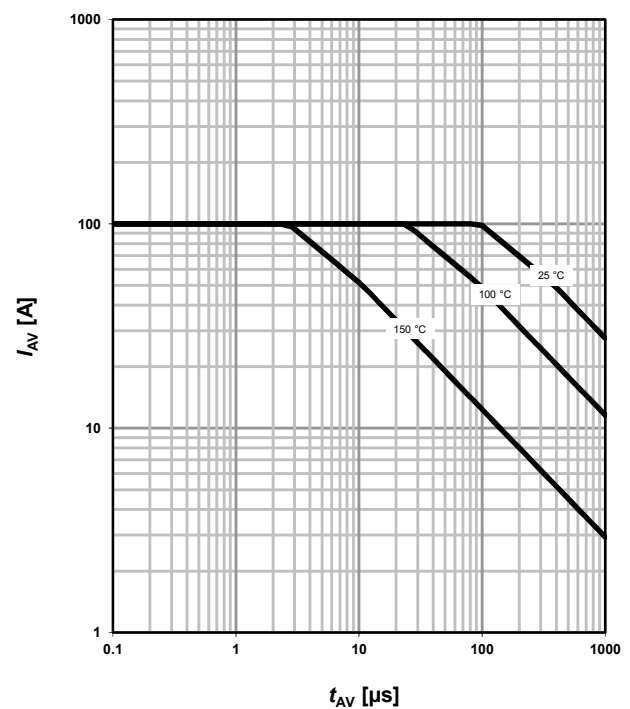
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$





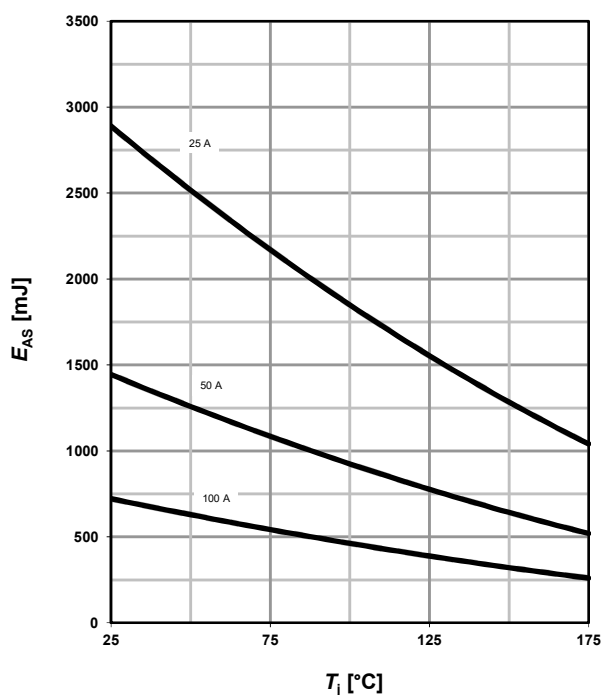
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13 Typical avalanche energy

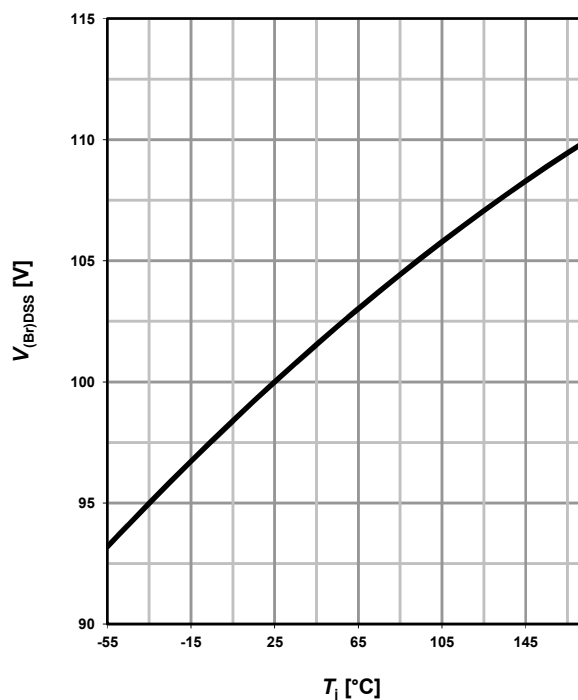
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Typ. drain-source breakdown voltage

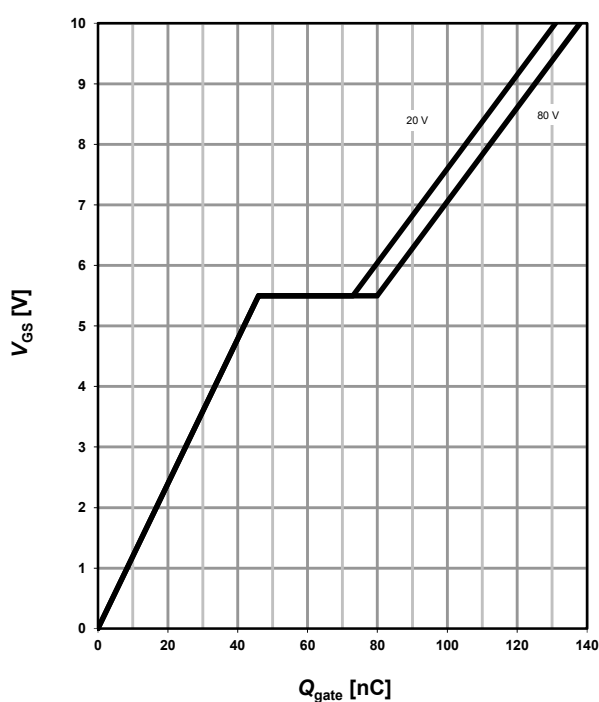
$$V_{(Br)DSS} = f(T_j); I_D = 1 \text{ mA}$$



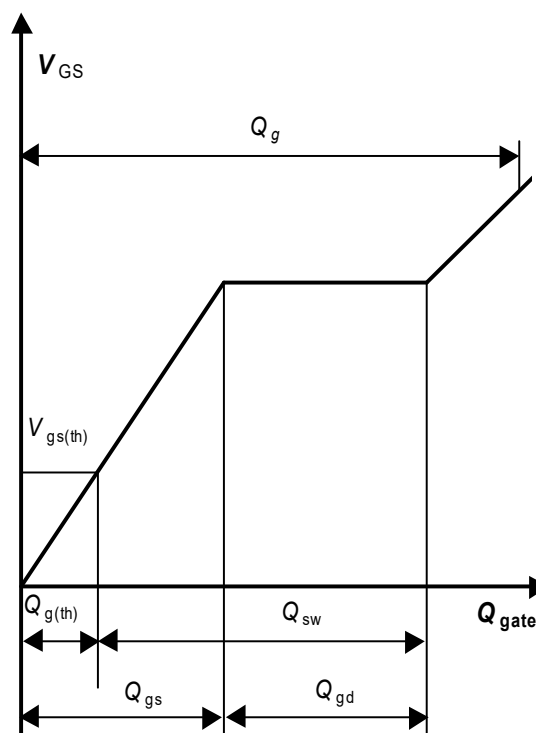
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 100 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Email: erratum@infineon.com

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Revision History

Version	Date	Changes
Rev 1.0	2008-02-11	Final Data Sheet
Rev 1.1	2023-06-15	Diagram 8 Typ. drain-source on-state resistance: used α value clarified
Rev 1.1	2023-06-15	Corrected diagram 3 safe operating area
Rev 1.1	2023-06-15	Corrected diagram 10 typical capacitances