



IPB70N10S3L-12

IPI70N10S3L-12, IPP70N10S3L-12

OptiMOS™-T Power-Transistor



Features

- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

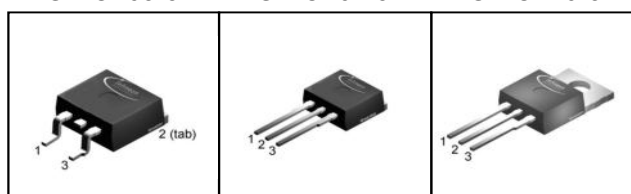
Product Summary

V_{DS}	100	V
$R_{DS(on),max}$ (SMD version)	12	mΩ
I_D	70	A

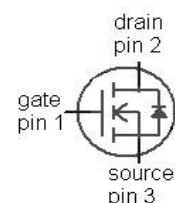
PG-TO263-3-2

PG-TO262-3-1

PG-TO220-3-1



Type	Package	Marking
IPB70N10S3L-12	PG-TO263-3-2	3N10L12
IPI70N10S3L-12	PG-TO262-3-1	3N10L12
IPP70N10S3L-12	PG-TO220-3-1	3N10L12



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	70	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	48	
		$T_C=25\text{ °C}$	280	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	280	
Avalanche energy, single pulse ¹⁾	E_{AS}	$I_D=35\text{ A}$	410	mJ
Avalanche current, single pulse	I_{AS}		70	A
Gate source voltage ²⁾	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	125	W
Operating and storage temperature	T_j , T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics¹⁾

Thermal resistance, junction - case	R_{thJC}		-	-	1.5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=83\mu\text{A}$	1.2	1.7	2.4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	0.1	10	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=70\text{ A}$	-	12.2	15.8	m Ω
		$V_{GS}=4.5\text{ V}, I_D=70\text{ A},$ SMD version	-	11.9	15.5	
		$V_{GS}=10\text{ V}, I_D=70\text{ A}$	-	10.1	12.1	
		$V_{GS}=10\text{ V}, I_D=70\text{ A},$ SMD version	-	9.8	11.8	



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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	4270	5570	pF
Output capacitance	C_{oss}		-	950	1230	
Reverse transfer capacitance	C_{rss}		-	90	135	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=50A, R_G=3.5\Omega$	-	10	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	28	-	
Fall time	t_f		-	5	-	

Gate Charge Characteristics¹⁾

Gate to source charge	Q_{gs}	$V_{DD}=80V, I_D=70A,$ $V_{GS}=0 \text{ to } 10V$	-	16	21	nC
Gate to drain charge	Q_{gd}		-	11	17	
Gate charge total	Q_g		-	60	80	
Gate plateau voltage	$V_{plateau}$		-	3.7	-	V

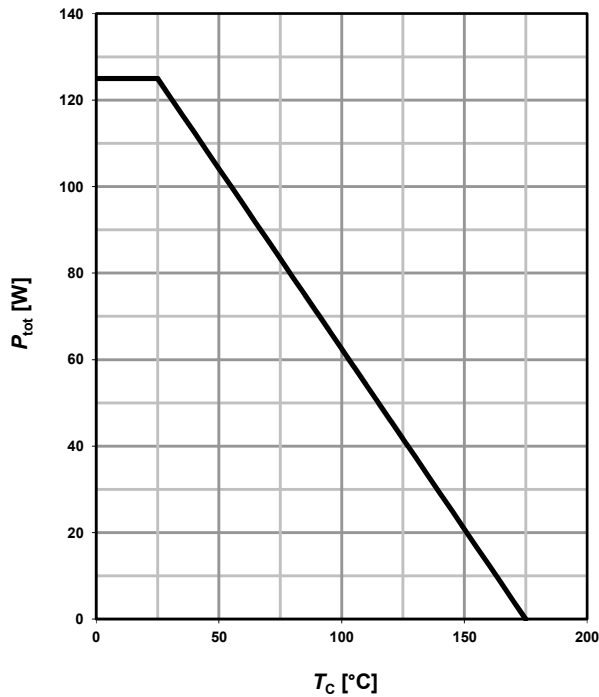
Reverse Diode

Diode continuous forward current ¹⁾	I_S	$T_C=25^\circ C$	-	-	70	A
Diode pulse current ¹⁾	$I_{S,pulse}$		-	-	280	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=70A,$ $T_j=25^\circ C$	0.6	1	1.2	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=50V, I_F=I_S,$ $di_F/dt=100A/\mu s$	-	80	-	ns
Reverse recovery charge ¹⁾	Q_{rr}		-	185	-	

¹⁾ Defined by design. Not subject to production test.²⁾ -5V to -20V for max. 168 non-consecutive hours³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

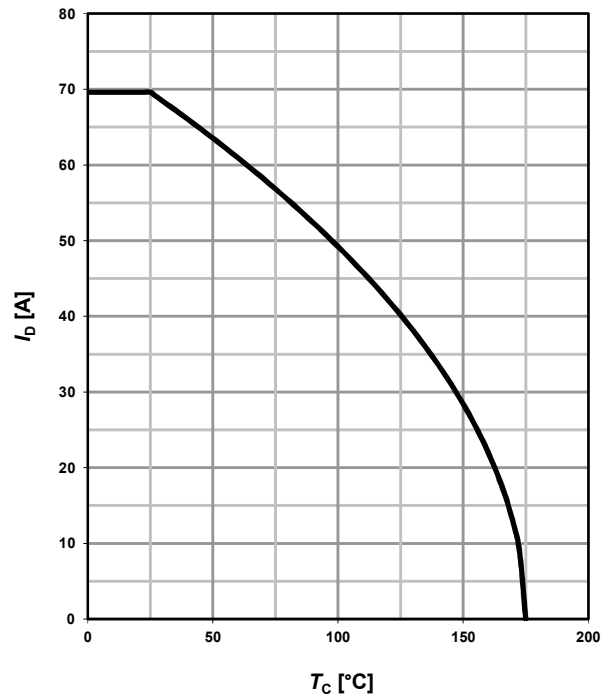
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

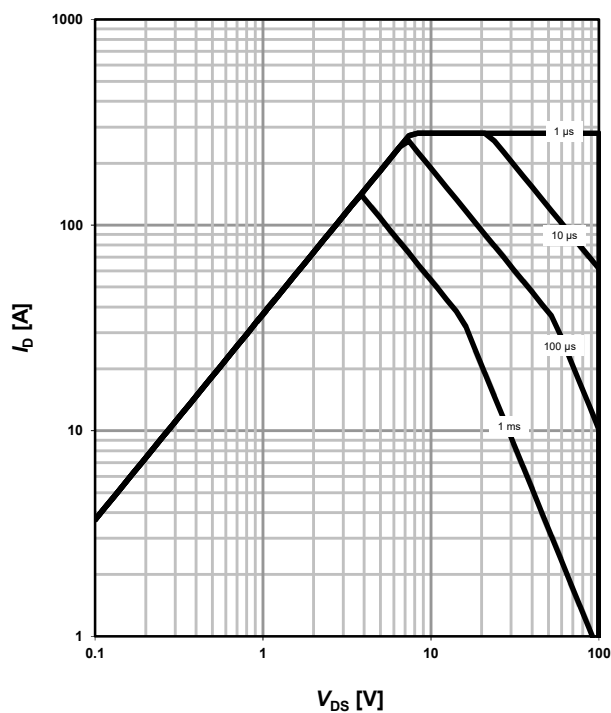
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}; \text{SMD}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0; \text{SMD}$$

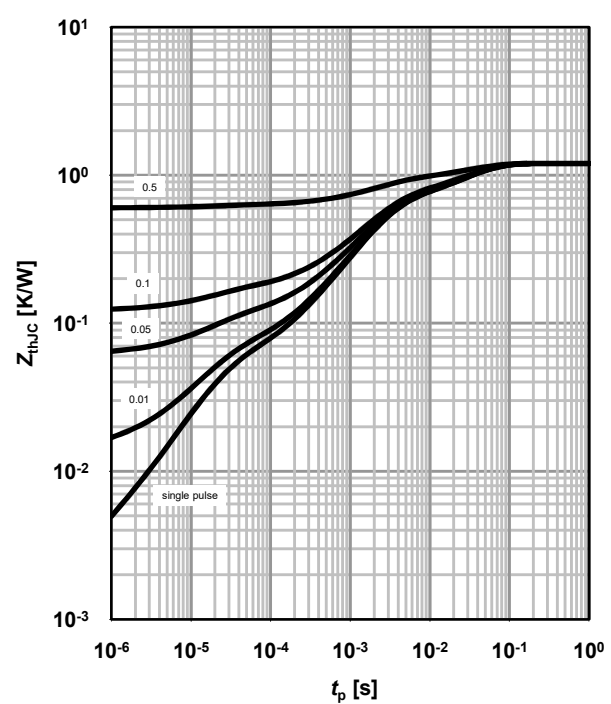
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

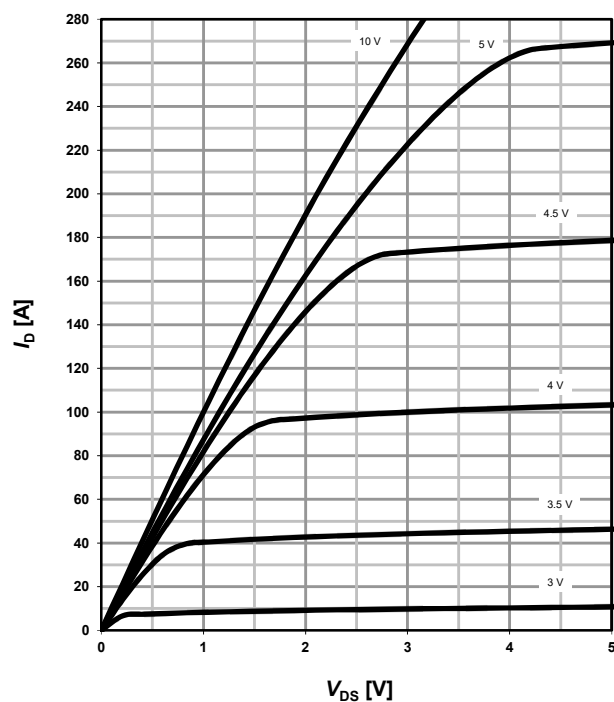
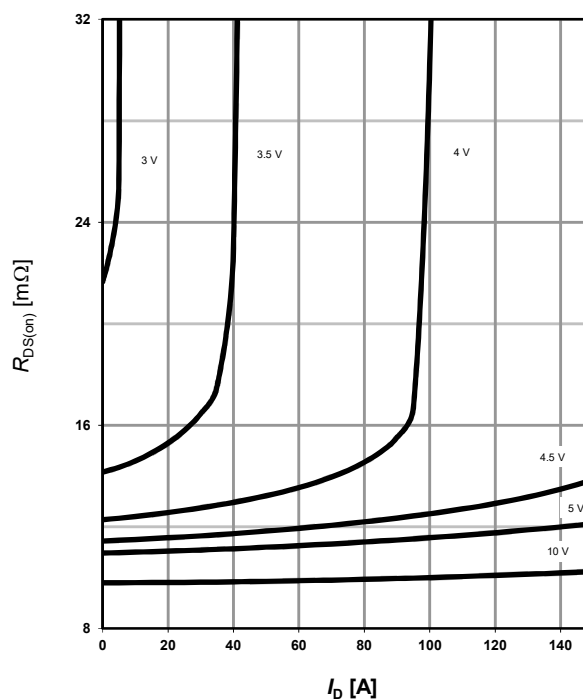
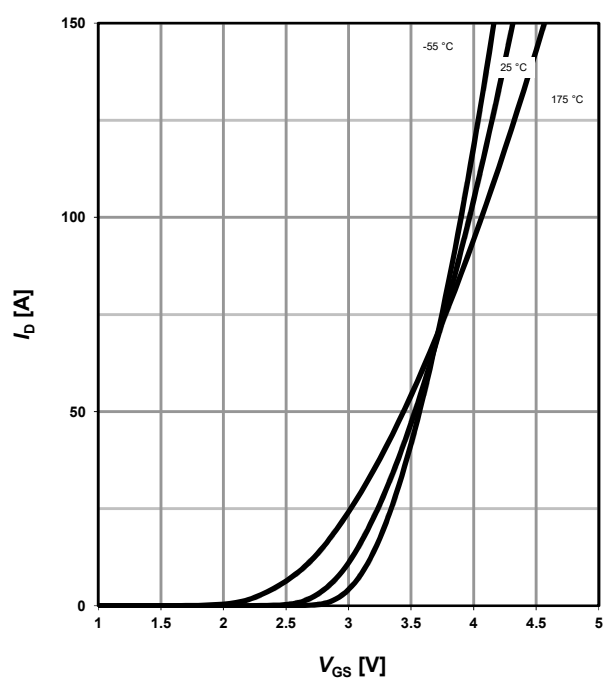
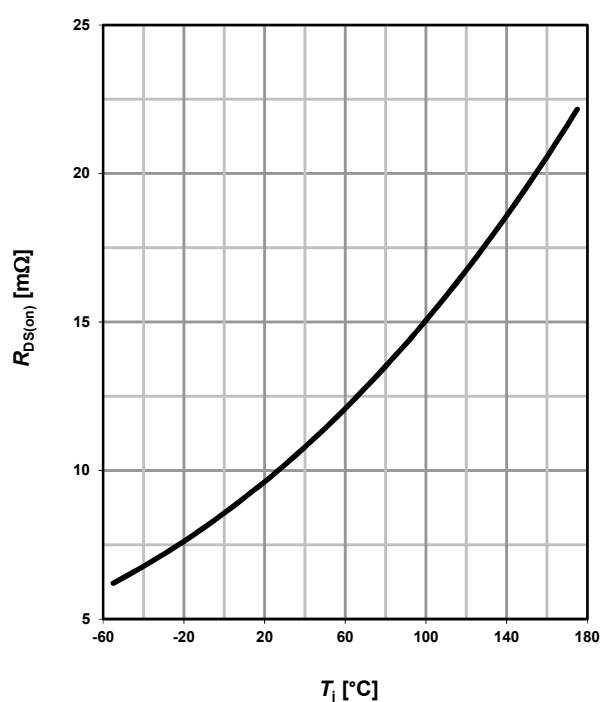
parameter: $D = t_p/T$





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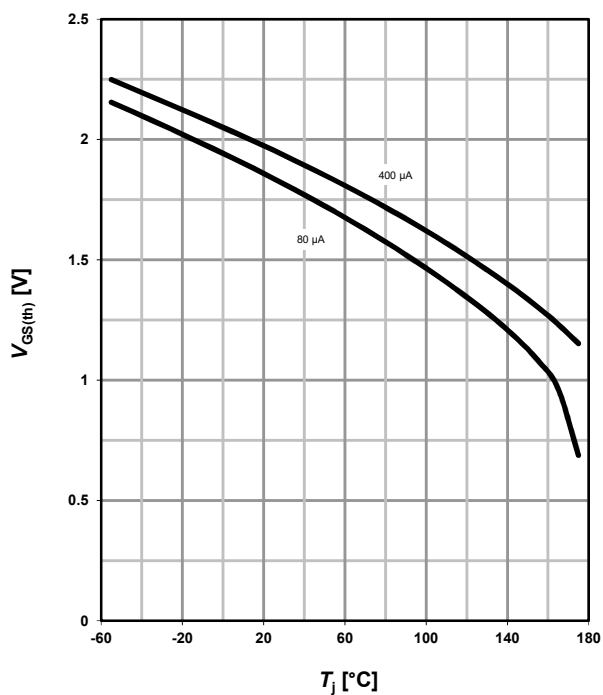
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5 Typ. output characteristics $I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{SMD}$ parameter: V_{GS} **6 Typ. drain-source on-state resistance** $R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{SMD}$ parameter: V_{GS} **7 Typ. transfer characteristics** $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$ parameter: T_j **8 Typ. drain-source on-state resistance** $R_{DS(on)} = f(T_j); I_D = 50\text{ A}; V_{GS} = 10\text{ V}; \text{SMD}$ $\alpha = 0.56$ 

9 Typ. gate threshold voltage

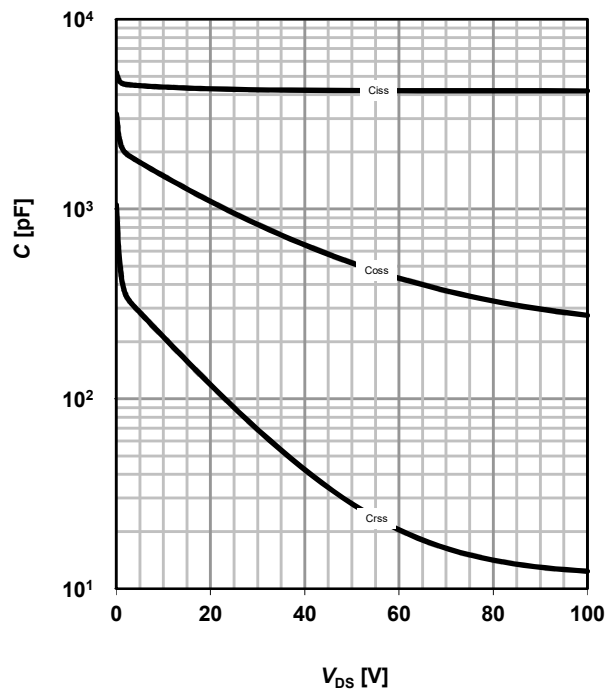
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

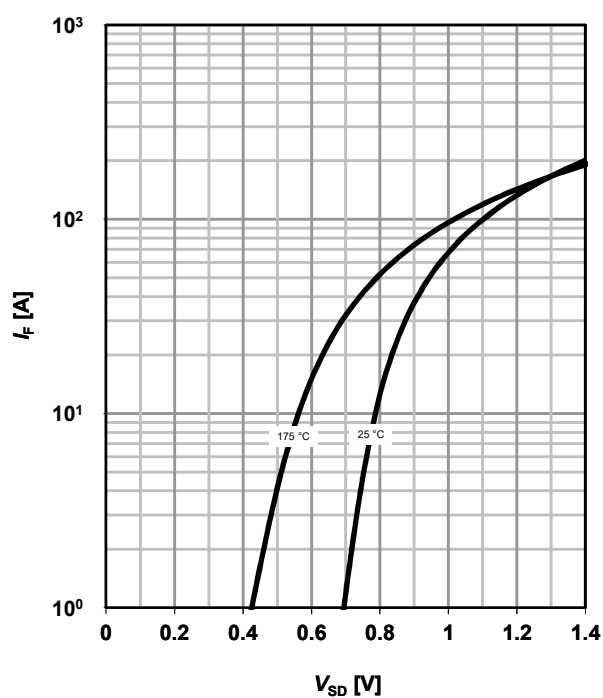
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

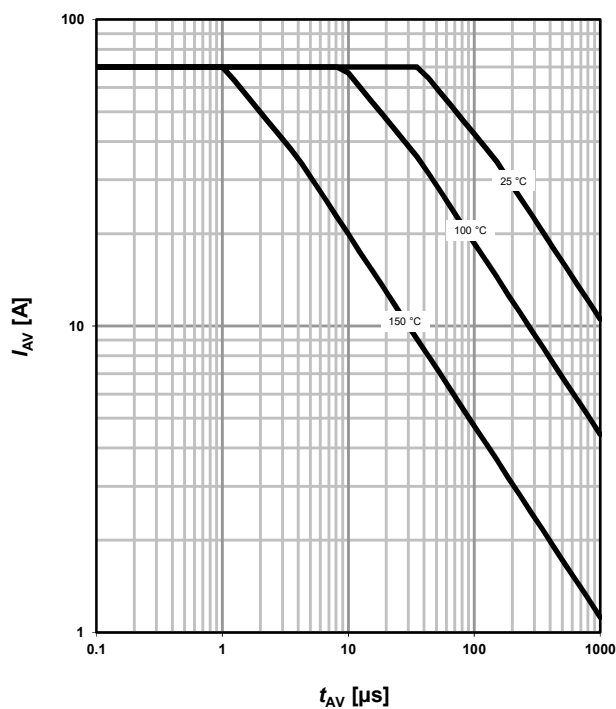
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$





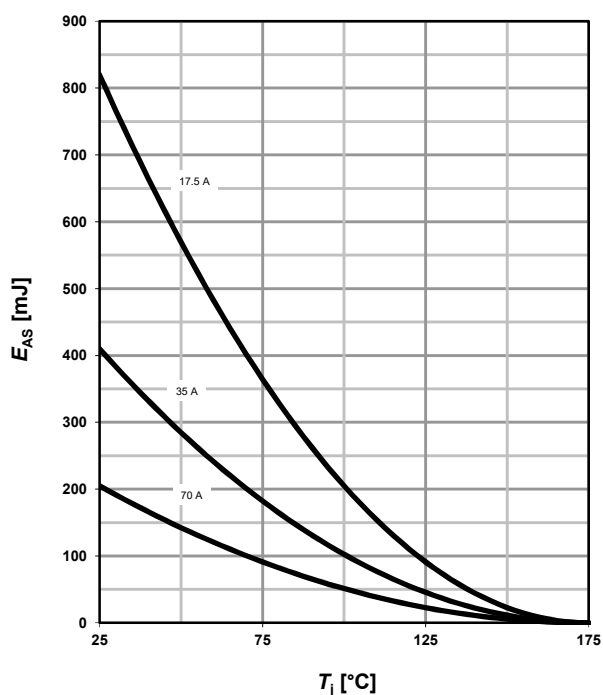
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13 Typical avalanche energy

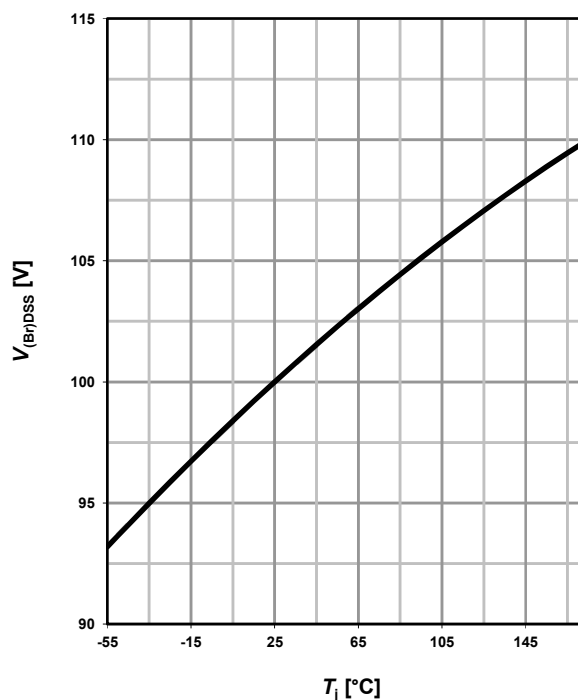
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Typ. drain-source breakdown voltage

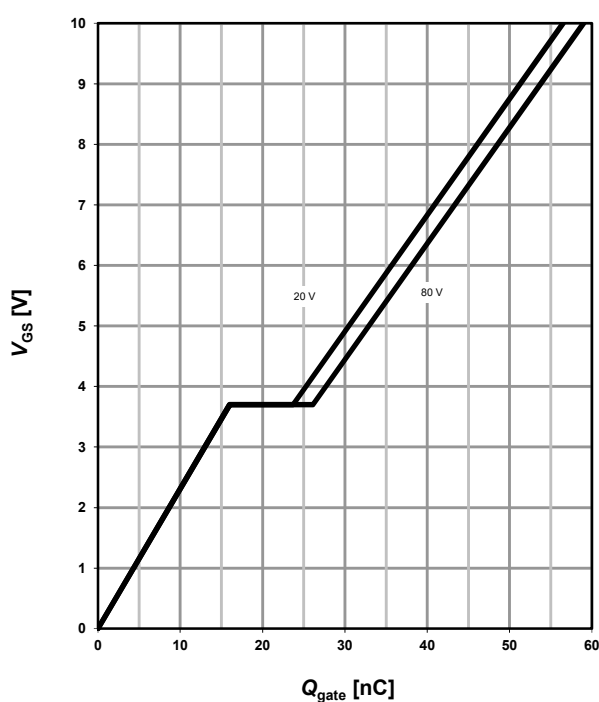
$$V_{(BR)DSS} = f(T_j); I_D = 1 \text{ mA}$$



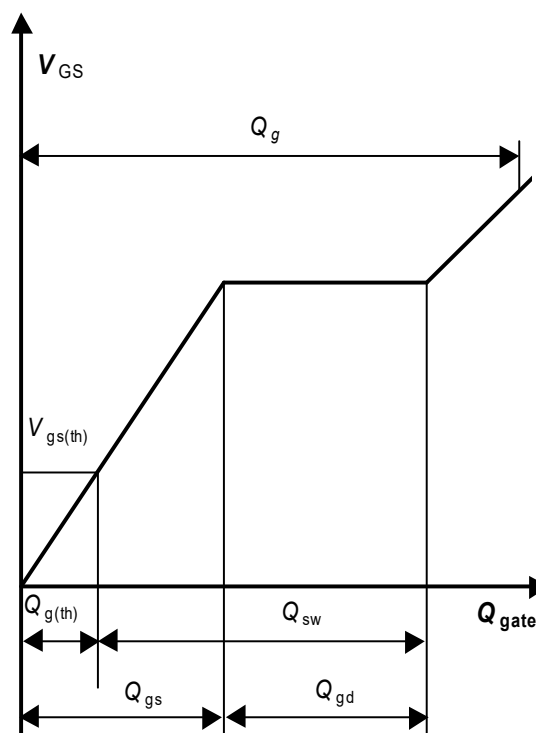
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 70 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Edition 2023-06-15

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

IPP_B_I70N10S3L-12-Data-Sheet-12-Infineon

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Revision History

Version	Date	Changes
Revision 1.1	2011-06-03	Update of I_{DSS}
Revision 1.2	2023-06-15	Diagram 8 Typ. drain-source on-state resistance: used α value clarified
Revision 1.2	2023-06-15	Ratings of Gate Source Voltage V_{GS} refined in footnote ²⁾
Revision 1.2	2023-06-15	Corrected diagram 3 safe operating area
Revision 1.2	2023-06-15	Corrected diagram 10 typical capacitances