

IPC313N10N3R

OptiMOS[™]3 Power MOS Transistor Chip

Туре	V _{(BR)DSS}	R _{DS(on)}	Die size	Thickness
IPC313N10N3R	100 V	$2.7~\text{m}\Omega^{1)}$	6 * 5.2 mm ²	220 μm

DESCRIPTION

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPB027N10N3 G²⁾
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to JEDEC
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlCu system
- Passivation: nitride (only on edge structure)

Electrical Characteristics on Wafer Level

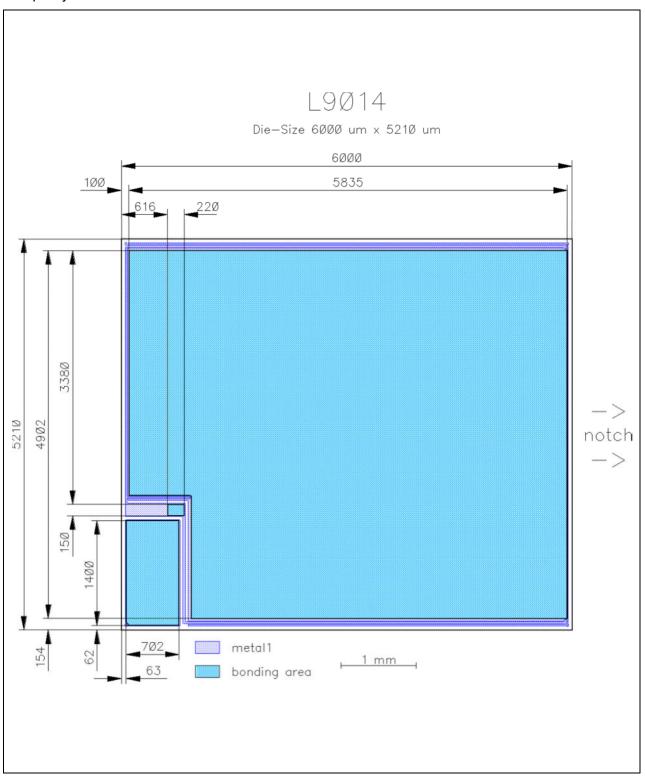
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Value			Unit	Conditions
		min.	typ.	max.		
Drain-source breakdown voltage	V _{(BR)DSS}	100	-	-	V	V _{GS} = 0V
						$I_D = 1 \text{ mA}$
Gate threshold voltage	V _{GS(th)}	2	2.7	3.5	V	$V_{DS} = V_{GS}$
						I _D = 275 μA
Zero gate voltage drain current	I _{DSS}	-	0.1	1	μΑ	V _{GS} = 0V
						V _{DS} = 100 V
Gate-source leakage current	I _{GSS}	-	1	100	nA	V _{GS} = 20 V
						$V_{DS} = 0 V$
Drain-source on-resistance	R _{DS(on)}	-	1.9 ³⁾	100 4)	mΩ	V _{GS} = 10 V
						I _D = 2.0 A
Reverse diode forward on-voltage	V SD	-	1.0	1.2	V	V _{GS} =0 V
						I _F = 1 A
Internal gate resistance	R G	-	8	-	Ω	
Avalanche energy, single pulse	E AS	-	45 ⁵⁾	-	mJ	$I_D = 30 \text{ A}, R_{GS} = 25 \Omega$



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Chip-Layout:



¹⁾ packaged in a P-TO263-3 (see ref. product)

 $^{^{2)}\,\}text{IPB027N10N3}$ G dynamic characterization does not include the internal added R_{G}

 $^{^{3)}}typical bare die <math display="inline">R_{\text{DS(on)}};\,V_{\text{GS}}\text{=}10V$

⁴⁾ limited by wafer test-equipment

⁵⁾Wafer tested. For general avalanche capability refer to the datasheet of IPB027N10N3 G



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