



IPD50N06S4L-08

OptiMOS[®] -T2 Power-Transistor



Features

- N-channel - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

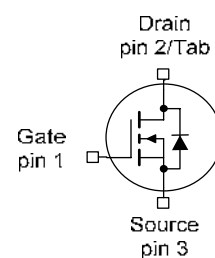
Product Summary

V_{DS}	60	V
$R_{DS(on),max}$	7.8	mΩ
I_D	50	A

PG-TO252-3-11



Type	Package	Marking
IPD50N06S4L-08	PG-TO252-3-11	4N06L08



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	50	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}$ ²⁾	47	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	200	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=25\text{ A}$	87	mJ
Avalanche current, single pulse	I_{AS}	-	50	A
Gate source voltage	V_{GS}	-	±16	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	71	W
Operating and storage temperature	T_j , T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	-

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	2.1	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=35\mu A$	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	0.01	1	μA
		$V_{DS}=60V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	5	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=16V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=25A$	-	9.0	13.5	m Ω
		$V_{GS}=10V, I_D=50A$	-	6.3	7.8	



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	3680	4780	pF
Output capacitance	C_{oss}		-	840	1090	
Reverse transfer capacitance	C_{rss}		-	40	80	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V,$ $I_D=50A, R_G=3.5\Omega$	-	9	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	45	-	
Fall time	t_f		-	8	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=48V, I_D=50A,$ $V_{GS}=0 \text{ to } 10V$	-	13	19	nC
Gate to drain charge	Q_{gd}		-	5	10	
Gate charge total	Q_g		-	49	64	
Gate plateau voltage	$V_{plateau}$		-	3.6	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	50	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=50A,$ $T_j=25^\circ C$	0.6	0.95	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=30V, I_F=I_S,$ $di_F/dt=100A/\mu s$	-	33	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	32	-	nC

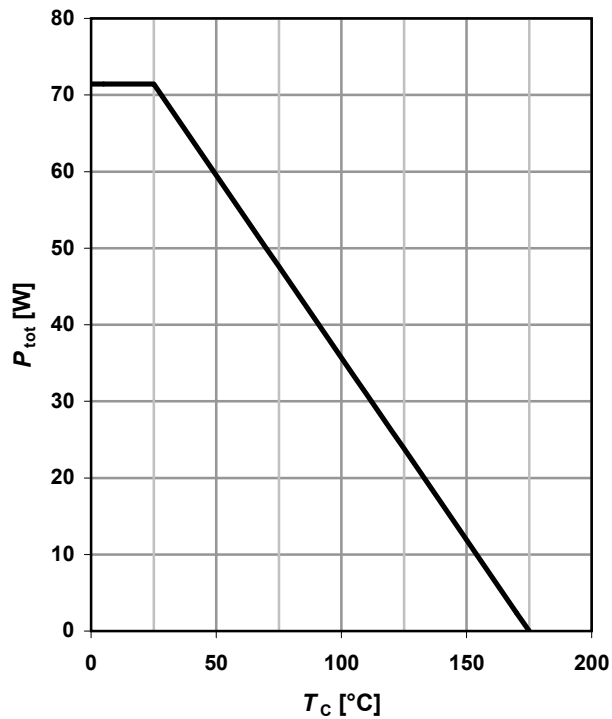
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 2.1K/W$ the chip is able to carry 65A at 25°C.

²⁾ Specified by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

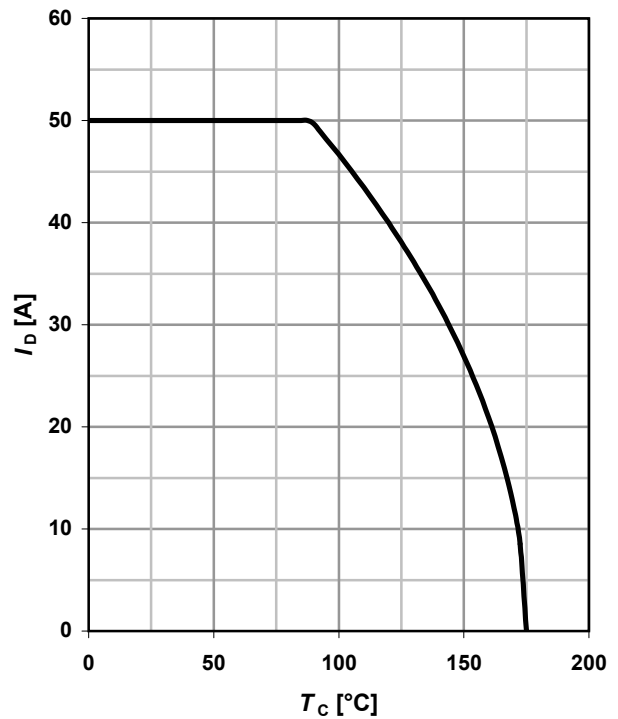
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

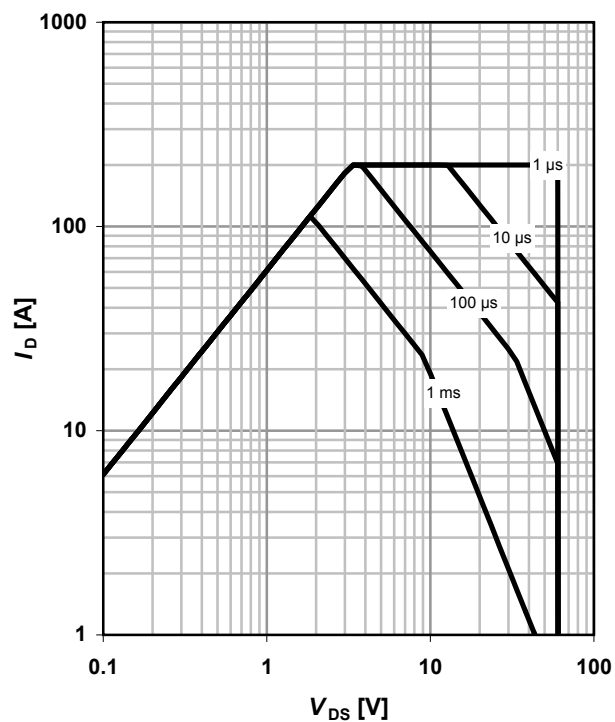
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

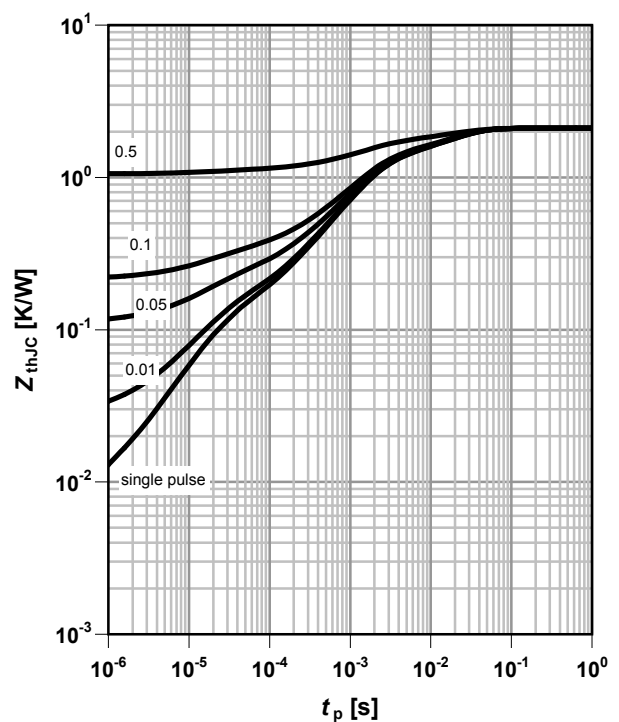
parameter: t_p



4 Max. transient thermal impedance

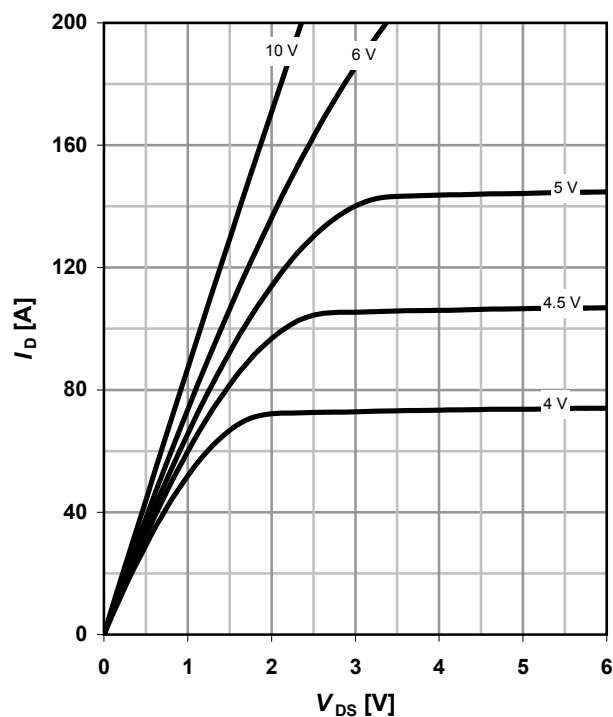
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$

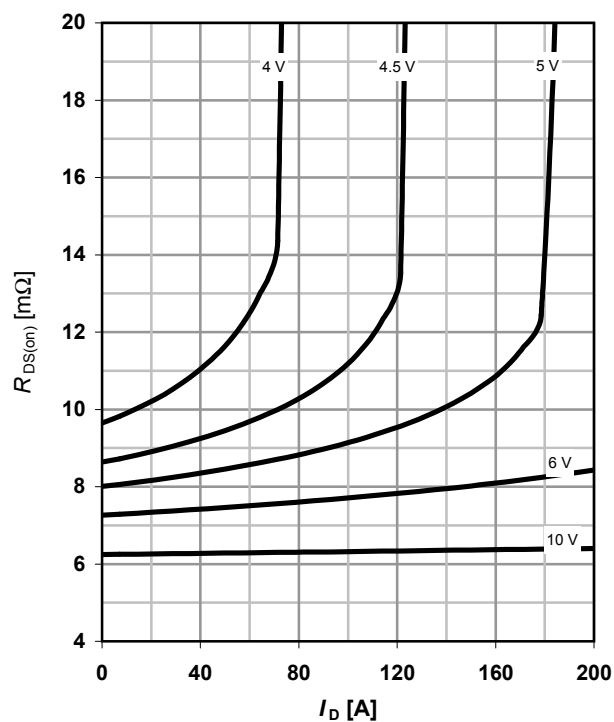


5 Typ. output characteristics

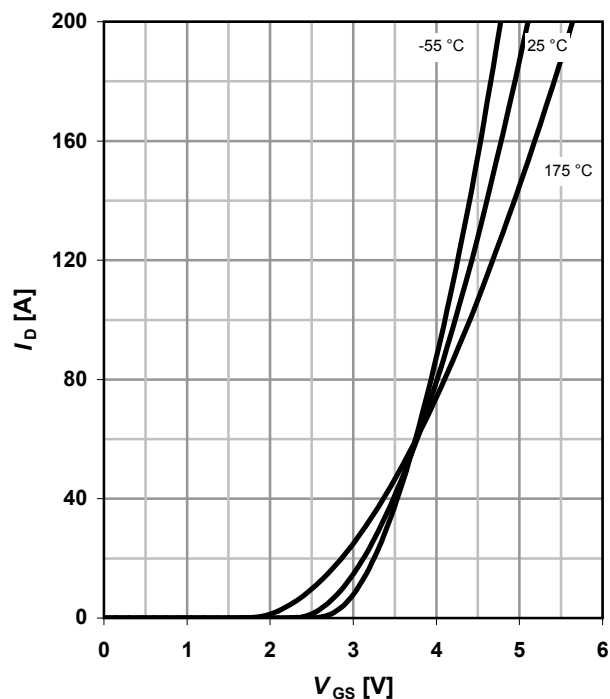
$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

parameter: V_{GS} **6 Typ. drain-source on-state resistance**

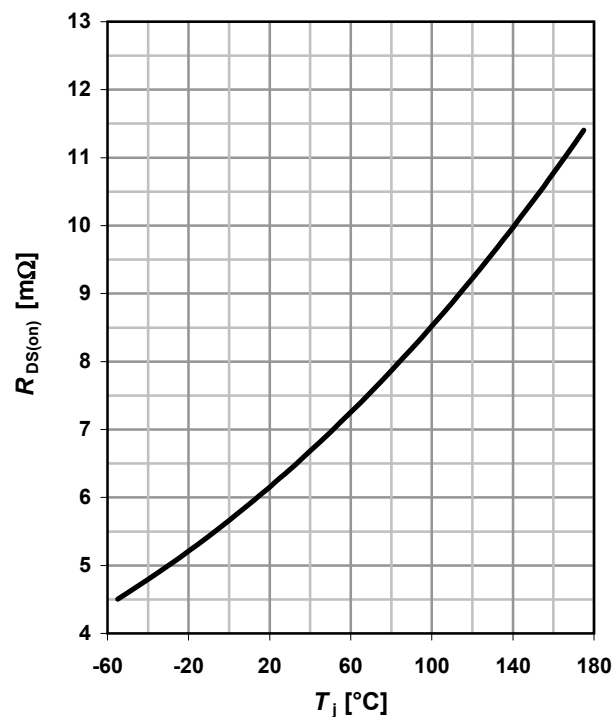
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

parameter: V_{GS} **7 Typ. transfer characteristics**

$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

parameter: T_j **8 Typ. drain-source on-state resistance**

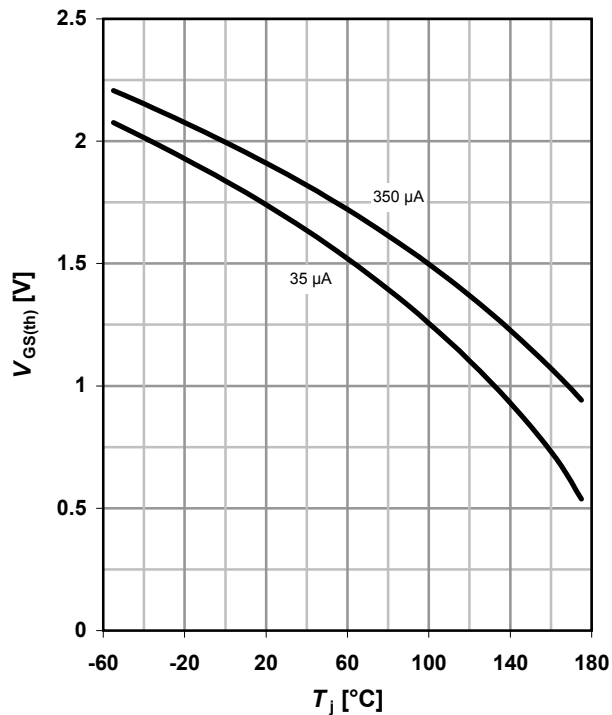
$$R_{DS(on)} = f(T_j); I_D = 50\text{ A}; V_{GS} = 10\text{ V}$$



9 Typ. gate threshold voltage

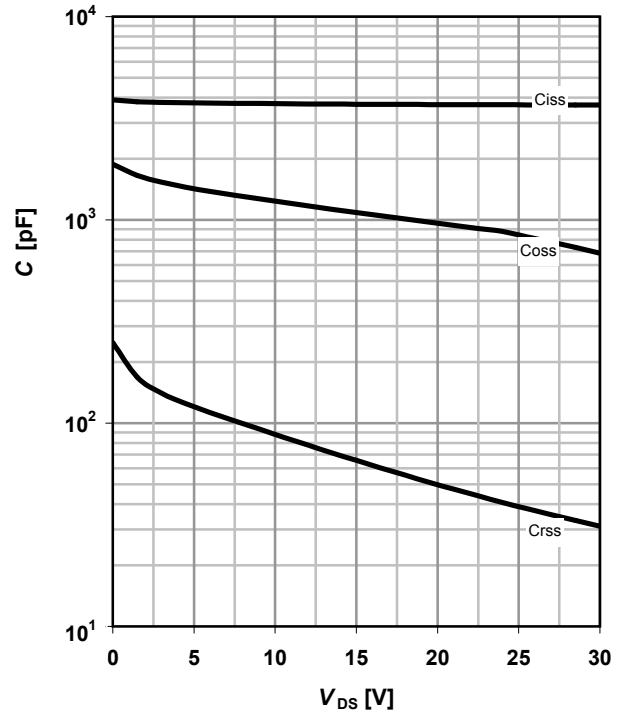
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

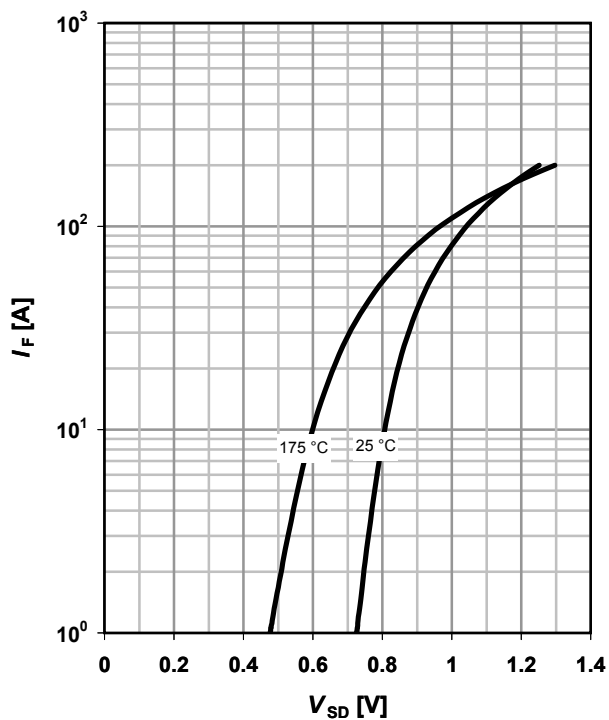
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

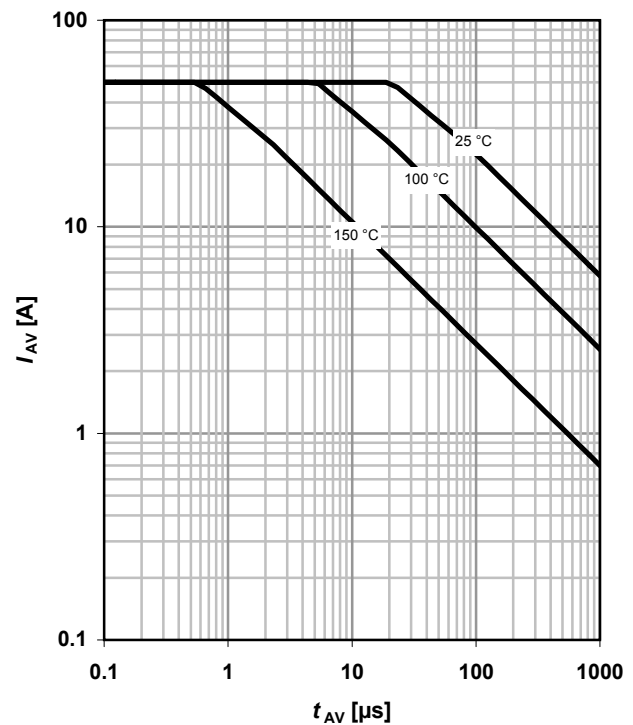
parameter: T_j



12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

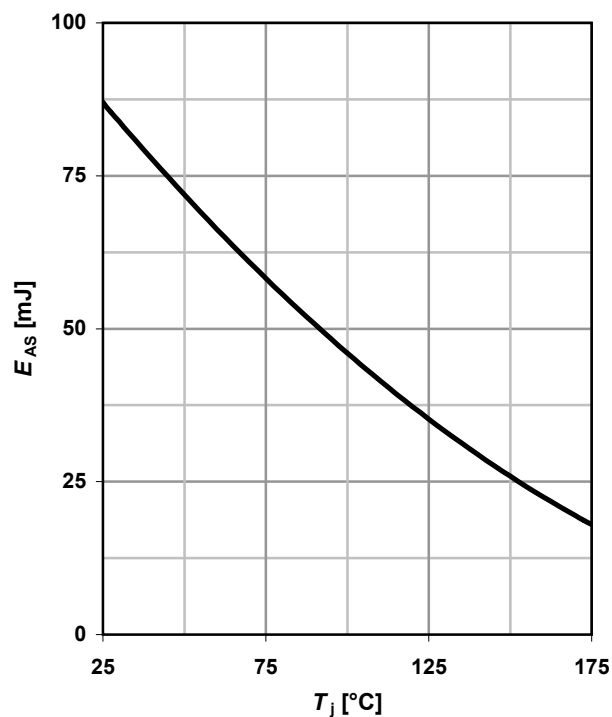
parameter: $T_{j(start)}$





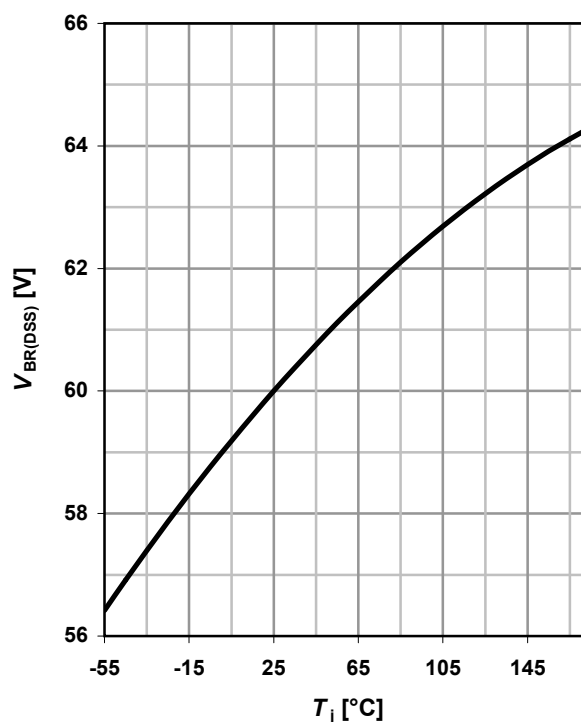
13 Avalanche energy

$$E_{AS} = f(T_j); I_D = 25 \text{ A}$$



14 Drain-source breakdown voltage

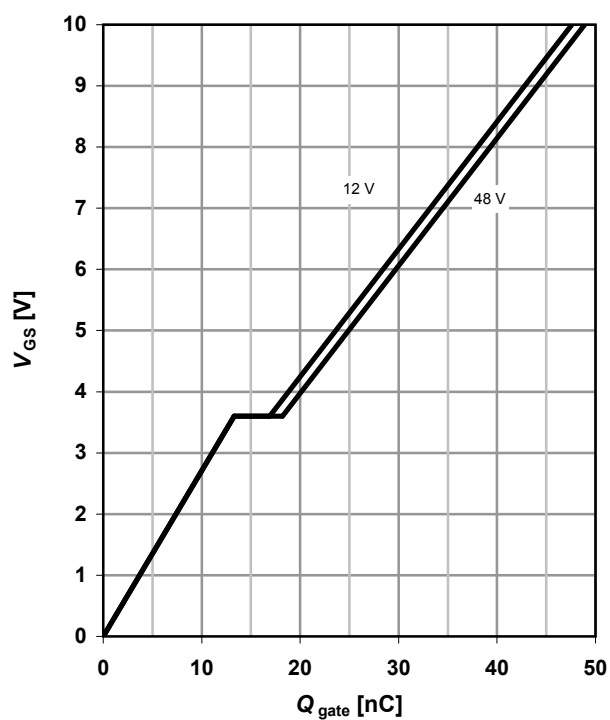
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



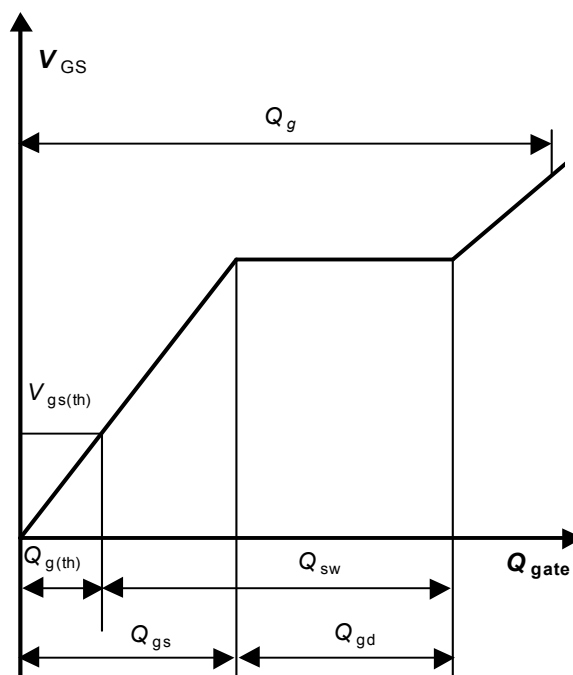
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 50 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	24.03.2009	Final data sheet