



OptiMOS®-P2 Power-Transistor



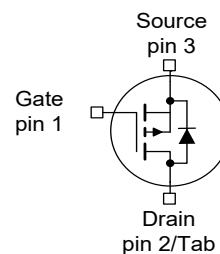
Features

- P-channel - Normal Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	-40	V
$R_{DS(on)}$	12.6	mΩ
I_D	-50	A

PG-TO252-3-313



Type	Package	Marking
IPD50P04P4-13	PG-TO252-3-313	4P0413

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=-10\text{ V}$	-50	A
		$T_C=100\text{ °C}$, $V_{GS}=-10\text{ V}^{2)}$	-45	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	-200	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=-25\text{ A}$	18	mJ
Avalanche current, single pulse	I_{AS}	-	-50	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	58	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	2.6	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-1mA$	-40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-85\mu A$	-2.0	-3.0	-4.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-32V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-0.05	-1	μA
		$V_{DS}=-32V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-20	-200	
Gate-source leakage current	I_{GSS}	$V_{GS}=-20V, V_{DS}=0V$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-50A$	-	9.2	12.6	m Ω



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$	-	2820	3670	pF
Output capacitance	C_{oss}		-	1000	1500	
Reverse transfer capacitance	C_{rss}		-	30	60	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-20V,$ $V_{GS}=-10V, I_D=-50A,$ $R_G=3.5\Omega$	-	17	-	ns
Rise time	t_r		-	10	-	
Turn-off delay time	$t_{d(off)}$		-	22	-	
Fall time	t_f		-	28	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-32V, I_D=-50A,$ $V_{GS}=0 \text{ to } -10V$	-	14	19	nC
Gate to drain charge	Q_{gd}		-	7	14	
Gate charge total	Q_g		-	39	51	
Gate plateau voltage	$V_{plateau}$		-	5.4	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	-50	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	-200	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=-50A,$ $T_j=25^\circ C$	-	-1	-1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=-20V, I_F=-50A,$ $di_F/dt=-100A/\mu s$	-	39	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	32	-	nC

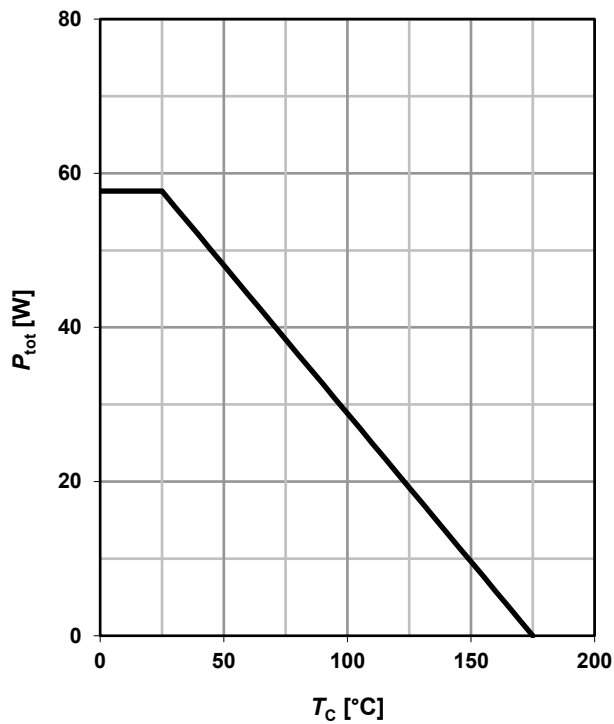
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 2.6K/W$ the chip is able to carry -55A at 25°C.

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

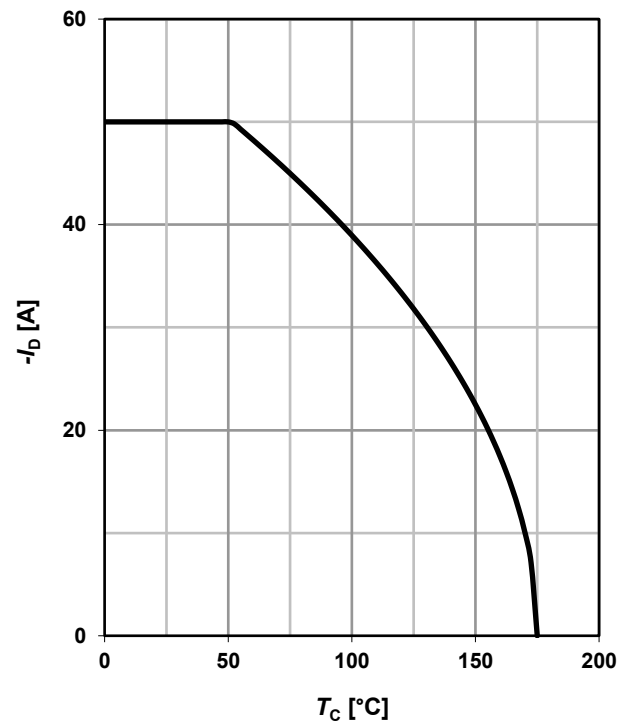
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = -10\text{V}$$



2 Drain current

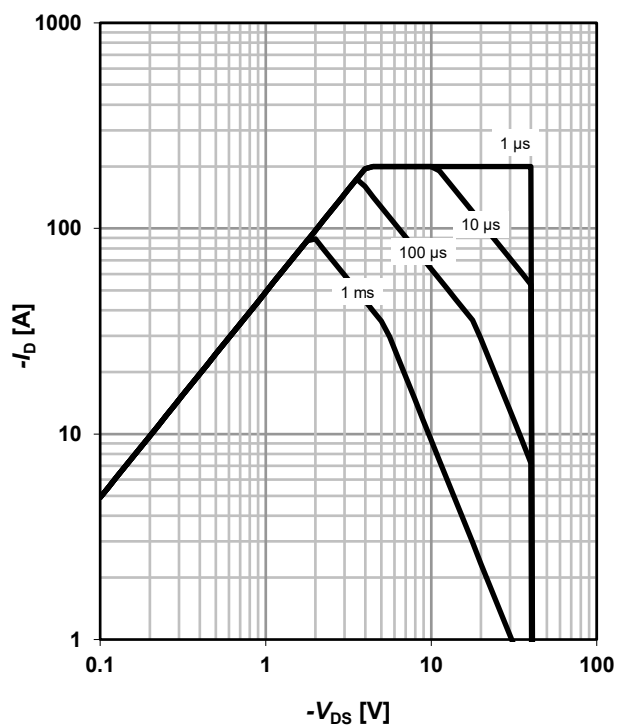
$$I_D = f(T_C); V_{\text{GS}} = -10\text{V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

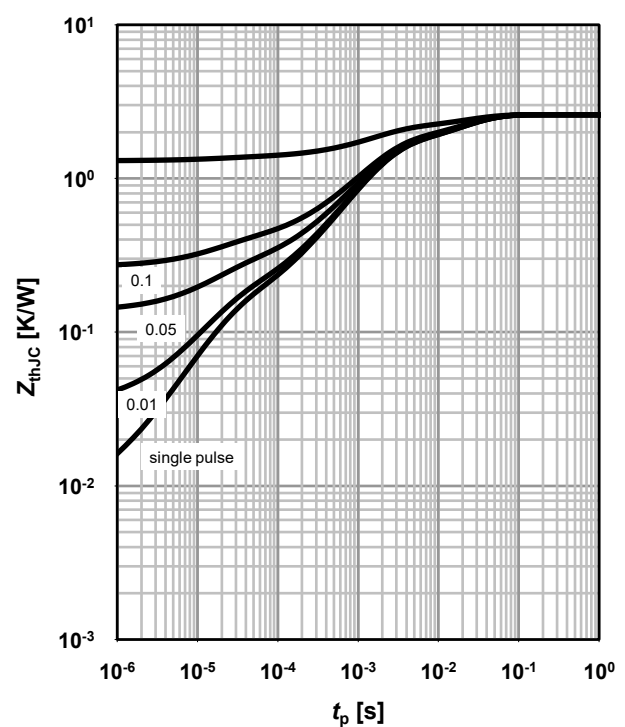
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

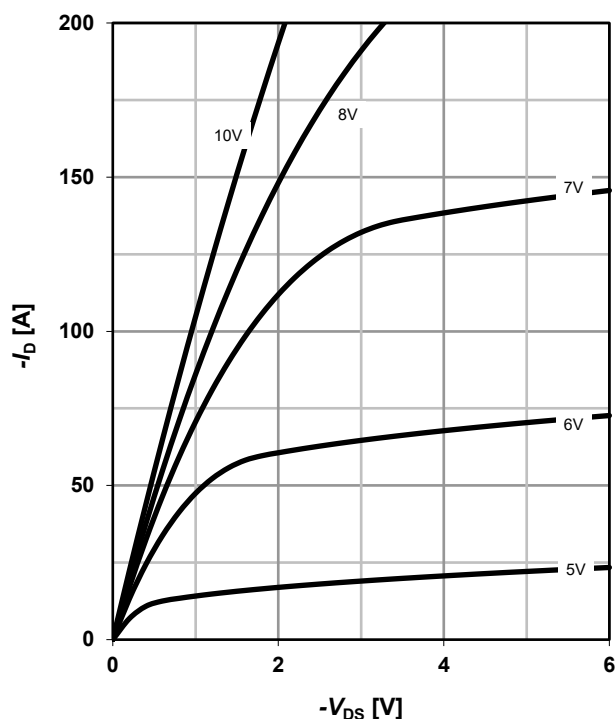
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

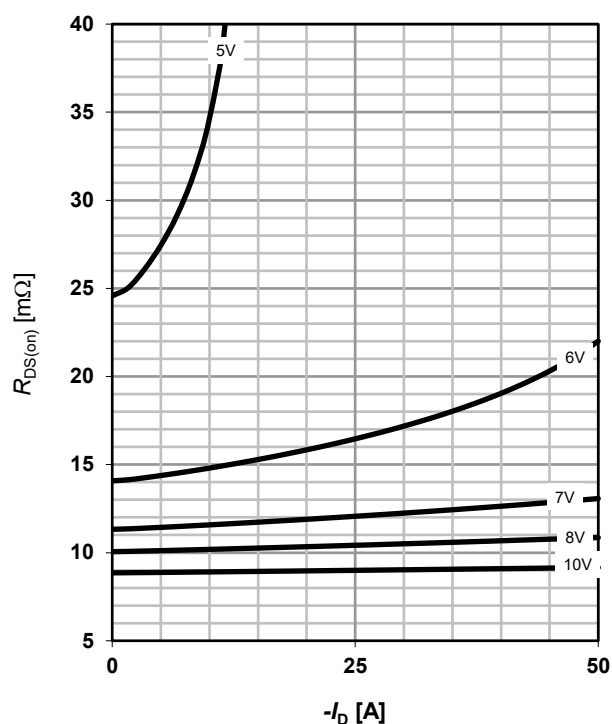
parameter: $-V_{GS}$



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

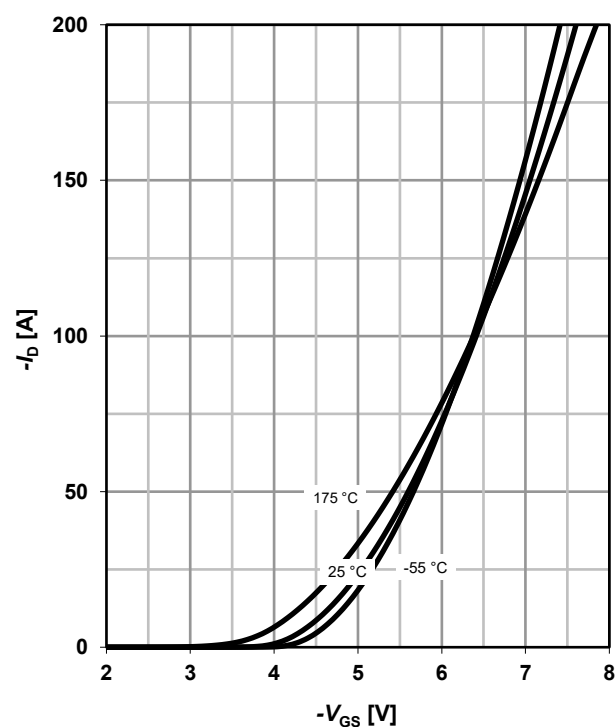
parameter: $-V_{GS}$



7 Typ. transfer characteristics

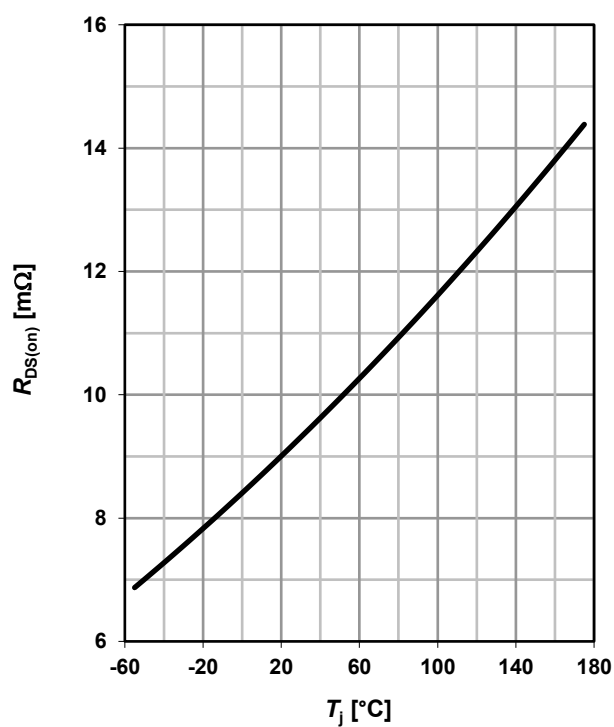
$I_D = f(V_{GS}); V_{DS} = -6V$

parameter: T_j



8 Typ. drain-source on-state resistance

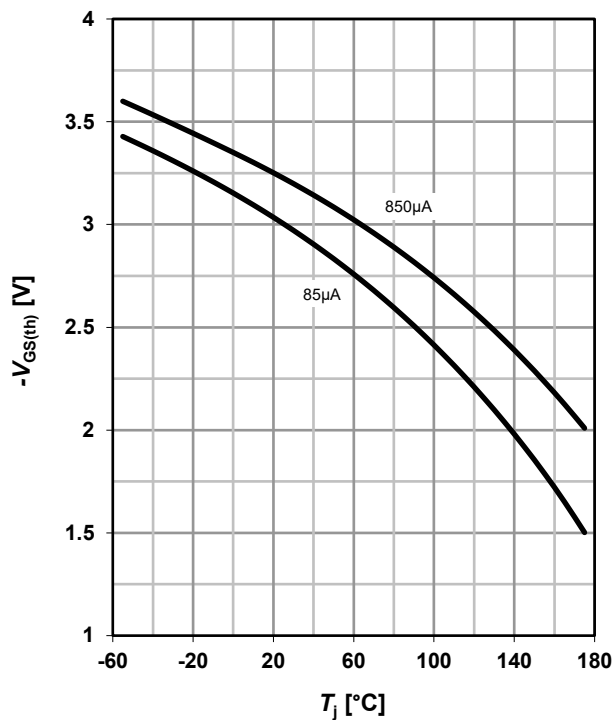
$R_{DS(on)} = f(T_j); I_D = -50\text{ A}; V_{GS} = -10\text{ V}$



9 Typ. gate threshold voltage

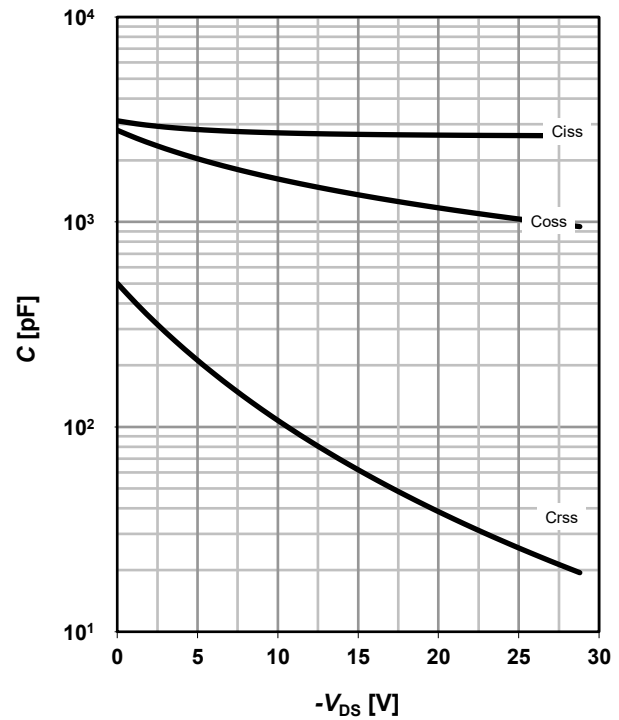
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: $-I_D$



10 Typ. capacitances

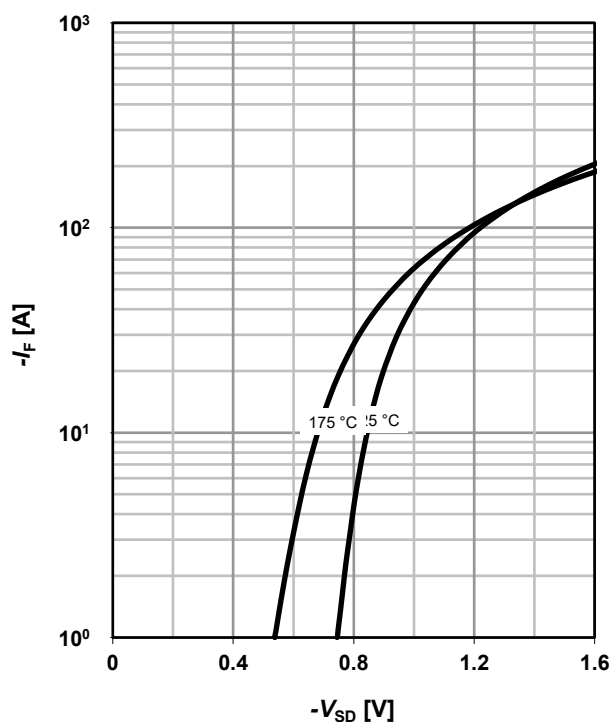
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

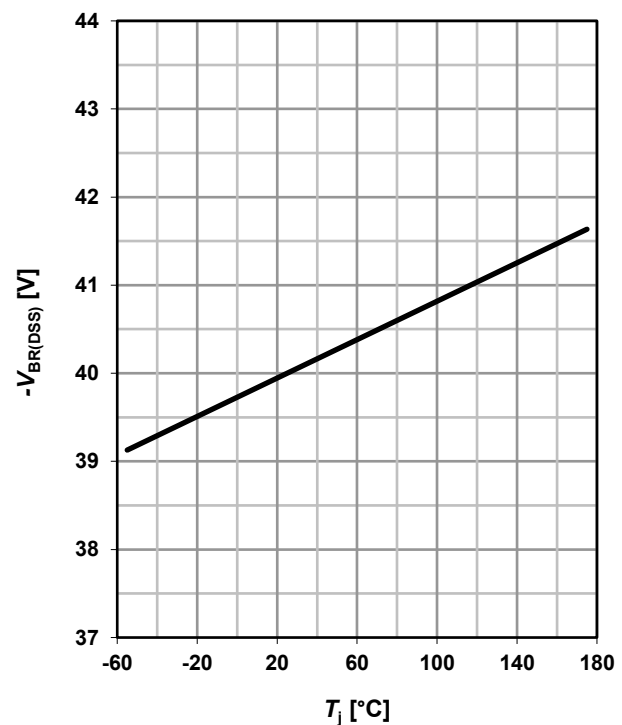
$$I_F = f(V_{SD})$$

parameter: T_j



12 Drain-source breakdown voltage

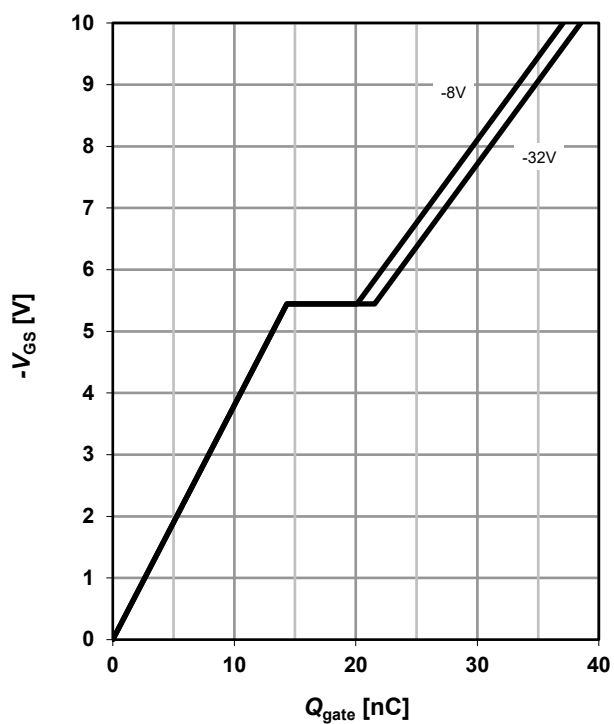
$$V_{BR(DSS)} = f(T_j); I_D = -1 mA$$



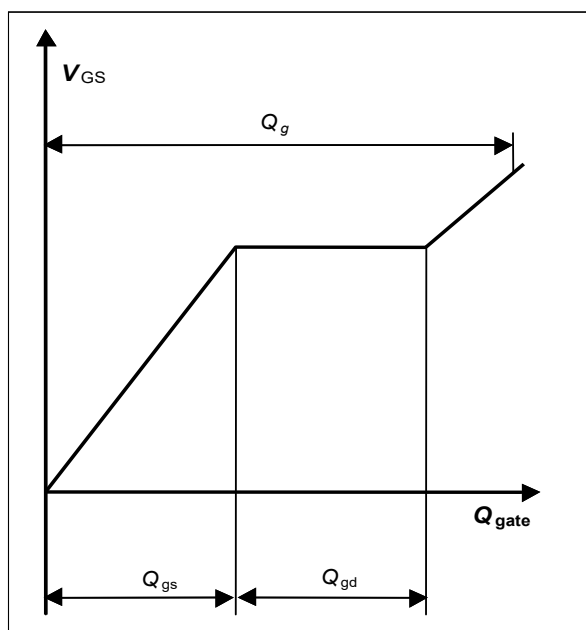
13 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = -50 \text{ A pulsed}$

parameter: V_{DD}



14 Gate charge waveforms



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Revision History

Version	Date	Changes
1.0	14.03.2011	Final Data Sheet
1.1	21.12.2012	Update of diagram 8
1.2	09.12.2013	Update of Idpuls and SOA
1.3	16.07.2019	graphs corrected