

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CE

500V CoolMOS™ CE Power Transistor
IPD50R500CE

Data Sheet

Rev. 2.2
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

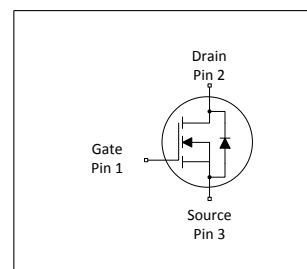
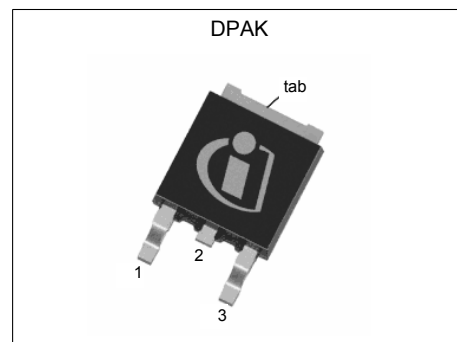


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	550	V
$R_{DS(on),max}$	0.5	Ω
$Q_{g,typ}$	18.7	nC
$I_{D,pulse}$	24	A
$E_{oss}@400V$	2.02	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPD50R500CE	PG-TO 252	50S500CE	see Appendix A

Table of Contents

Description	2
Maximum ratings	4
Thermal characteristics	4
Electrical characteristics	5
Electrical characteristics diagrams	7
Test Circuits	11
Package Outlines	12
Appendix A	13
Revision History	14
Disclaimer	14

2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	7.6 4.8	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	24	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	129	mJ	$I_D = 2.9\text{A}$; $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.20	mJ	$I_D = 2.9\text{A}$; $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}	-	-	2.9	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation (non FullPAK) TO-252	P_{tot}	-	-	57	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	6.6	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	24.0	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$
Maximum diode commutation speed ³⁾	di/dt	-	-	500	A/ μs	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$

3 Thermal characteristics

Table 3 Thermal characteristics DPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.19	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	-	- 35	62 -	$^\circ\text{C/W}$	SMD version, device on PCB, minimal footprint SMD version, device on PCB, 6cm ² cooling area ⁴⁾
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}	-	-	260	$^\circ\text{C}$	reflow MSL 1

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DCLink}=400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G

⁴⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70 μm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	$V_{DS}=V_{GS}$, $I_D=0.2mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=500V$, $V_{GS}=0V$, $T_j=25^\circ C$ $V_{DS}=500V$, $V_{GS}=0V$, $T_j=150^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.45	0.50	Ω	$V_{GS}=13V$, $I_D=2.3A$, $T_j=25^\circ C$ $V_{GS}=13V$, $I_D=2.3A$, $T_j=150^\circ C$
Gate resistance	R_G	-	3	-	Ω	$f=1\text{ MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	433	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Output capacitance	C_{oss}	-	31	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	25	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	100	-	pF	$I_D=constant$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.9A$, $R_G=3.4\Omega$
Rise time	t_r	-	5	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.9A$, $R_G=3.4\Omega$
Turn-off delay time	$t_{d(off)}$	-	30	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.9A$, $R_G=3.4\Omega$
Fall time	t_f	-	12	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=2.9A$, $R_G=3.4\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2.3	-	nC	$V_{DD}=400V$, $I_D=2.9A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	10	-	nC	$V_{DD}=400V$, $I_D=2.9A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	18.7	-	nC	$V_{DD}=400V$, $I_D=2.9A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	$V_{DD}=400V$, $I_D=2.9A$, $V_{GS}=0$ to $10V$

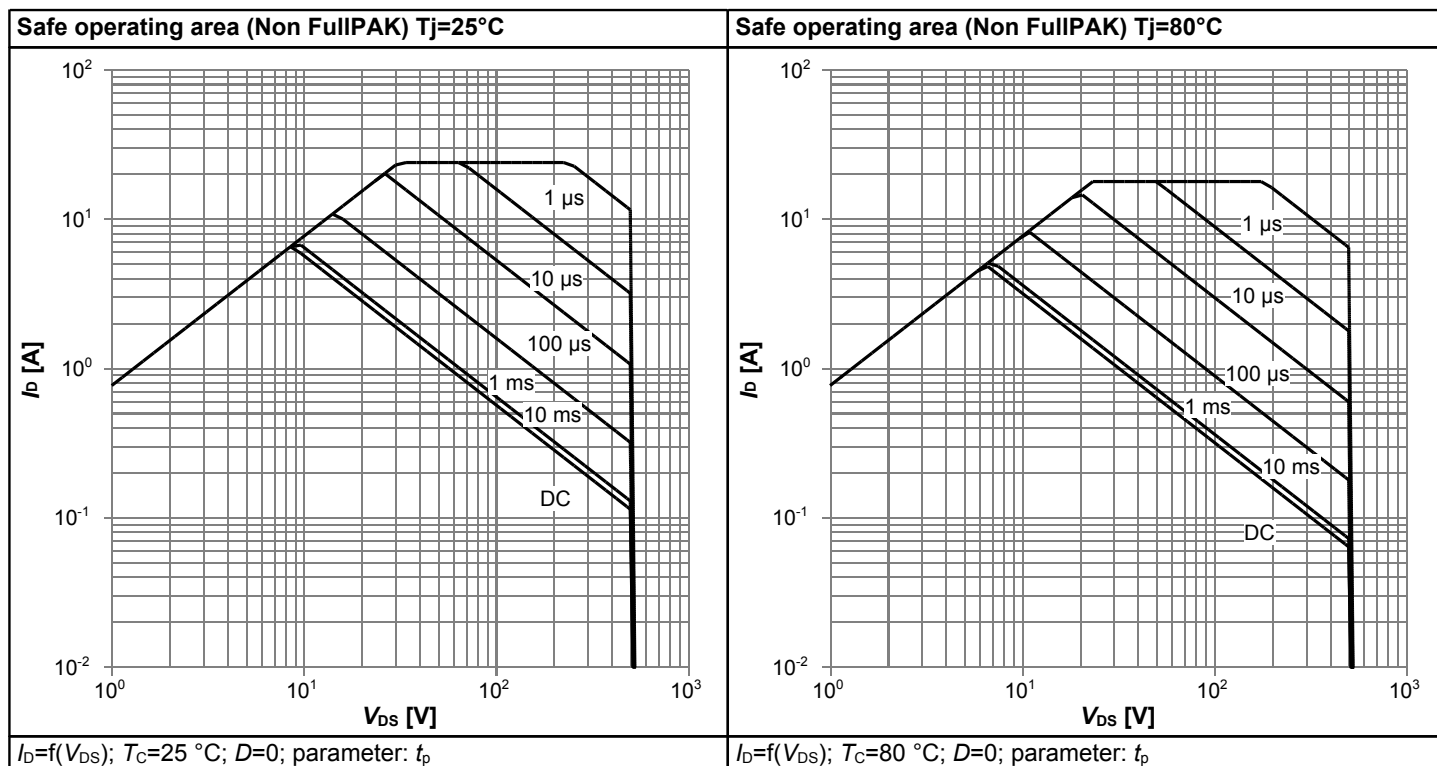
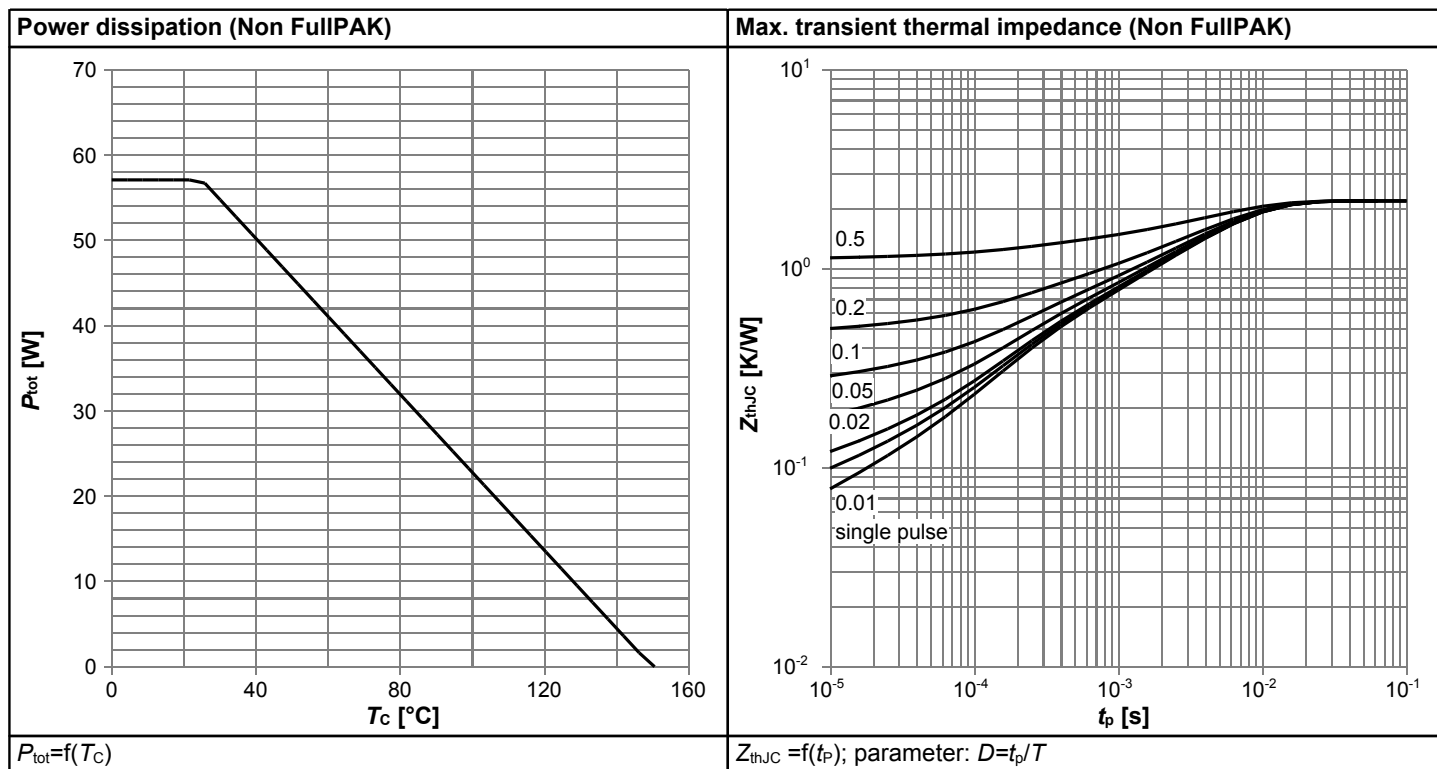
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

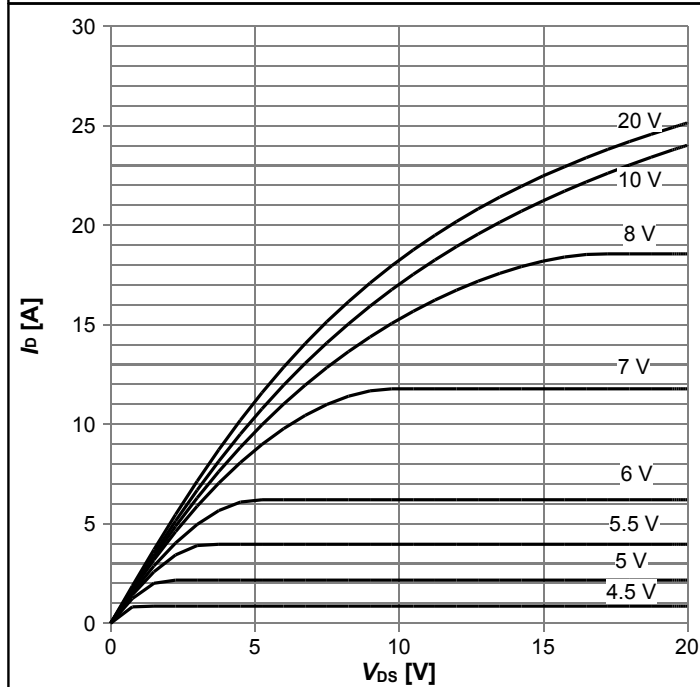
²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

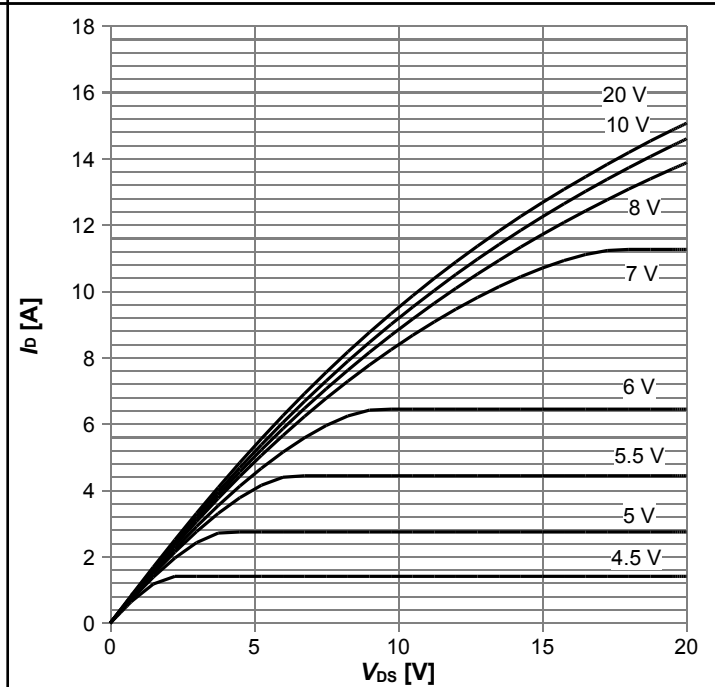
Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.85	-	V	$V_{GS}=0V$, $I_F=2.9A$, $T_i=25^{\circ}C$
Reverse recovery time	t_{rr}	-	180	-	ns	$V_R=400V$, $I_F=2.9A$, $di_F/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	-	1.2	-	μC	$V_R=400V$, $I_F=2.9A$, $di_F/dt=100A/\mu s$
Peak reverse recovery current	I_{rrm}	-	12	-	A	$V_R=400V$, $I_F=2.9A$, $di_F/dt=100A/\mu s$

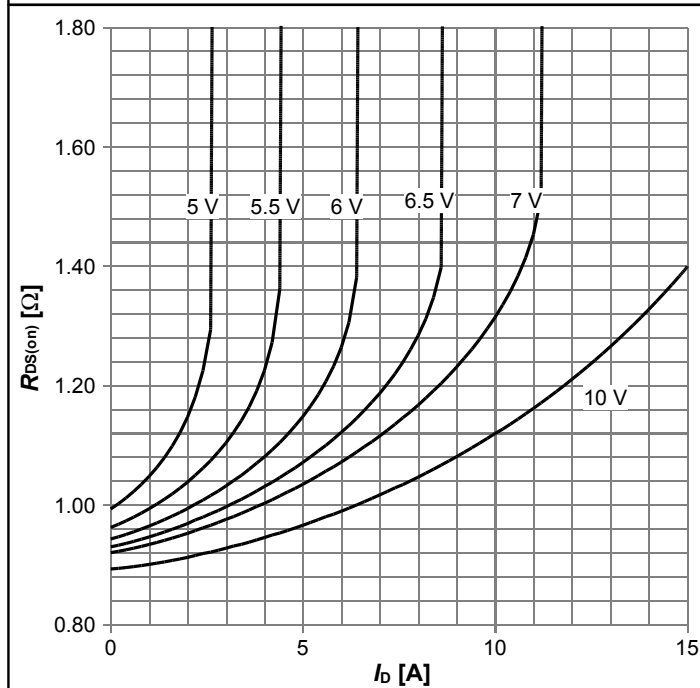
5 Electrical characteristics diagrams



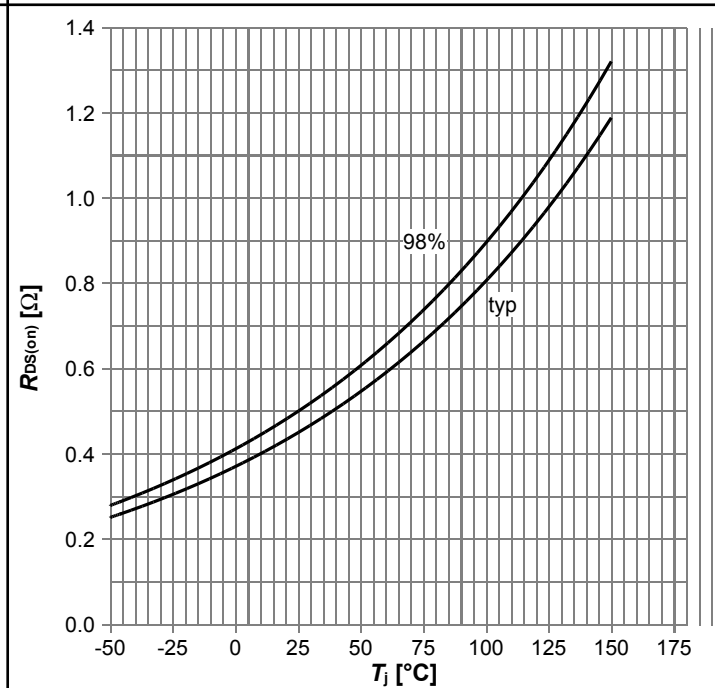
Typ. output characteristics $T_j=25^\circ\text{C}$

 $I_D=f(V_{DS})$; $T_j=25^\circ\text{C}$; parameter: V_{GS}

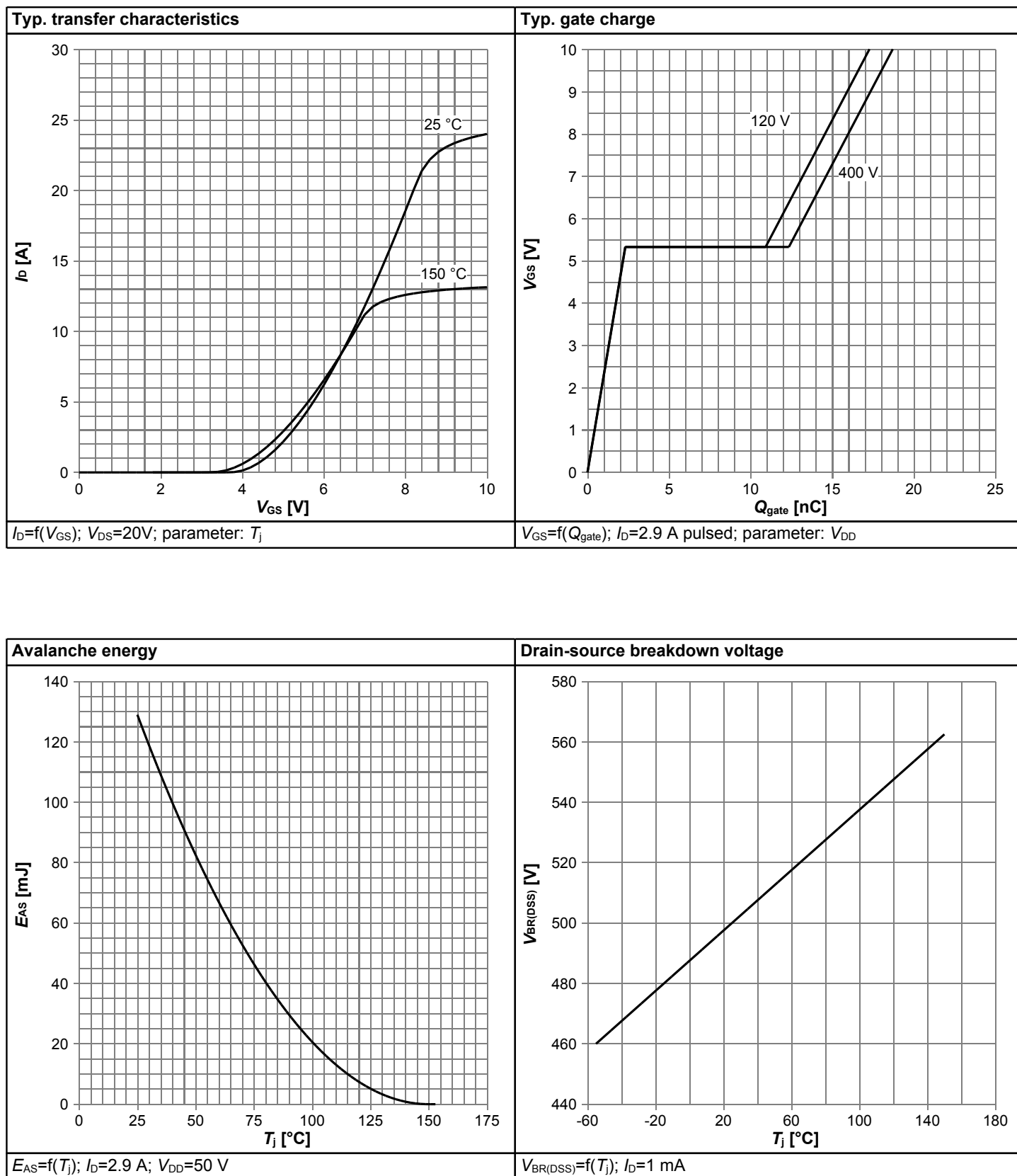
Typ. output characteristics $T_j=125^\circ\text{C}$

 $I_D=f(V_{DS})$; $T_j=125^\circ\text{C}$; parameter: V_{GS}

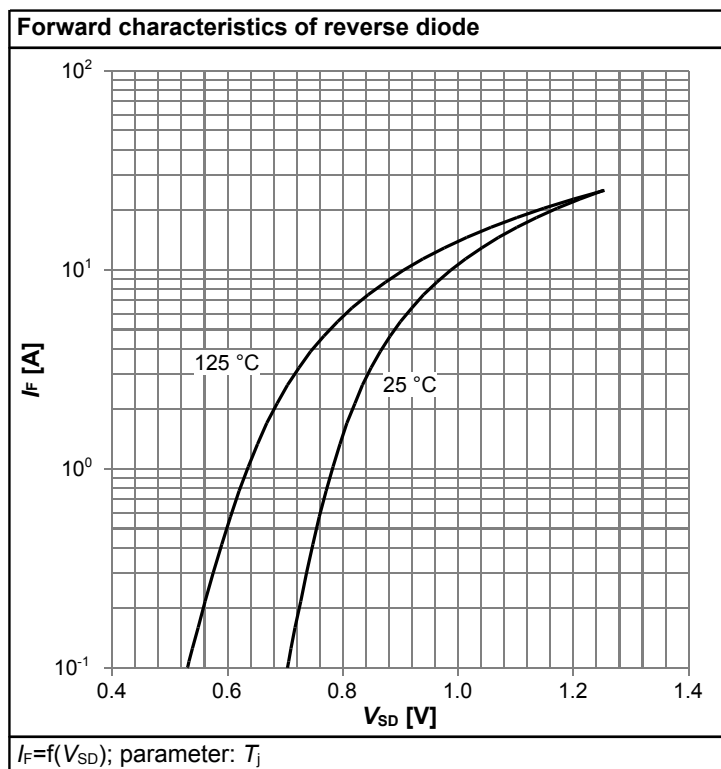
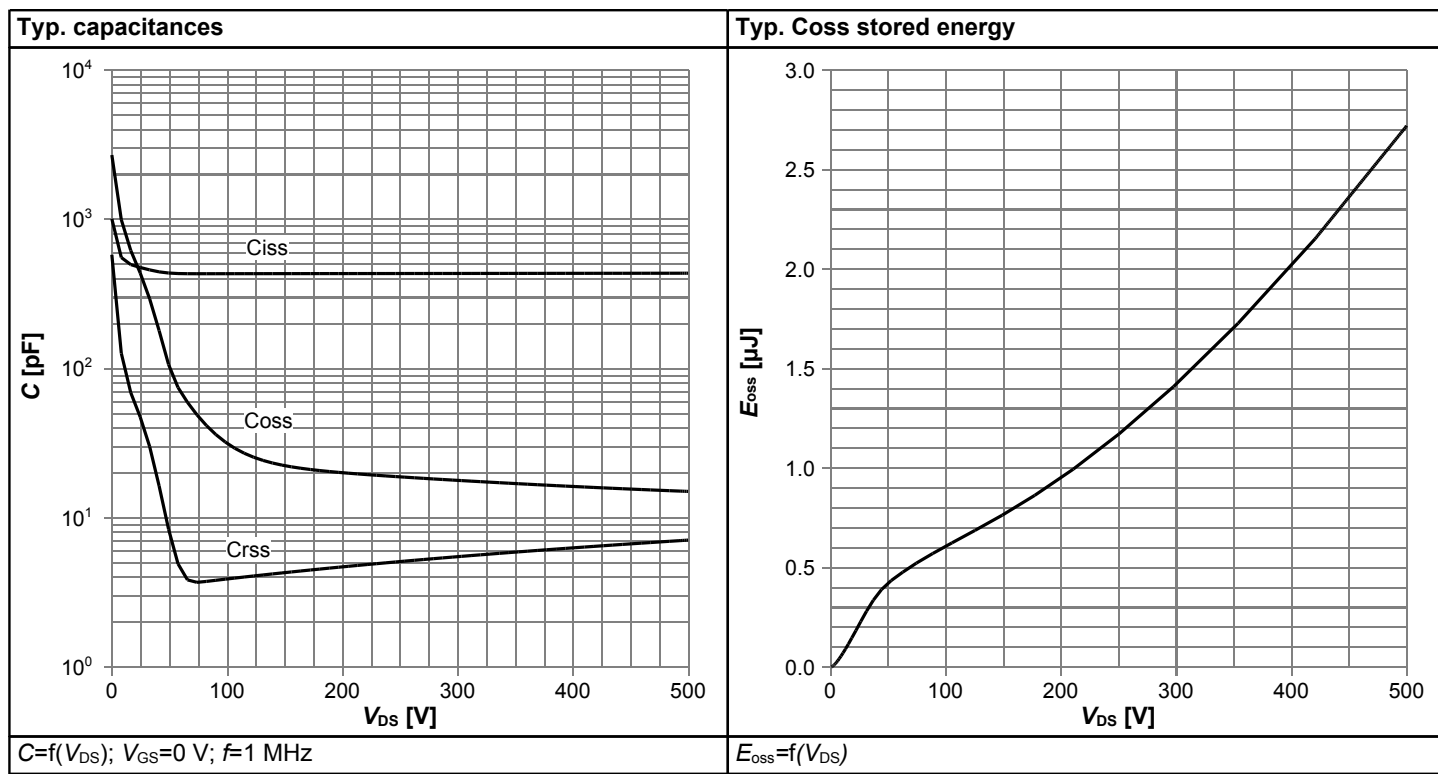
Typ. drain-source on-state resistance


 $R_{DS(on)}=f(I_D)$; $T_j=125^\circ\text{C}$; parameter: V_{GS}

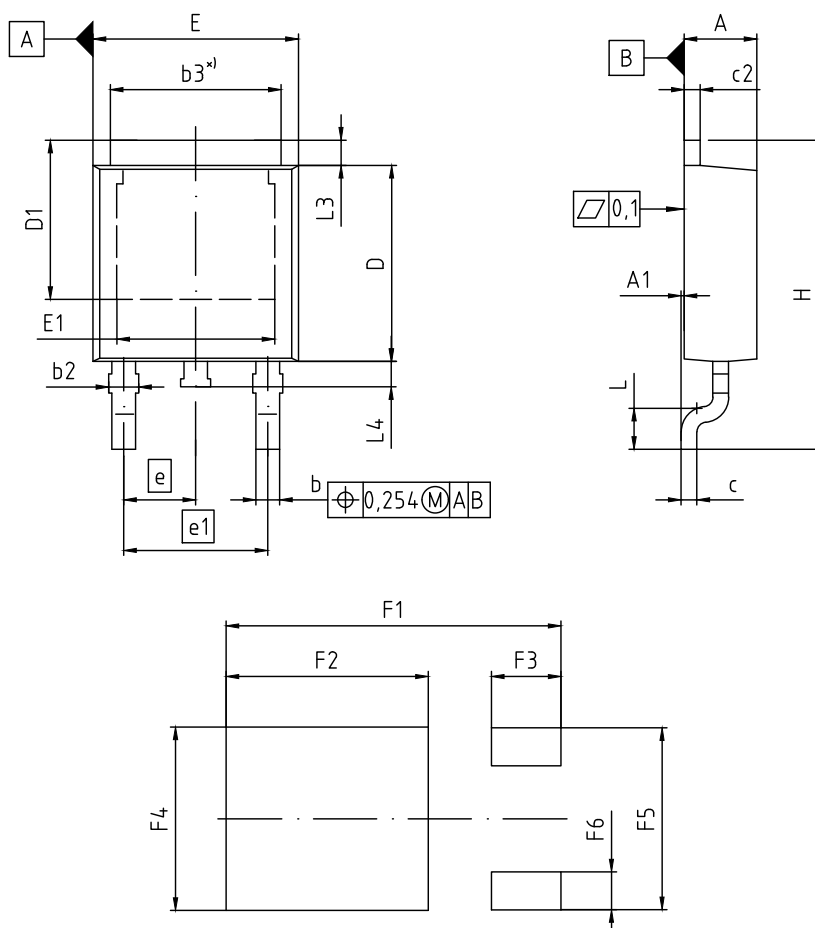
Drain-source on-state resistance


 $R_{DS(on)}=f(T_j)$; $I_D=2.3\text{ A}$; $V_{GS}=13\text{ V}$





7 Package Outlines



*) mold flash not included

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.60	0.185	0.220
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57 (BSC)		0.180 (BSC)	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.60		0.417	
F2	6.40		0.252	
F3	2.20		0.087	
F4	5.80		0.228	
F5	5.76		0.227	
F6	1.20		0.047	

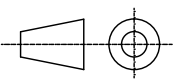
DOCUMENT NO. Z8B00003328
SCALE 0 2.0 4mm
EUROPEAN PROJECTION 
ISSUE DATE 01-09-2015
REVISION 05

Figure 1 Outline PG-TO 252, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS Webpage: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPD50R500CE

Revision: 2015-11-17, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2012-06-29	Release of final version
2.1	2013-07-16	update to Halogen free mold compound
2.2	2015-11-17	Updated to qualified for standard grade & updated package drawing

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

erratum@infineon.com

Published by

Infineon Technologies AG
81726 München, Germany
© 2015 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.