



IPG20N04S4-12A

OptiMOS™-T2 Power-Transistor



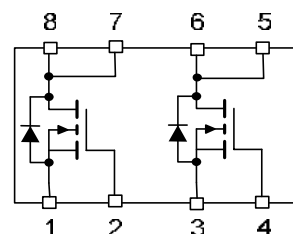
Product Summary

V_{DS}	40	V
$R_{DS(on),max}^{4)}$	12.2	mΩ
I_D	20	A

Features

- Dual N-channel Normal Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

PG-TDSON-8



Type	Package	Marking
IPG20N04S4-12A	PG-TDSON-8	4N0412

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	20	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	20	
Pulsed drain current ²⁾ one channel active	$I_{D,pulse}$	-	80	
Avalanche energy, single pulse ^{2, 4)}	E_{AS}	$I_D=10\text{ A}$	80	mJ
Avalanche current, single pulse ⁴⁾	I_{AS}	-	15	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation one channel active	P_{tot}	$T_C=25\text{ °C}$	41	W
Operating and storage temperature	T_J , T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	3.7	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm ² cooling area ³⁾	-	60	-	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=15\mu\text{A}$	2.0	3.0	4.0	
Zero gate voltage drain current ⁴⁾	I_{DSS}	$V_{DS}=40\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=18\text{ V}, V_{GS}=0\text{ V}, T_j=85\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current ⁴⁾	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance ⁴⁾	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=17\text{ A}$	-	11.1	12.2	m Ω



Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance ⁴⁾	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	1130	1470	pF
Output capacitance ⁴⁾	C_{oss}		-	300	390	
Reverse transfer capacitance ⁴⁾	C_{rss}		-	9	21	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=11\ \Omega$	-	9	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	10	-	
Fall time	t_f		-	8	-	

Gate Charge Characteristics^{2, 4)}

Gate to source charge	Q_{gs}	$V_{DD}=32\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	6	8	nC
Gate to drain charge	Q_{gd}		-	2	4.6	
Gate charge total	Q_g		-	14	18	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

Reverse Diode

Diode continuous forward current ²⁾ one channel active	I_S	$T_C=25\text{ °C}$	-	-	20	A
Diode pulse current ²⁾ one channel active	$I_{S,pulse}$		-	-	80	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=17\text{ A},$ $T_J=25\text{ °C}$	-	0.9	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=20\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	32	-	ns
Reverse recovery charge ^{2, 4)}	Q_{rr}		-	25	-	nC

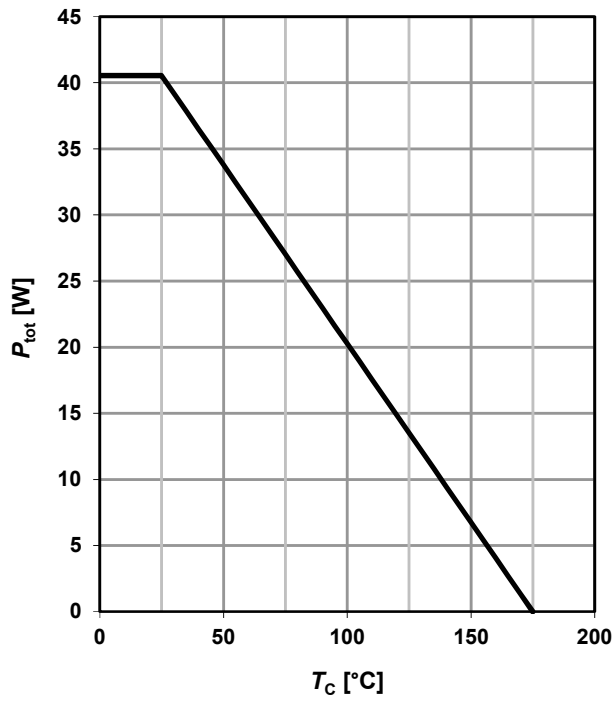
¹⁾ Current is limited by bondwire; with an $R_{thJC}=3.7\text{ K/W}$ the chip is able to carry 44A at 25°C.

²⁾ Specified by design. Not subject to production test.

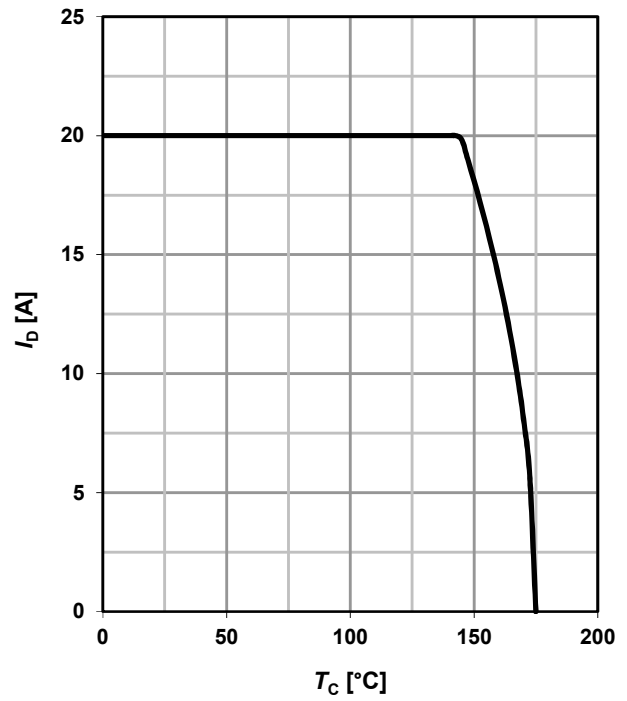
³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁴⁾ Per channel

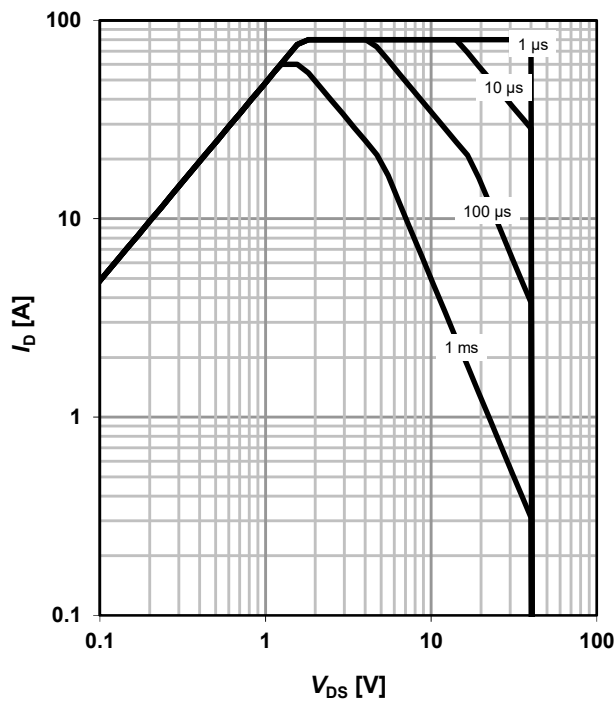
1 Power dissipation

 $P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}; \text{ one channel active}$


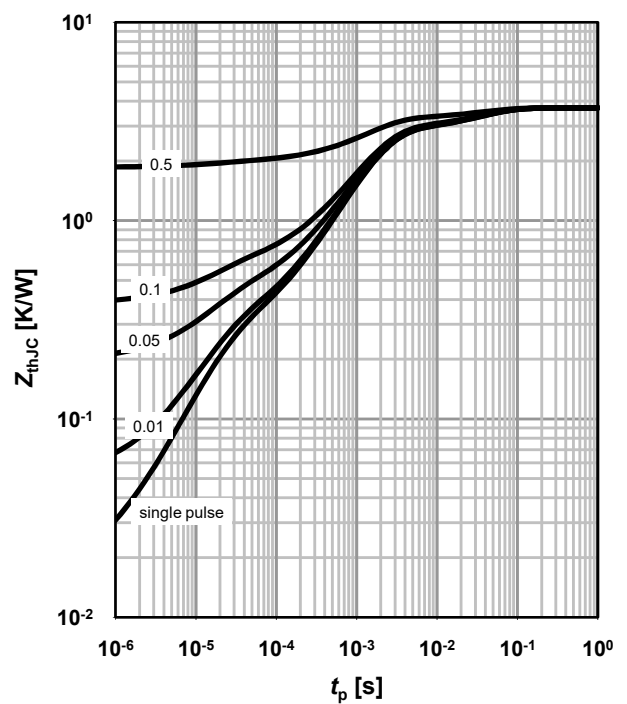
2 Drain current

 $I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}; \text{ one channel active}$


3 Safe operating area

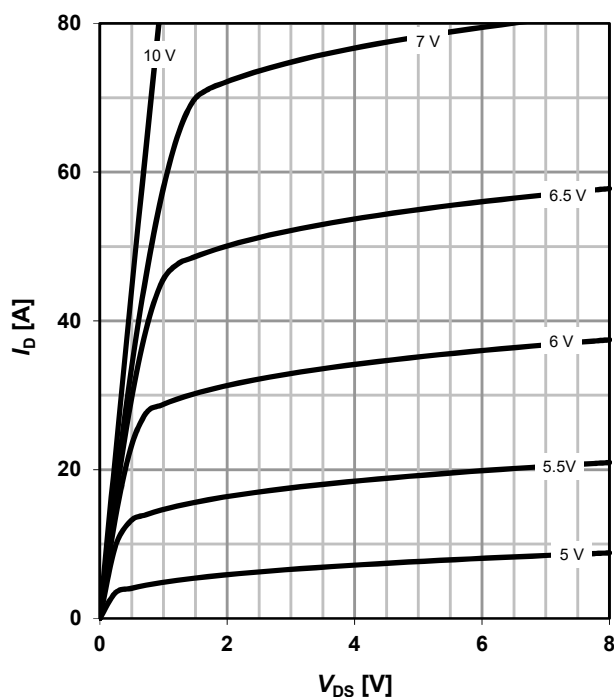
 $I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0; \text{ one channel active}$
 parameter: t_p


4 Max. transient thermal impedance

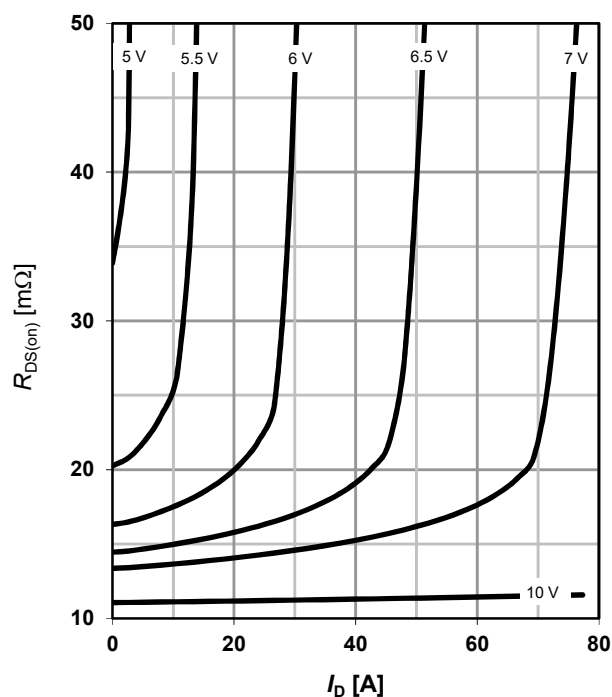
 $Z_{\text{thJC}} = f(t_p)$
 parameter: $D = t_p/T$


5 Typ. output characteristics⁴⁾

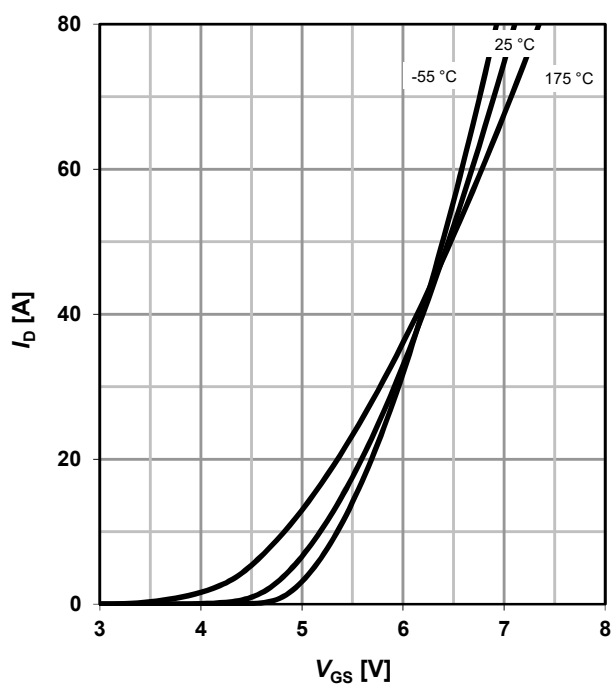
$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

parameter: V_{GS} **6 Typ. drain-source on-state resistance⁴⁾**

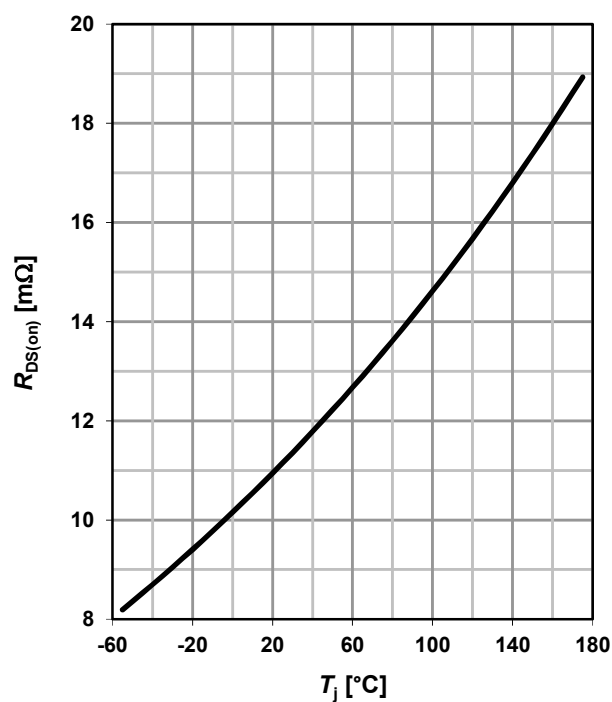
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

parameter: V_{GS} **7 Typ. transfer characteristics⁴⁾**

$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

parameter: T_j **8 Typ. drain-source on-state resistance⁴⁾**

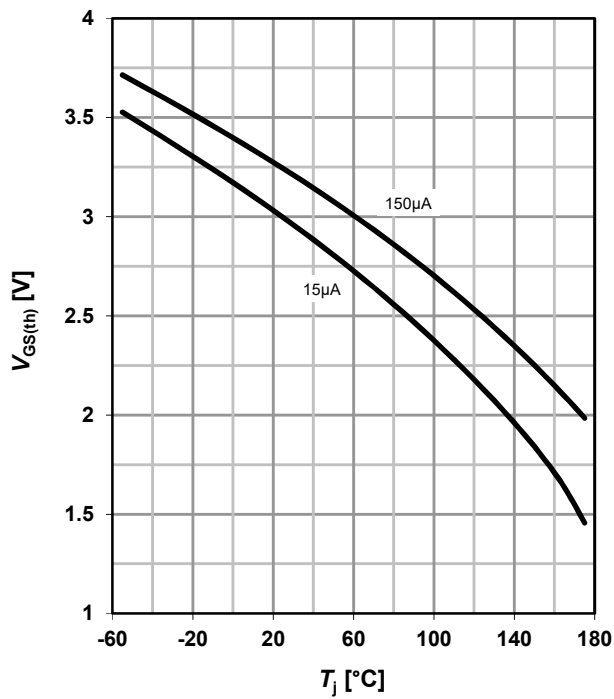
$$R_{DS(on)} = f(T_j); I_D = 17\text{ A}; V_{GS} = 10\text{ V}$$



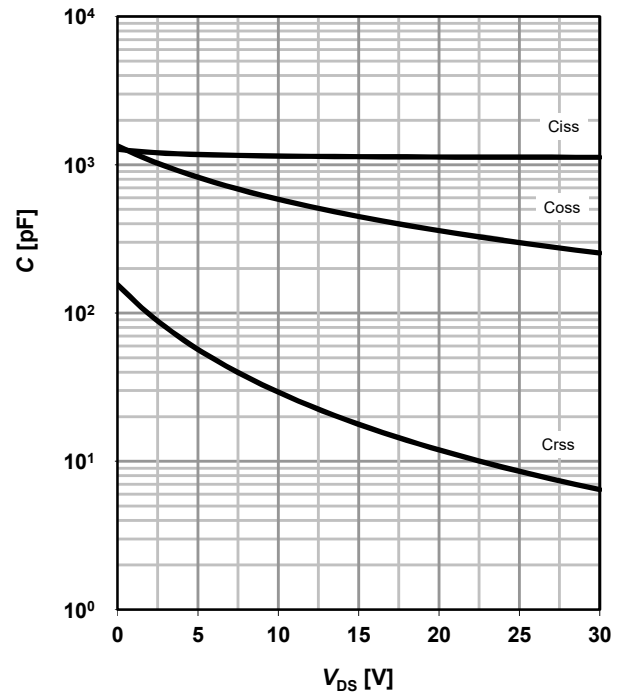
9 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D

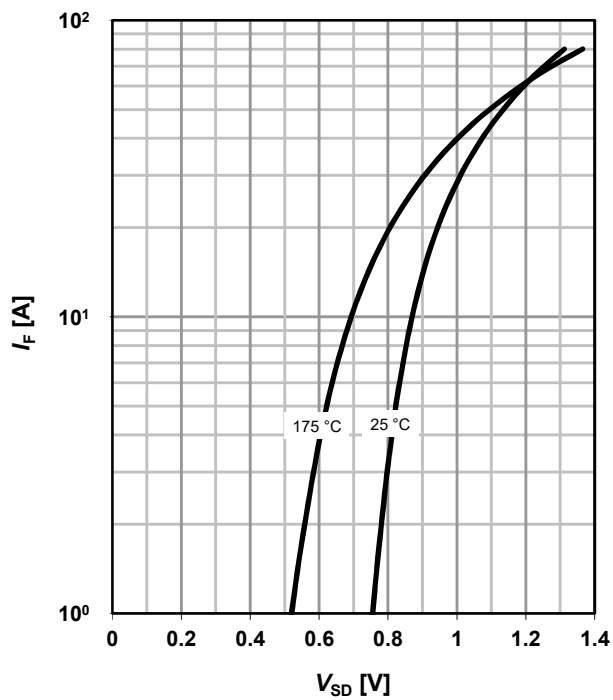

10 Typ. Capacitances⁴⁾

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$


11 Typical forward diode characteristics⁴⁾

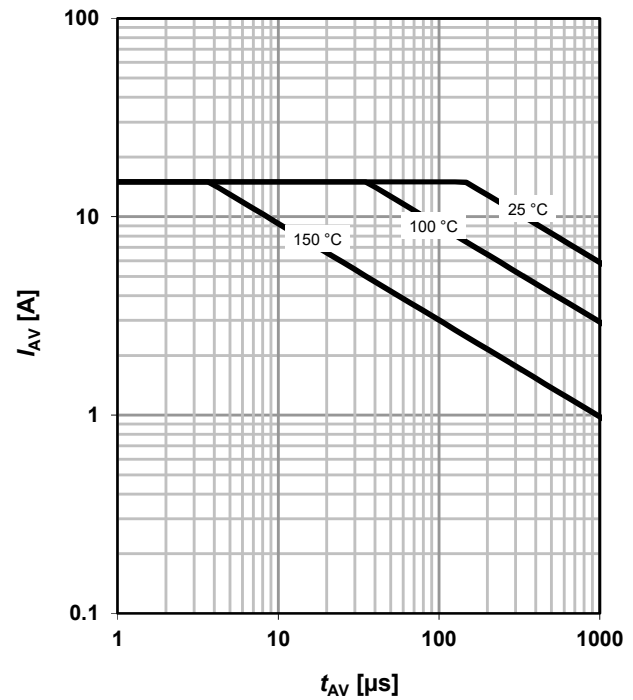
$$I_F = f(V_{SD})$$

parameter: T_j


12 Avalanche characteristics⁴⁾

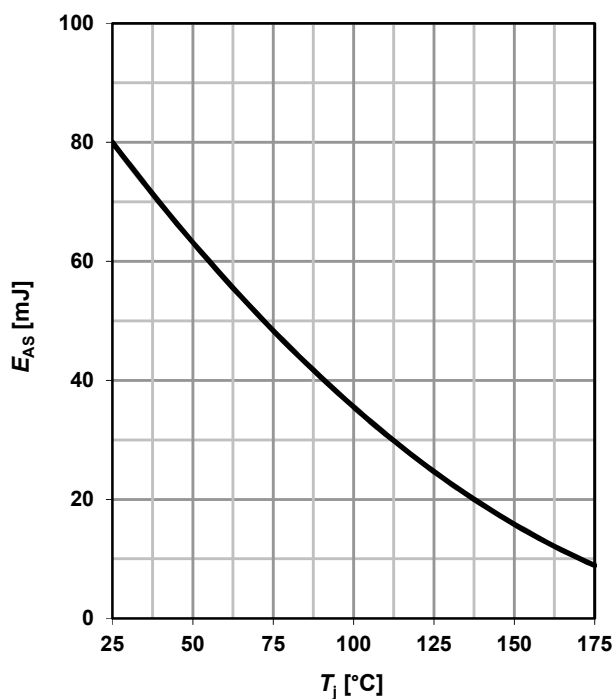
$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$

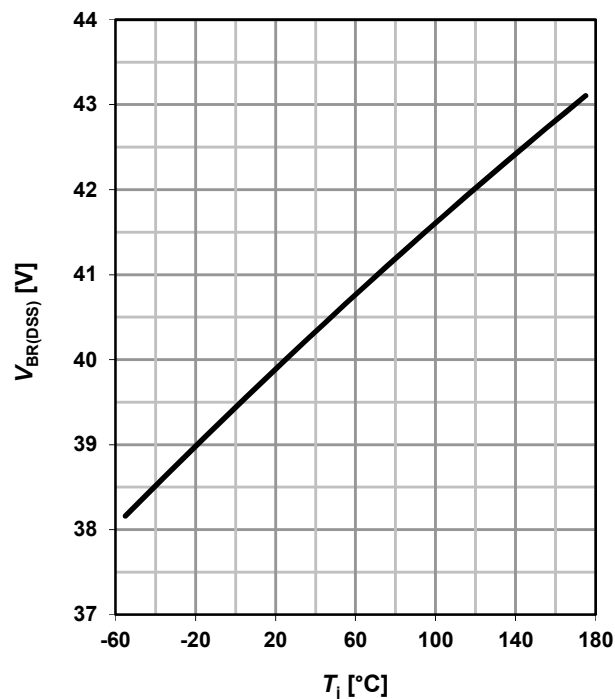


13 Avalanche energy⁴⁾

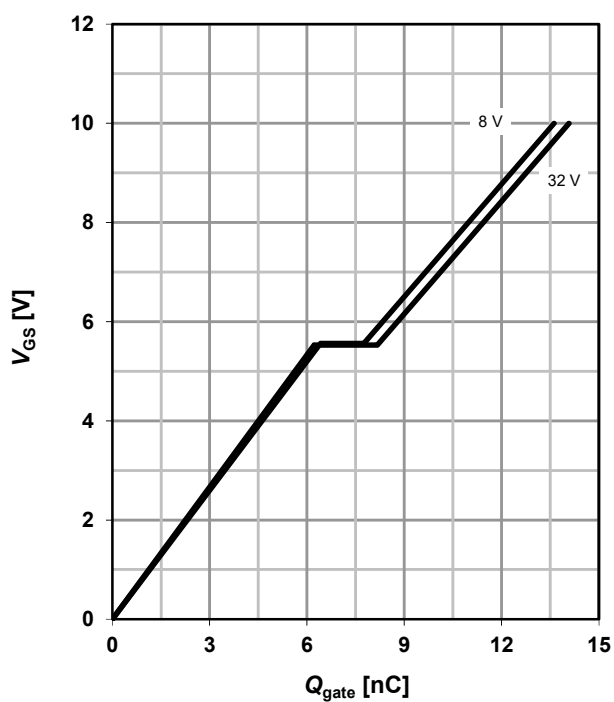
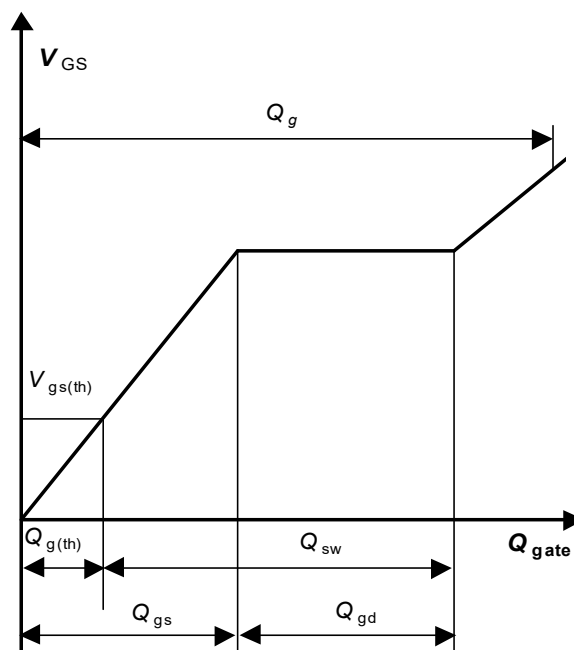
$$E_{AS} = f(T_j); I_D = 10A$$

**14 Drain-source breakdown voltage**

$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

**15 Typ. gate charge⁴⁾**

$$V_{GS} = f(Q_{gate}); I_D = 20 \text{ A pulsed}$$

parameter: V_{DD} **16 Gate charge waveforms**

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Revision History

Version	Date	Changes
Revision 1.0	18.09.2012	Data Sheet revision 1.0
Revision 1.1	20.01.2022	diagrams 7 and 15 modified
Revision 1.11	24.05.2024	Package naming updated