

MOSFET

OptiMOS™ 6 Power-Transistor, 200 V

Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020
- 100% avalanche tested

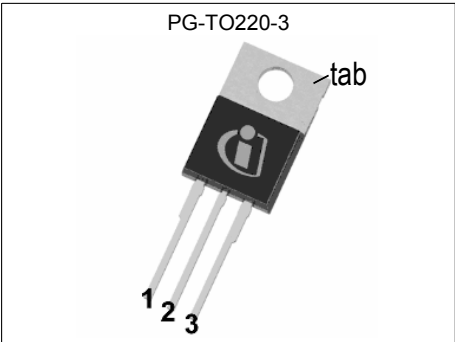
Product validation

Fully qualified according to JEDEC for Industrial Applications

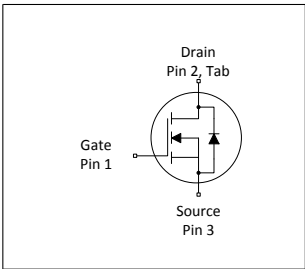
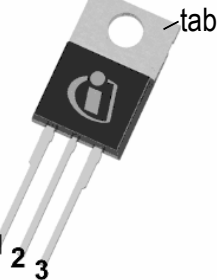
Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	200	V
$R_{DS(on),max}$	6.9	mΩ
I_D	136	A
Q_{oss}	232	nC
Q_G	73	nC
Q_{rr} (1000A/μs)	391	nC

Type / Ordering Code	Package	Marking	Related Links
IPP069N20NM6	PG-TO220-3	069N20N6	-



PG-TO220-3



RoHS

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	136 96 101 15.3	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=15\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	544	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	516	mJ	$I_D=77\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	300 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^{2)}$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.31	0.5	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.0	3.7	4.5	V	$V_{DS}=V_{GS}$, $I_D=258\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=160\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=160\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.9 5.2	6.9 6.3	m Ω	$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ $V_{GS}=15\text{ V}$, $I_D=100\text{ A}$
Gate resistance	R_G	-	3.8	-	Ω	-
Transconductance ¹⁾	g_{fs}	33	65	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=100\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	5700	7400	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	910	1200	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	30	52	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	56	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	37	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	29	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	38	-	nC	$V_{DD}=100\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	21	-	nC	$V_{DD}=100\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	14	21	nC	$V_{DD}=100\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	31	-	nC	$V_{DD}=100\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	73	110	nC	$V_{DD}=100\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	6.6	-	V	$V_{DD}=100\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	63	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	232	302	nC	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

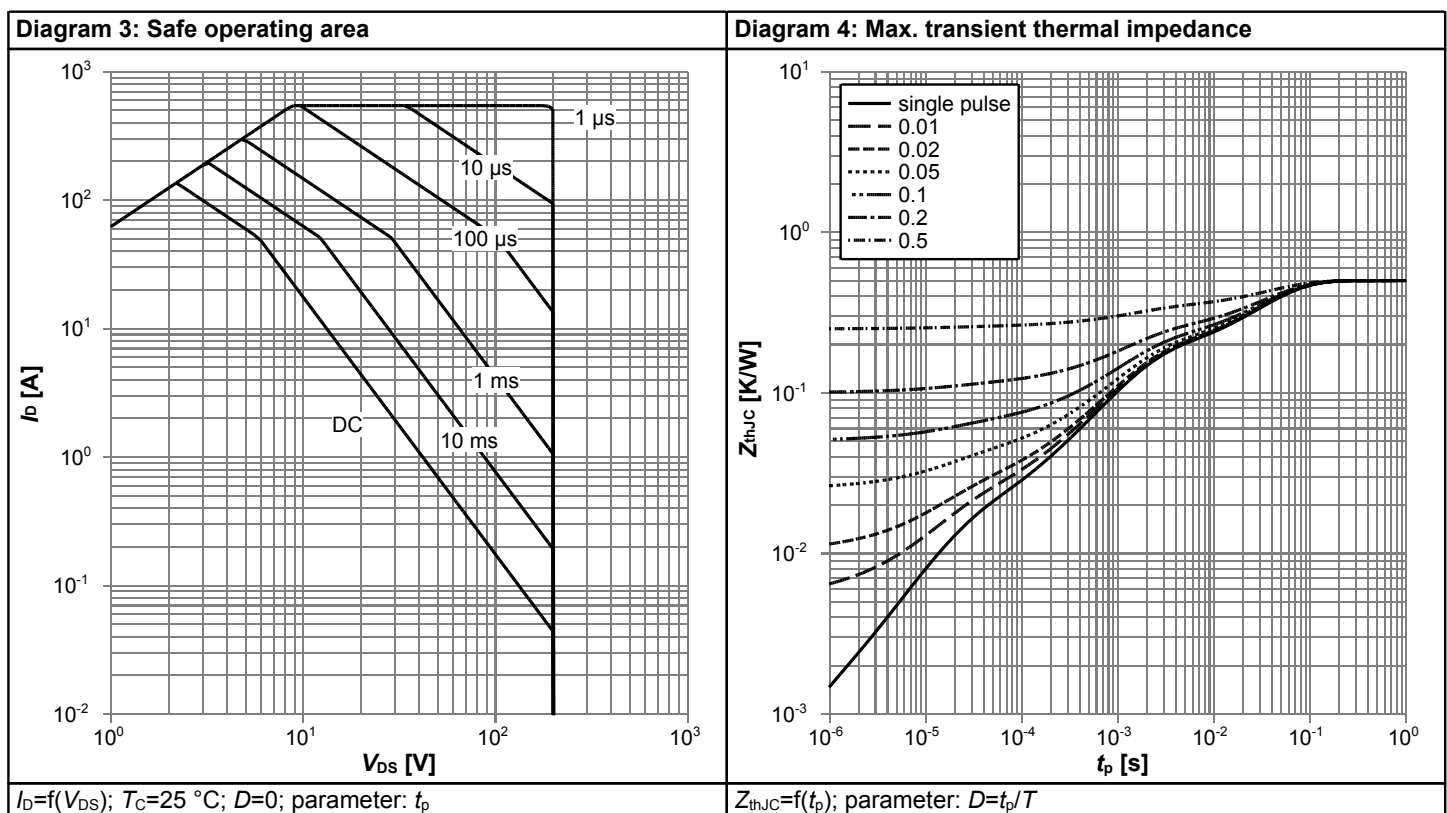
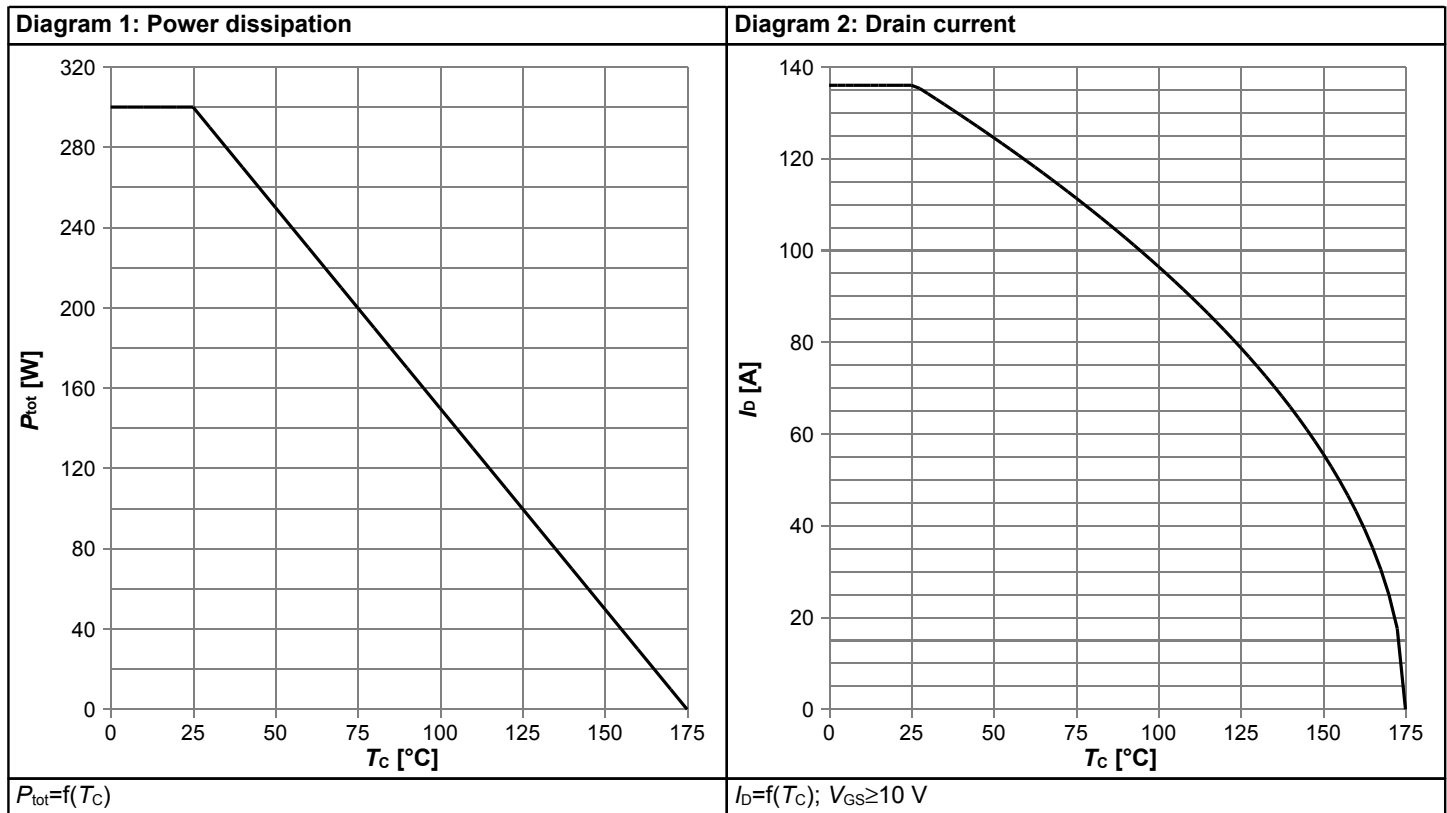
²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	136	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	544	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.92	1.0	V	$V_{GS}=0\text{ V}$, $I_F=100\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	53	-	ns	$V_R=100\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	70	140	nC	$V_R=100\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery time ¹⁾	t_{rr}	-	38	-	ns	$V_R=100\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	391	782	nC	$V_R=100\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

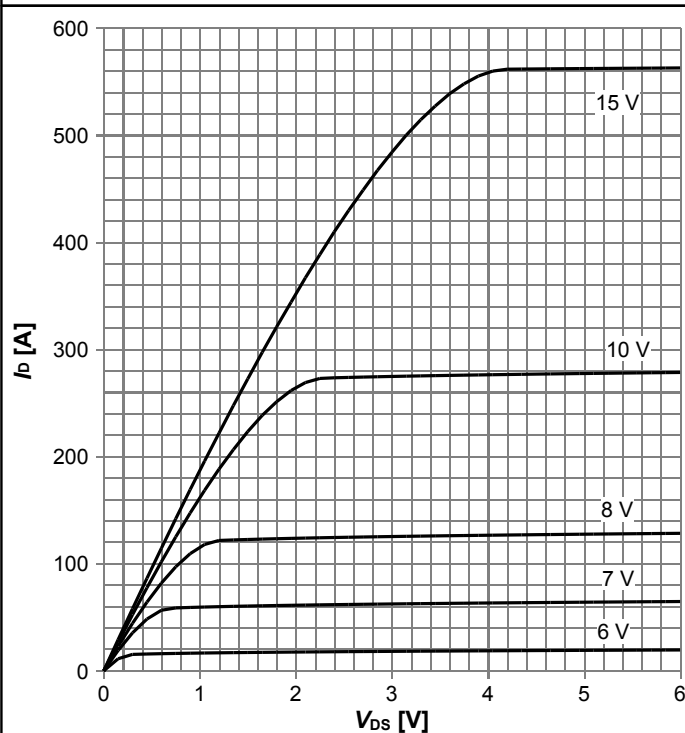
4 Electrical characteristics diagrams



OptiMOS™ 6 Power-Transistor, 200 V

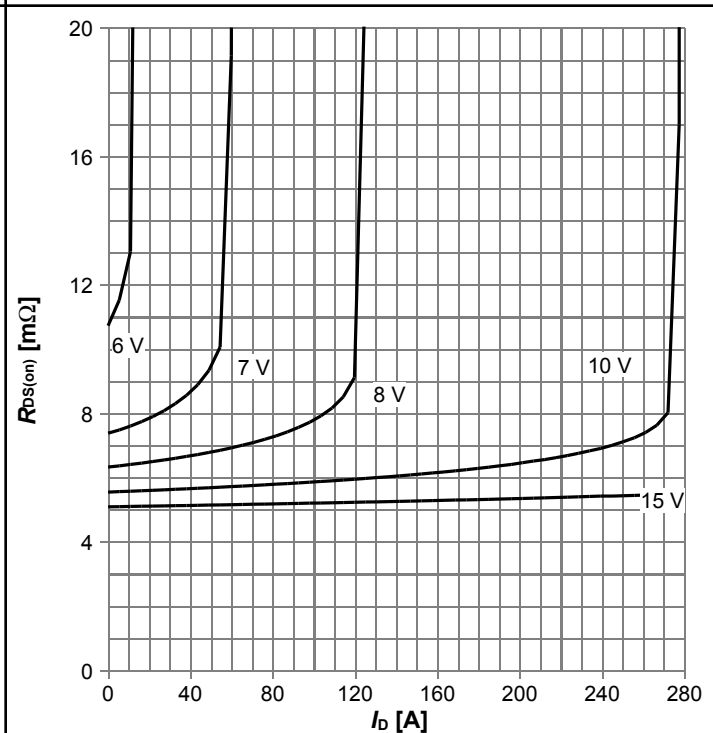
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Diagram 5: Typ. output characteristics



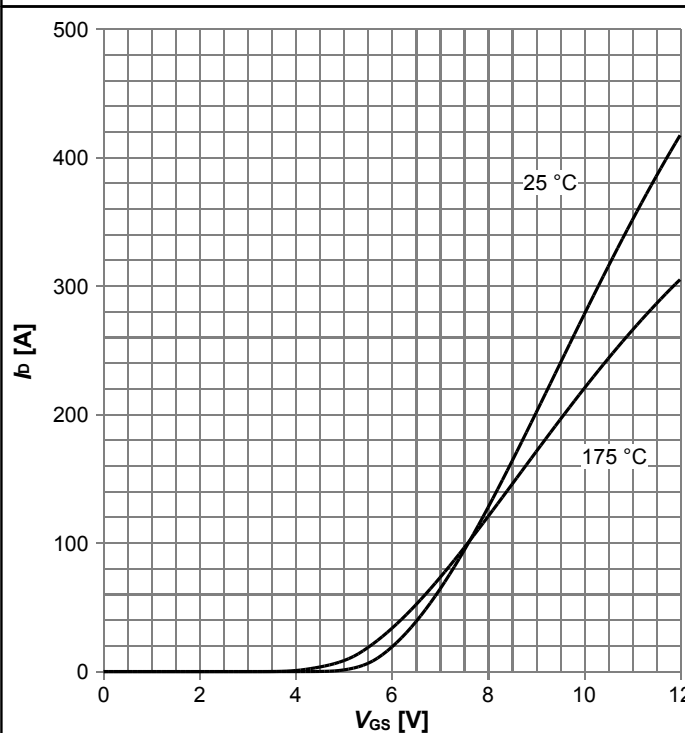
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



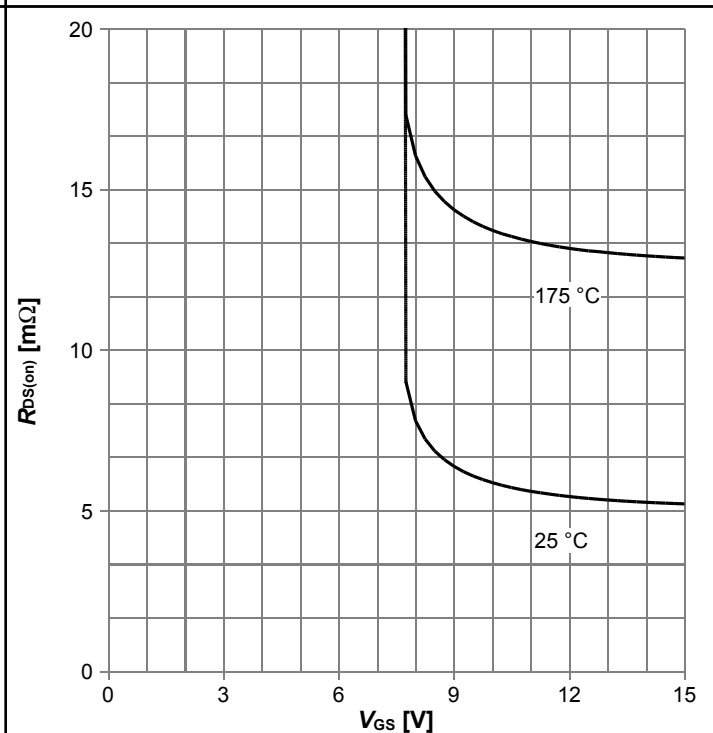
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



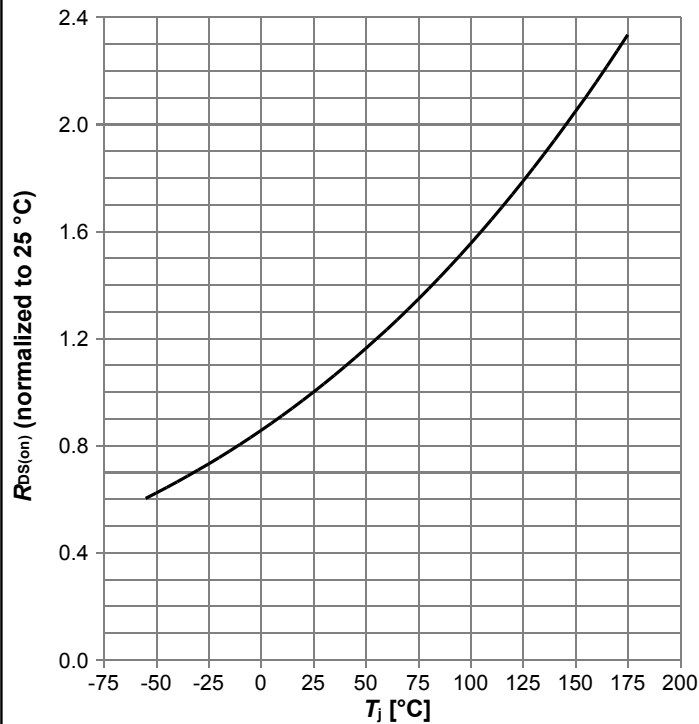
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



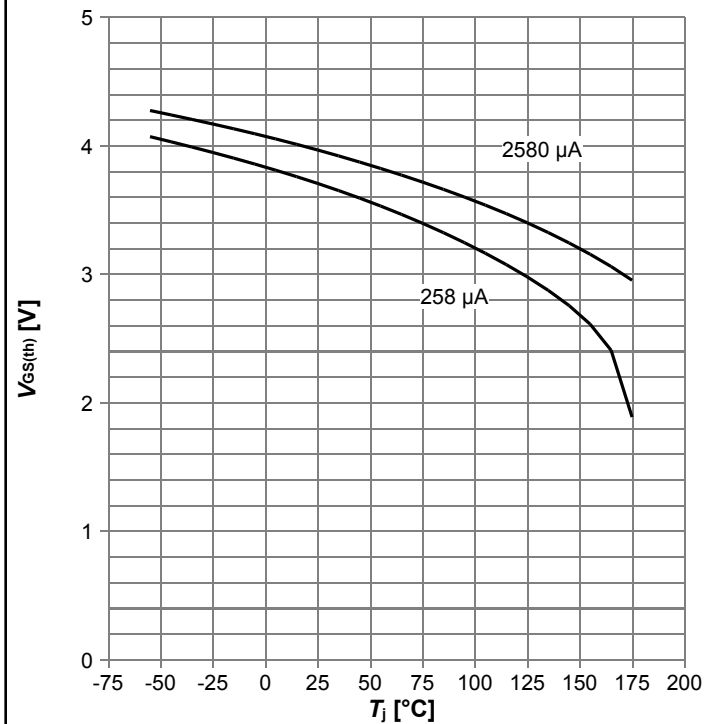
$R_{DS(on)} = f(V_{GS})$, $I_D = 100\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



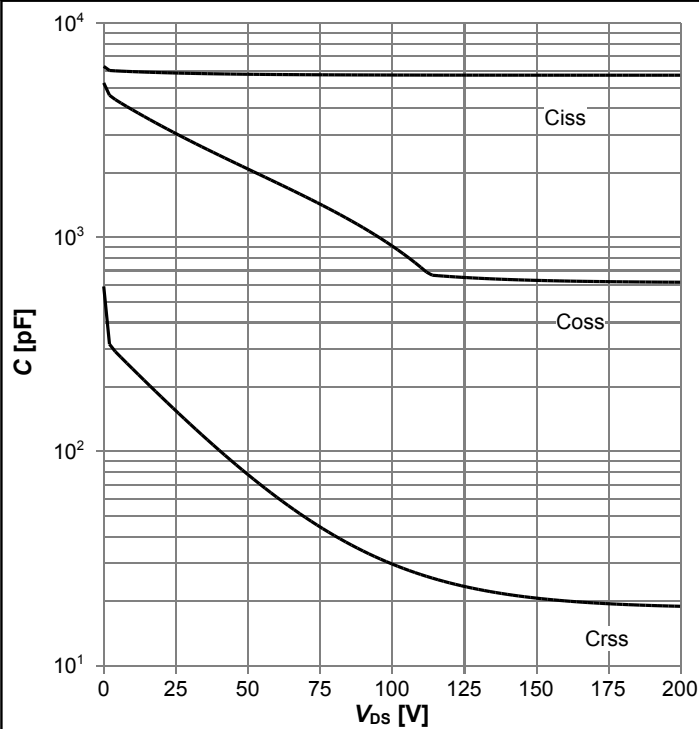
$R_{DS(on)} = f(T_j)$, $I_D = 100$ A, $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



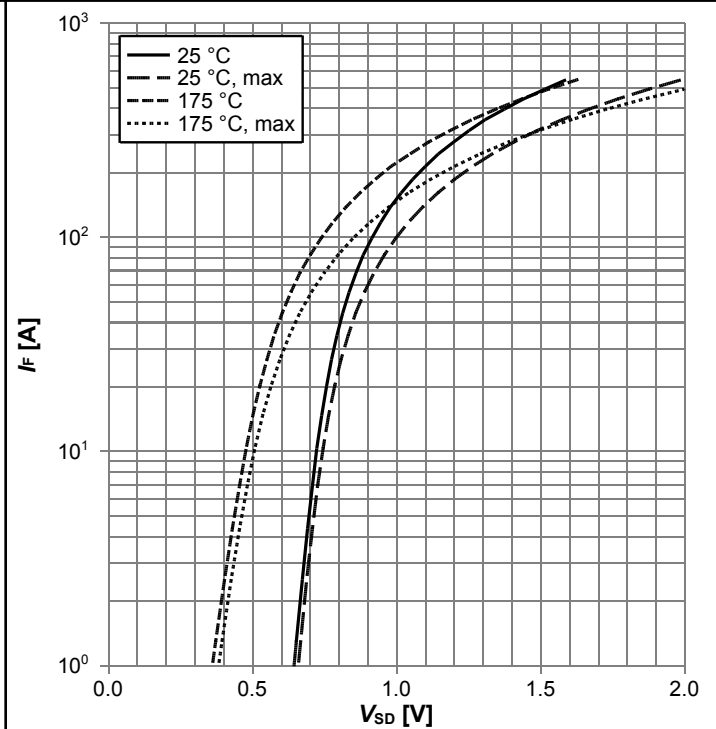
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode

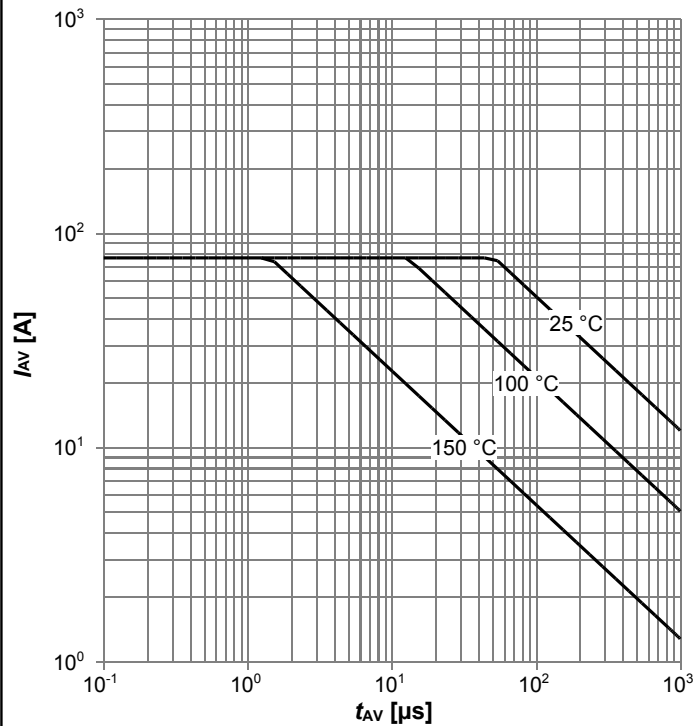


$I_F = f(V_{SD})$; parameter: T_j

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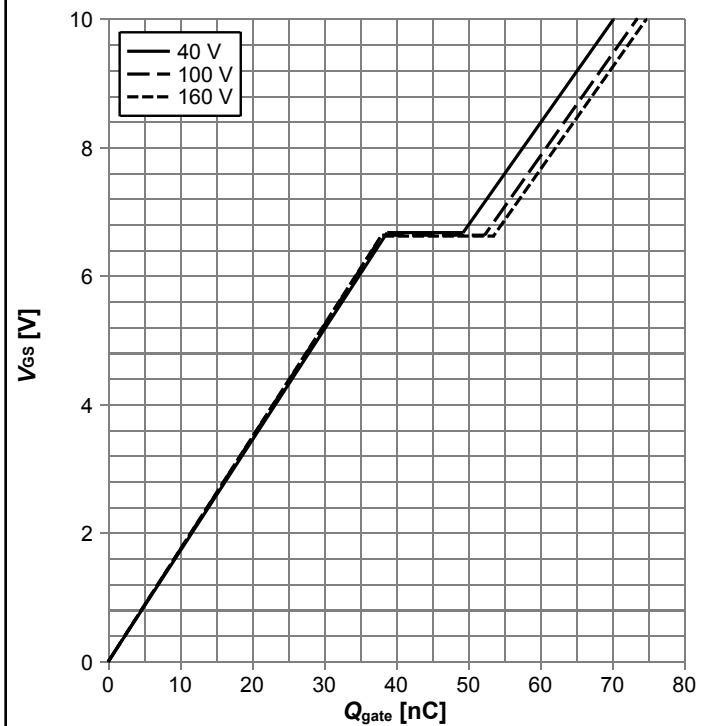
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Diagram 13: Avalanche characteristics



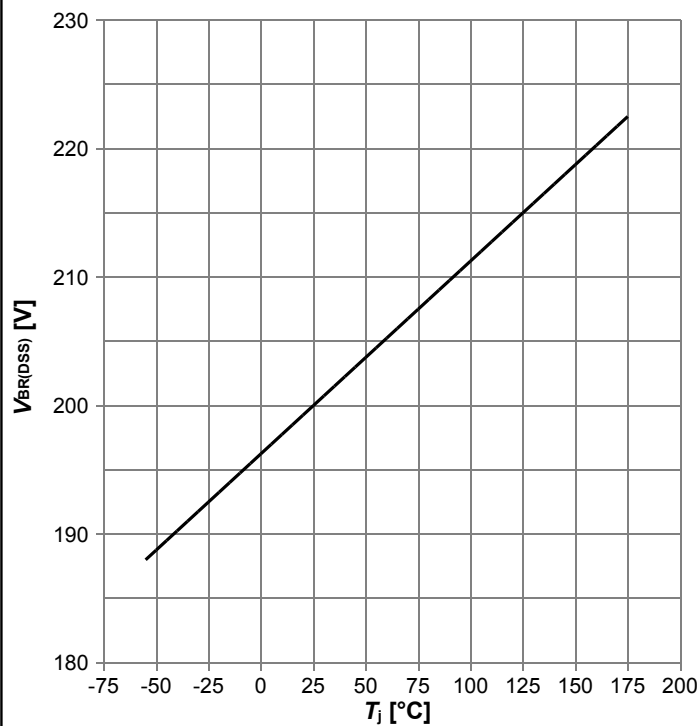
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



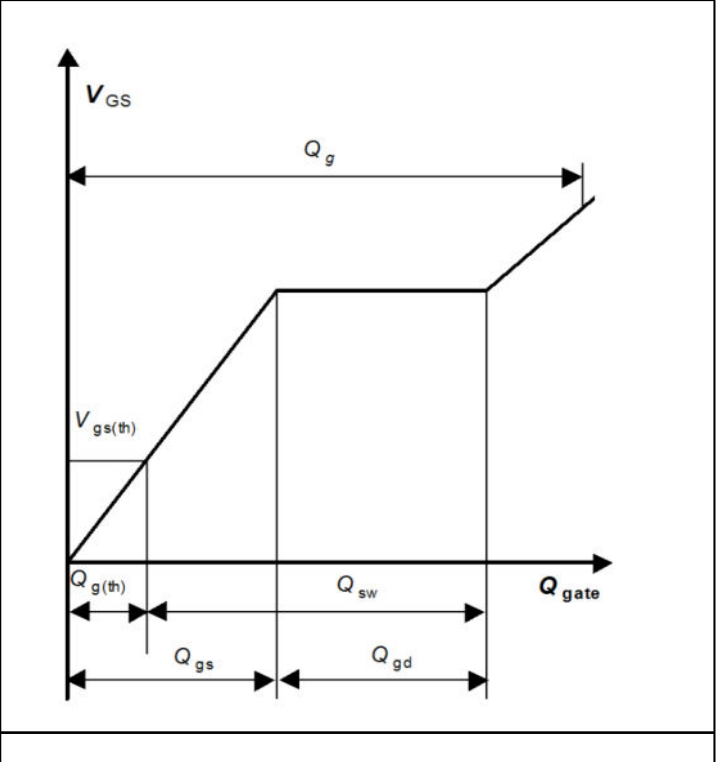
$V_{GS}=f(Q_{gate})$, $I_D=50\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

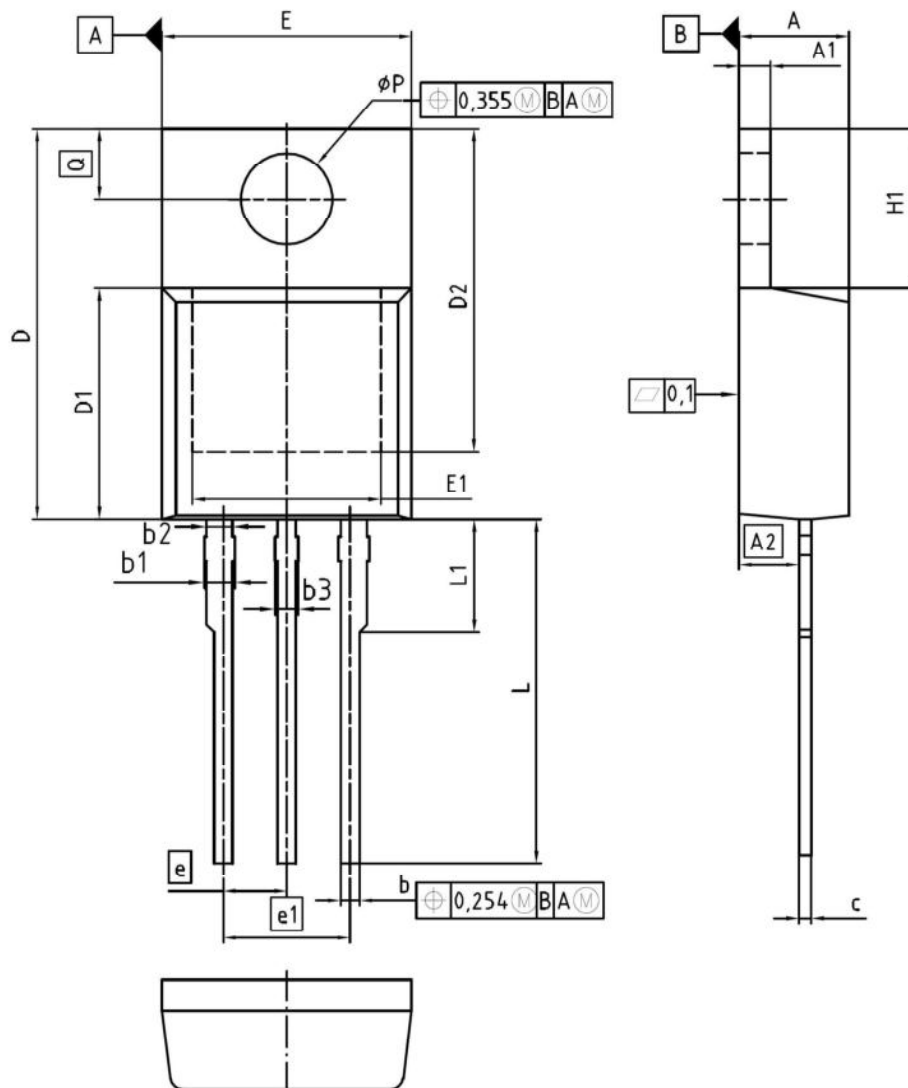


$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
ϕP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

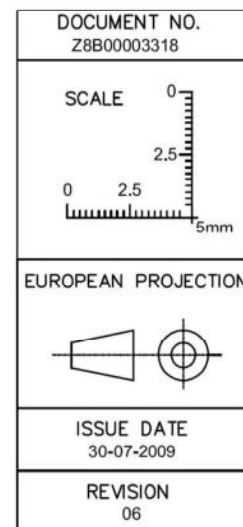


Figure 1 Outline PG-TO220-3, dimensions in mm/inches

Revision History

IPP069N20NM6

Revision: 2023-12-07, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2023-12-07	Release of final version

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Published by

Infineon Technologies AG

81726 München, Germany

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