



IPB70N12S3-11

IPI70N12S3-11, IPP70N12S3-11

OptiMOS™-T Power-Transistor



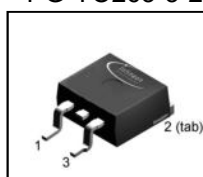
Product Summary

V_{DS}	120	V
$R_{DS(on),max}$ (SMD version)	11.3	mΩ
I_D	70	A

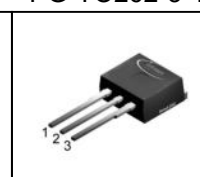
Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

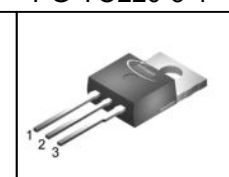
PG-TO263-3-2



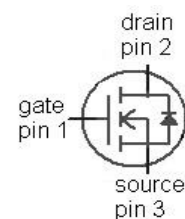
PG-TO262-3-1



PG-TO220-3-1



Type	Package	Marking
IPB70N12S3-11	PG-TO263-3-2	3N1211
IPI70N12S3-11	PG-TO262-3-1	3N1211
IPP70N12S3-11	PG-TO220-3-1	3N1211



Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	70	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	48	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	280	
Avalanche energy, single pulse ¹⁾	E_{AS}	$I_D=35\text{ A}$	410	mJ
Avalanche current, single pulse	I_{AS}	-	70	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	125	W
Operating and storage temperature	T_J , T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics¹⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	1.2	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ²⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	120	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=83\mu\text{A}$	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=120\text{V}, V_{GS}=0\text{V}, T_j=25^\circ\text{C}$	-	0.01	0.1	μA
		$V_{DS}=120\text{V}, V_{GS}=0\text{V}, T_j=125^\circ\text{C}^{1)}$	-	1	10	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=70\text{A}$	-	9.7	11.6	m Ω
		$V_{GS}=10\text{V}, I_D=70\text{A},$ SMD version	-	9.4	11.3	



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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	3350	4355	pF
Output capacitance	C_{oss}		-	940	1222	
Reverse transfer capacitance	C_{rss}		-	105	158	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=70A, R_G=3.5\Omega$	-	17	-	ns
Rise time	t_r		-	8	-	
Turn-off delay time	$t_{d(off)}$		-	25	-	
Fall time	t_f		-	8	-	

Gate Charge Characteristics¹⁾

Gate to source charge	Q_{gs}	$V_{DD}=96V, I_D=70A,$ $V_{GS}=0 \text{ to } 10V$	-	18	23	nC
Gate to drain charge	Q_{gd}		-	16	24	
Gate charge total	Q_g		-	51	65	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

Reverse Diode

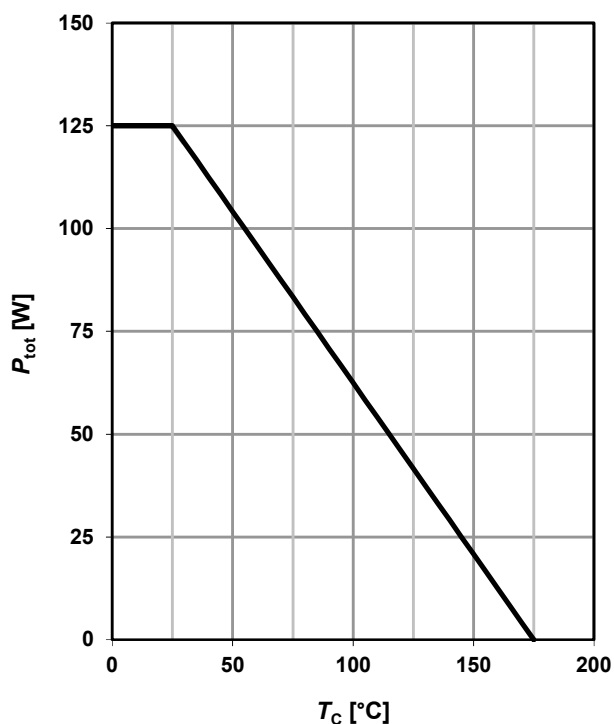
Diode continuous forward current ¹⁾	I_S	$T_C=25^\circ C$	-	-	70	A
Diode pulse current ¹⁾	$I_{S,pulse}$		-	-	280	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=70A,$ $T_j=25^\circ C$	0.6	1	1.2	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=60V, I_F=50A,$ $di_F/dt=100A/\mu s$	-	100	-	ns
Reverse recovery charge ¹⁾	Q_{rr}		-	265	-	

¹⁾ Defined by design. Not subject to production test.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

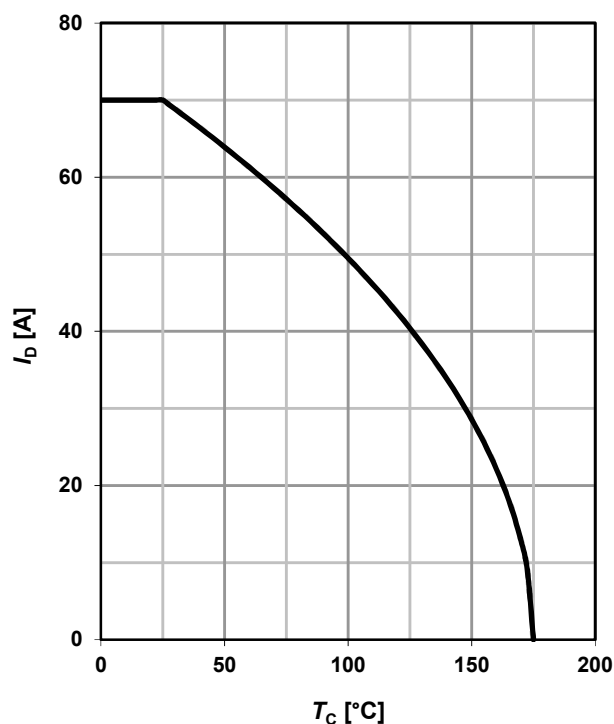
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



2 Drain current

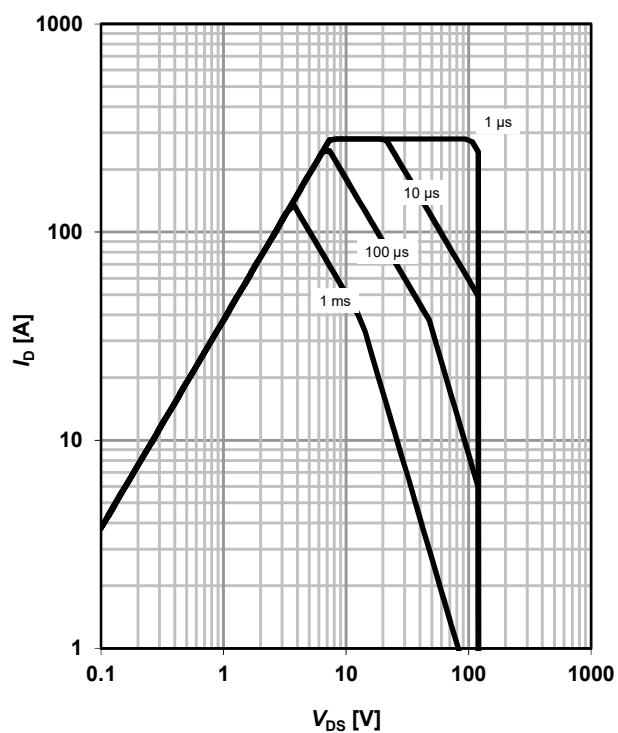
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}; \text{SMD}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0; \text{SMD}$$

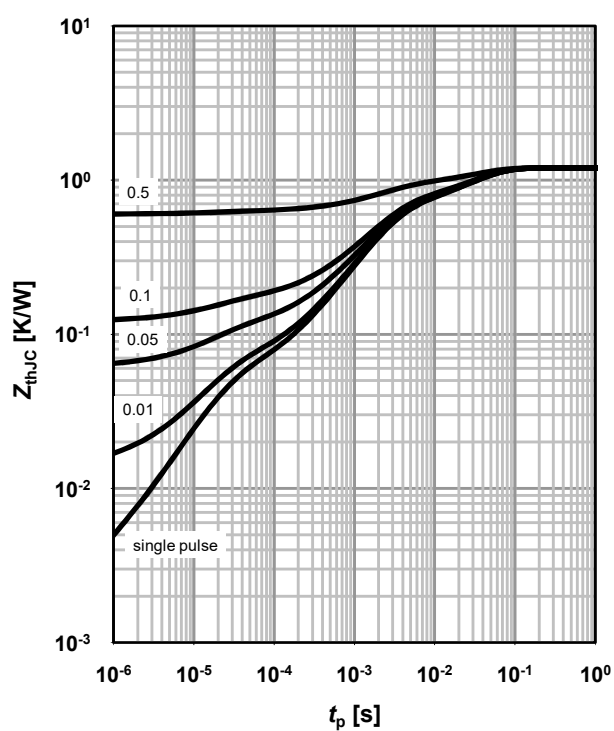
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

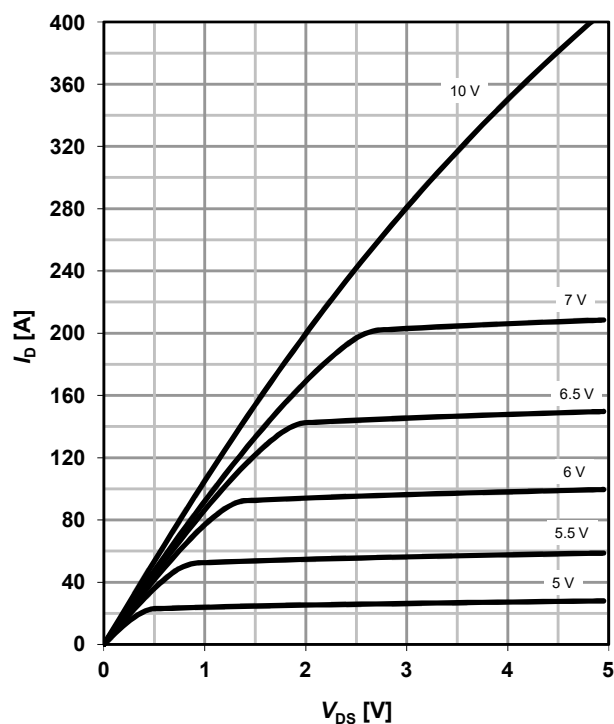
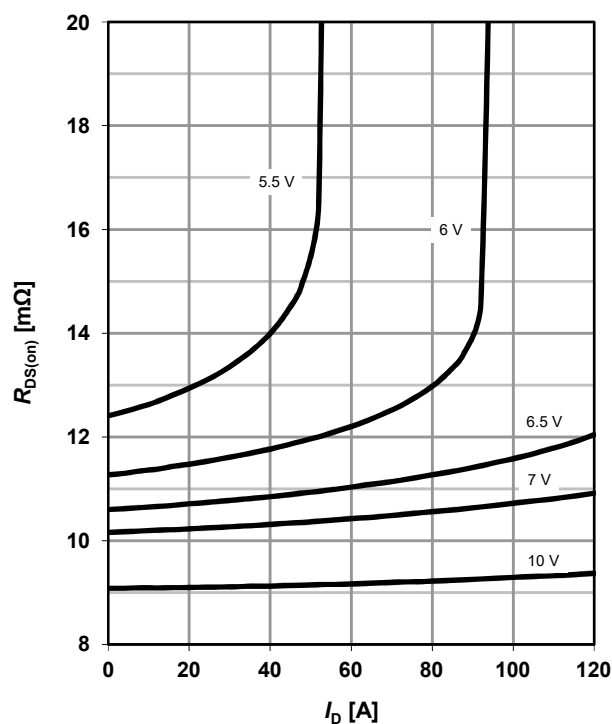
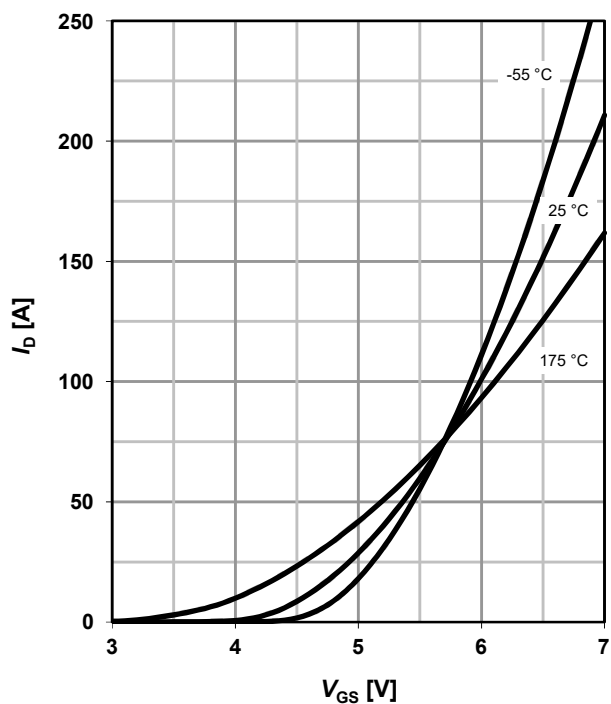
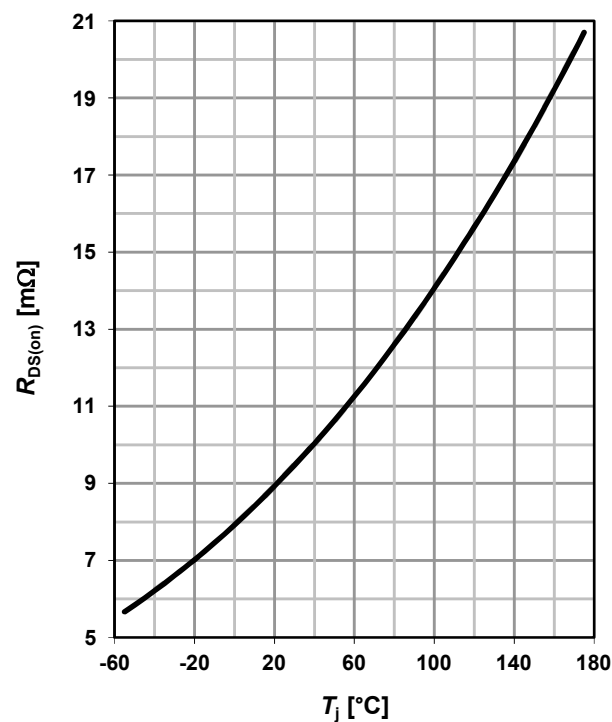
parameter: $D = t_p/T$





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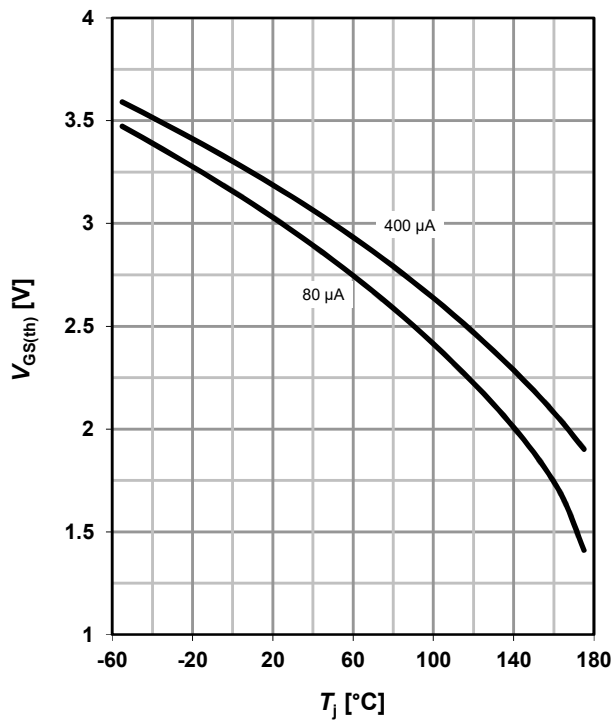
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5 Typ. output characteristics $I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{SMD}$ parameter: V_{GS} **6 Typ. drain-source on-state resistance** $R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{SMD}$ parameter: V_{GS} **7 Typ. transfer characteristics** $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$ parameter: T_j **8 Typ. drain-source on-state resistance** $R_{DS(on)} = f(T_j); I_D = 70\text{ A}; V_{GS} = 10\text{ V}; \text{SMD}$ $\alpha = 0.4$ 

9 Typ. gate threshold voltage

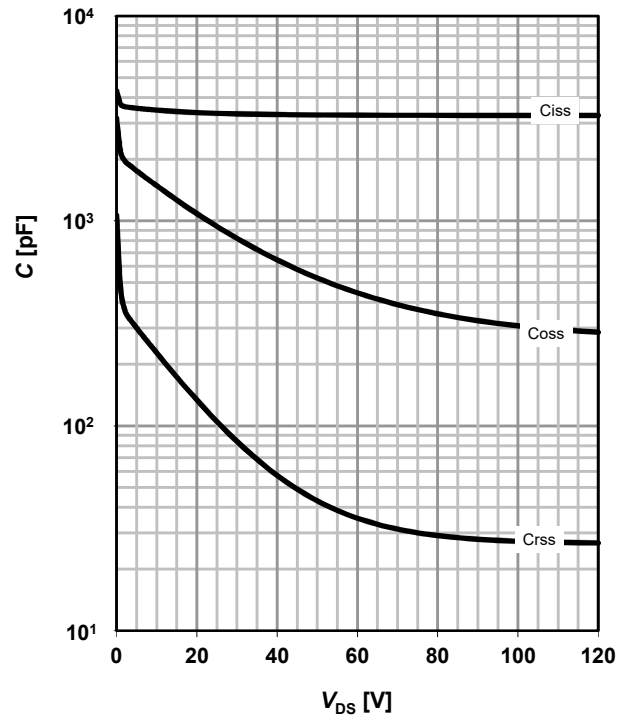
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

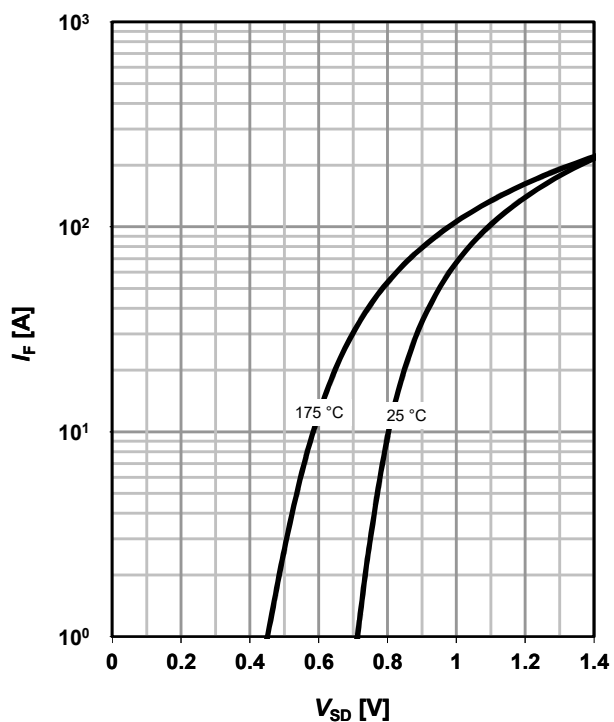
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

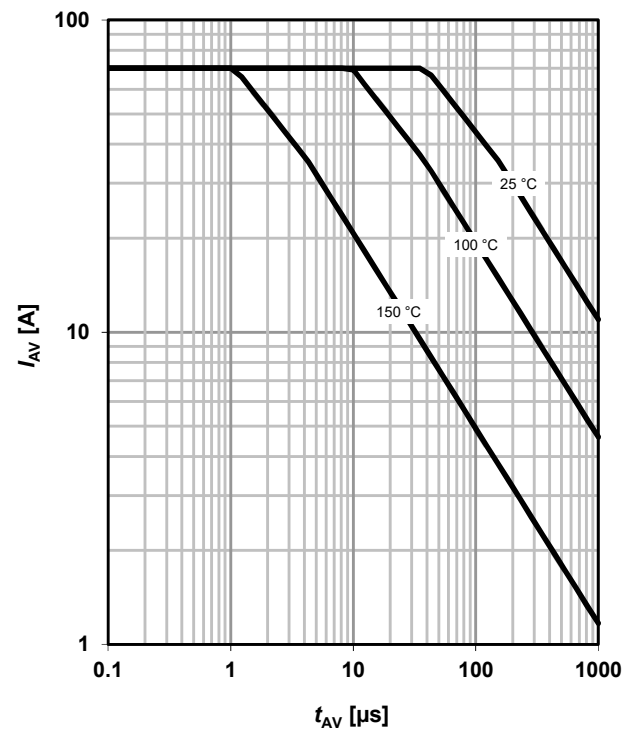
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$





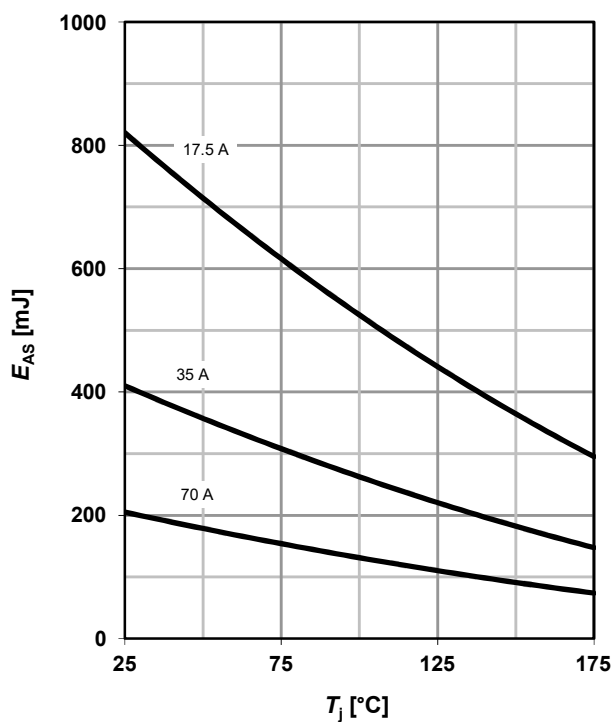
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13 Typical avalanche energy

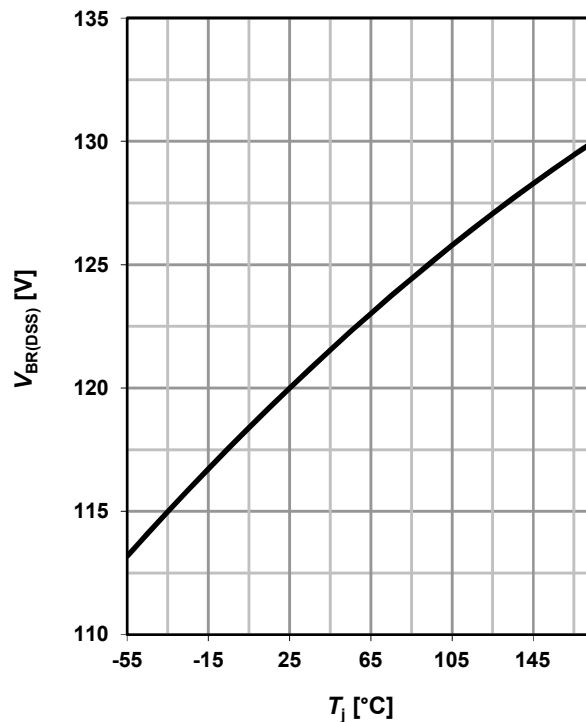
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Typ. drain-source breakdown voltage

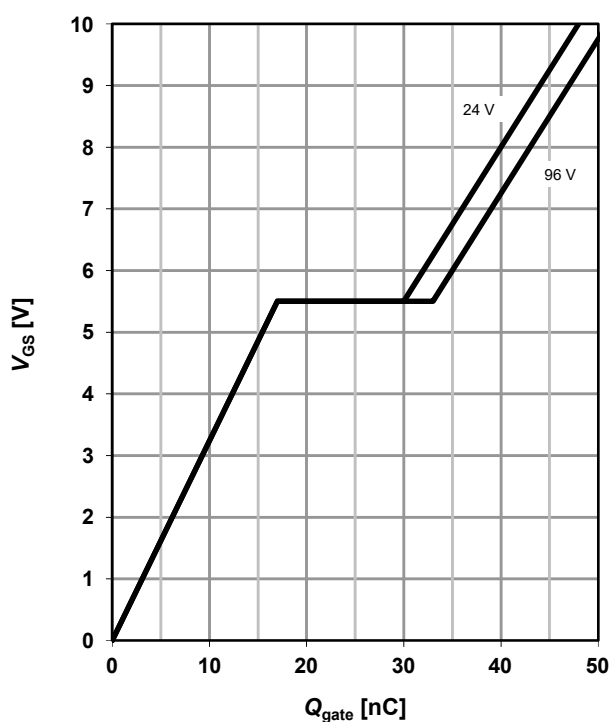
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



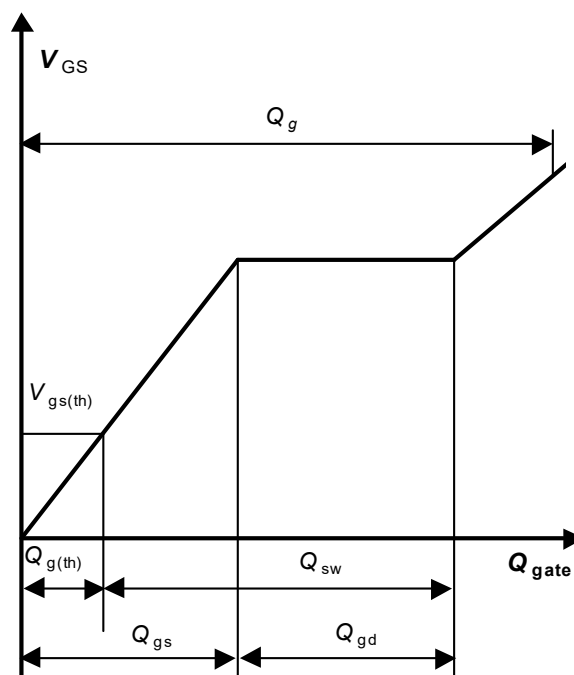
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 70 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	2016-06-20	Final Data Sheet
Revision 1.1	2023-06-15	Diagram 8 Typ. drain-source on-state resistance: used α value clarified
Revision 1.1	2023-06-15	Corrected diagram 10 typical capacitances