

MOSFET

OptiMOS™5 Power-Transistor, 80 V

Features

- Optimized for battery powered applications
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications
- Halogen-free according to IEC61249-2-21

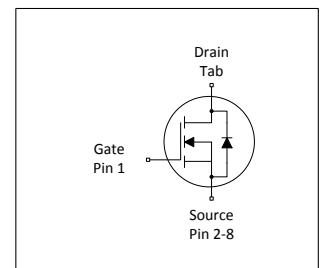


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	1.4	mΩ
I_D	331	A
Q_{oss}	187	nC
$Q_G(0V..10V)$	160	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IPT014N08NM5	PG-HSOF-8	014N08N5	-

¹⁾ J-STD20 and JESD22

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	331 234 37	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1324	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	632	mJ	$I_D=150\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	300	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.27	0.5	°C/W	-
Device on PCB, top	R_{thJA}	-	-	62	°C/W	-
Device on PCB, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	40	°C/W	-

¹⁾ Rating refer to the product only with data sheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environment conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D=280\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.1 1.5	1.4 1.7	m Ω	$V_{GS}=10\text{ V}$, $I_D=150\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=75\text{ A}$
Gate resistance ¹⁾	R_G	-	1.4	2.1	Ω	-
Transconductance	g_{fs}	160	240	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=100\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	11000	14000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	1800	2300	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	78	140	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	32	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Rise time	t_r	-	16.2	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	61	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Fall time	t_f	-	17.6	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	51	-	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	34	-	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	34	50	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	51	-	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	160	200	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	138	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ²⁾	Q_{oss}	-	187	249	nC	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	213	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1324	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.85	1.2	V	$V_{GS}=0\text{ V}$, $I_F=100\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	60.5	121	ns	$V_R=40\text{ V}$, $I_F=100\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	169	338	nC	$V_R=40\text{ V}$, $I_F=100\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

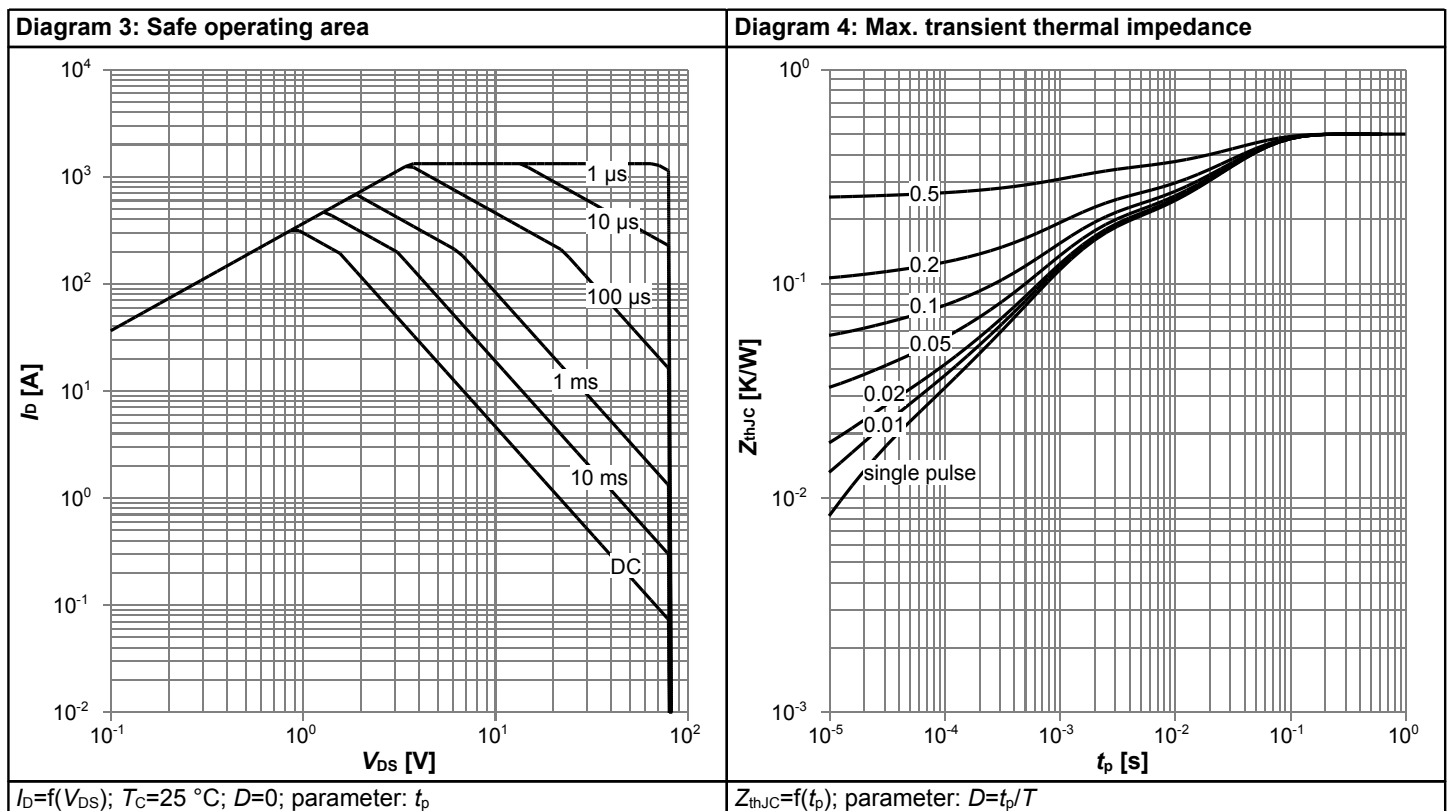
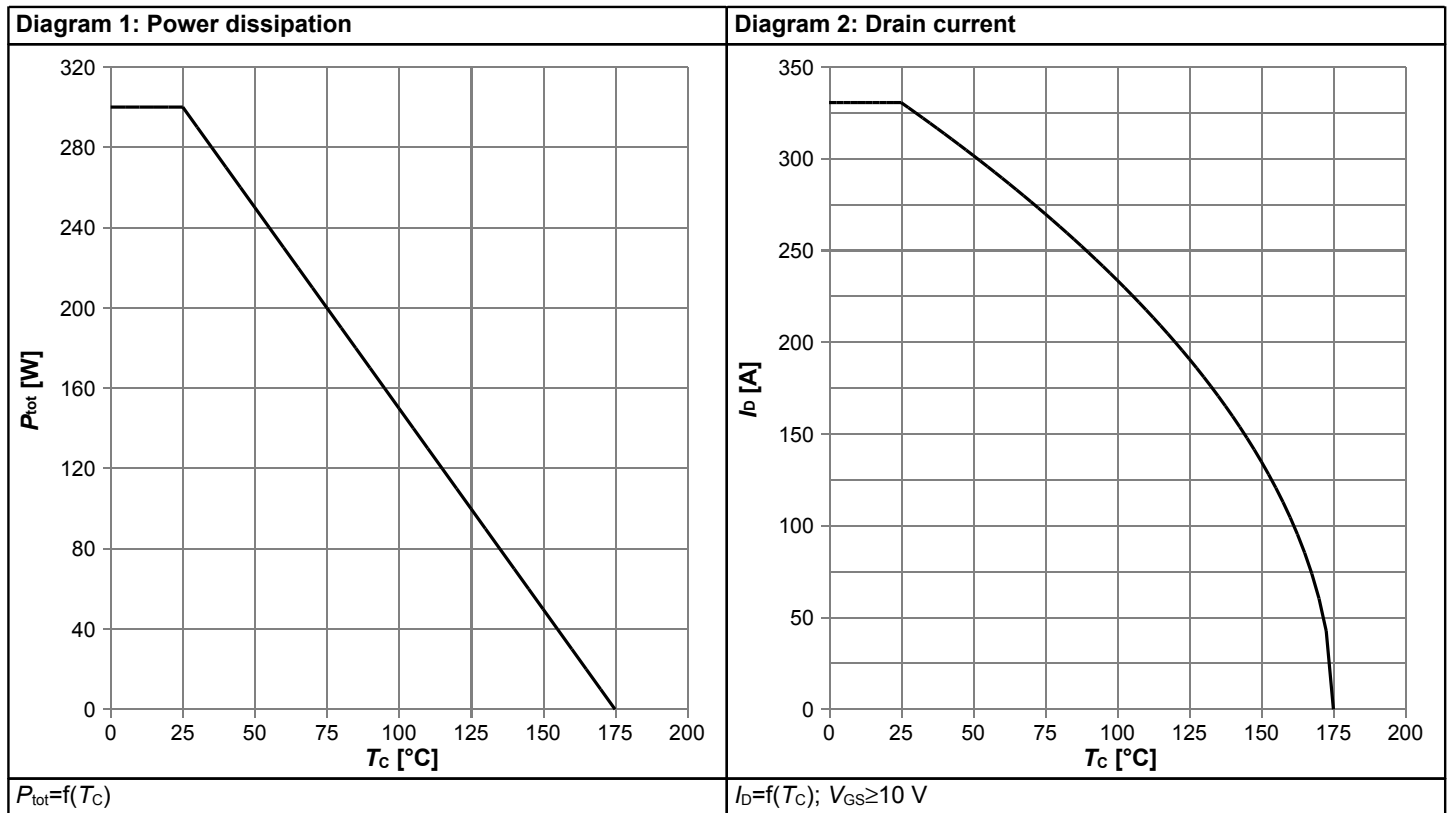
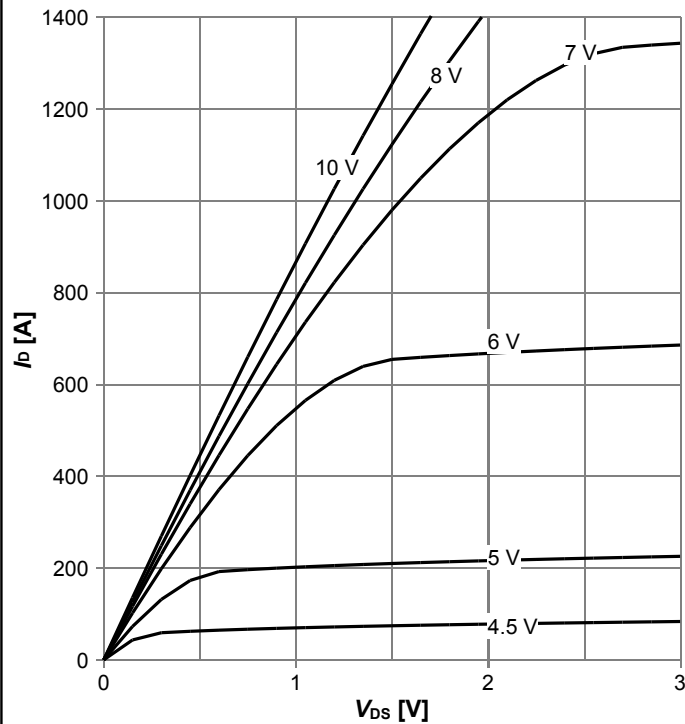
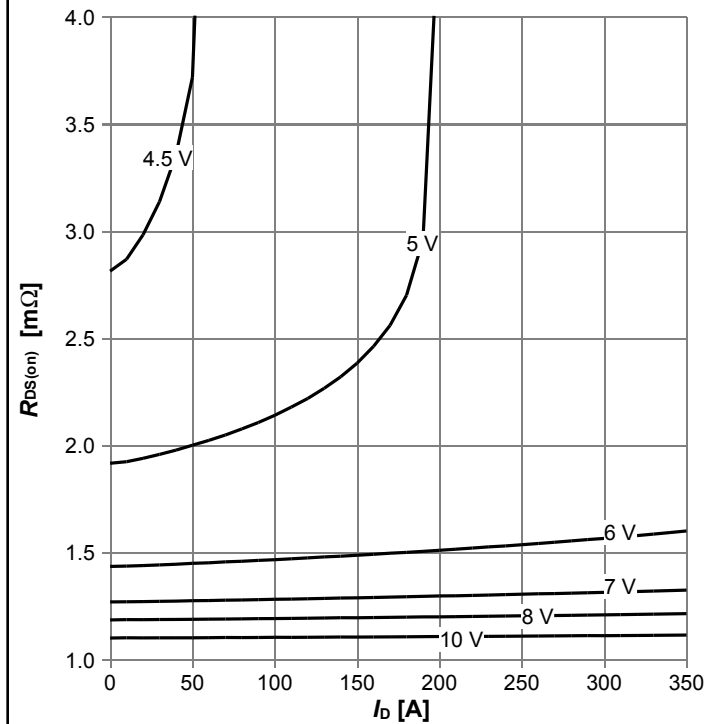


Diagram 5: Typ. output characteristics



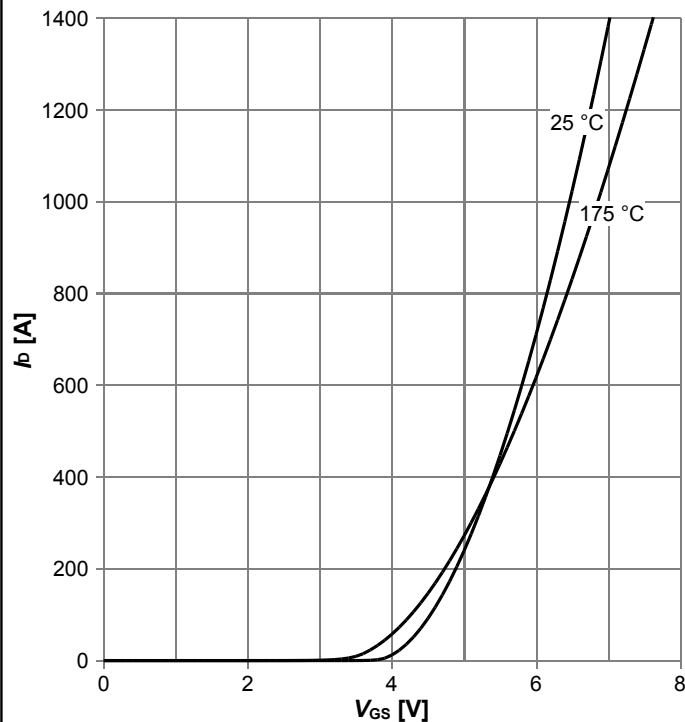
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



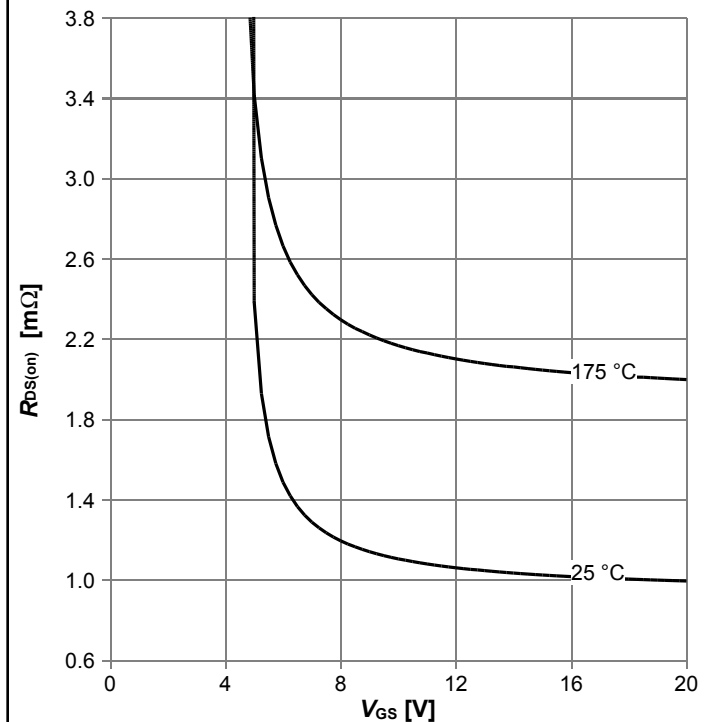
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



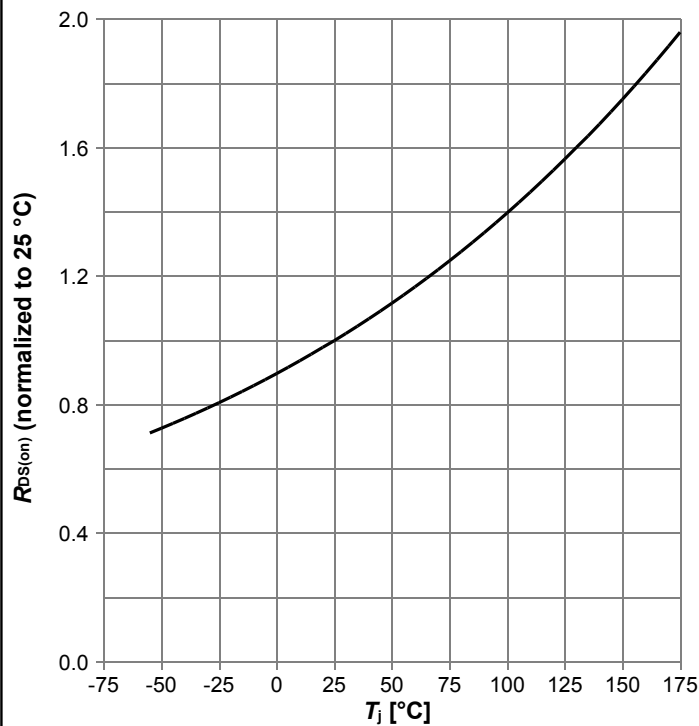
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



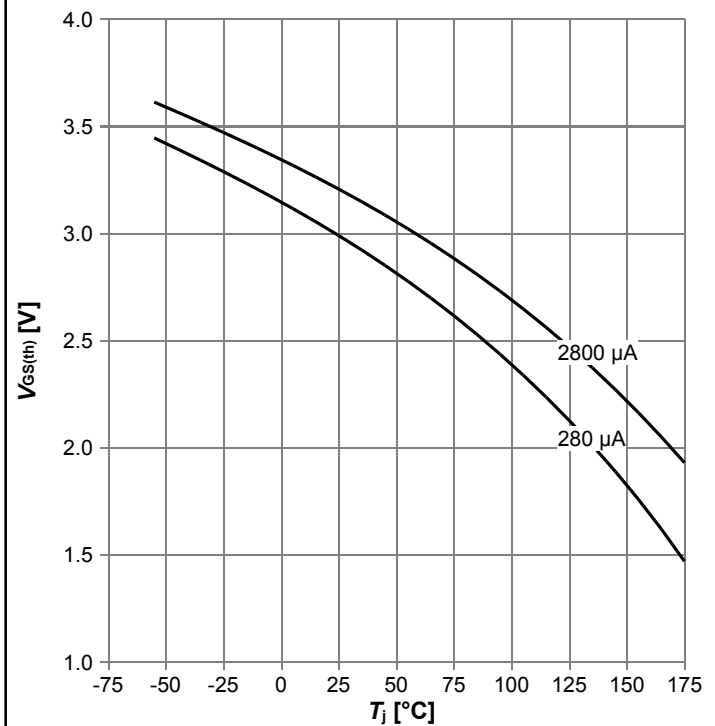
$R_{DS(on)} = f(V_{GS})$, $I_D = 150\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



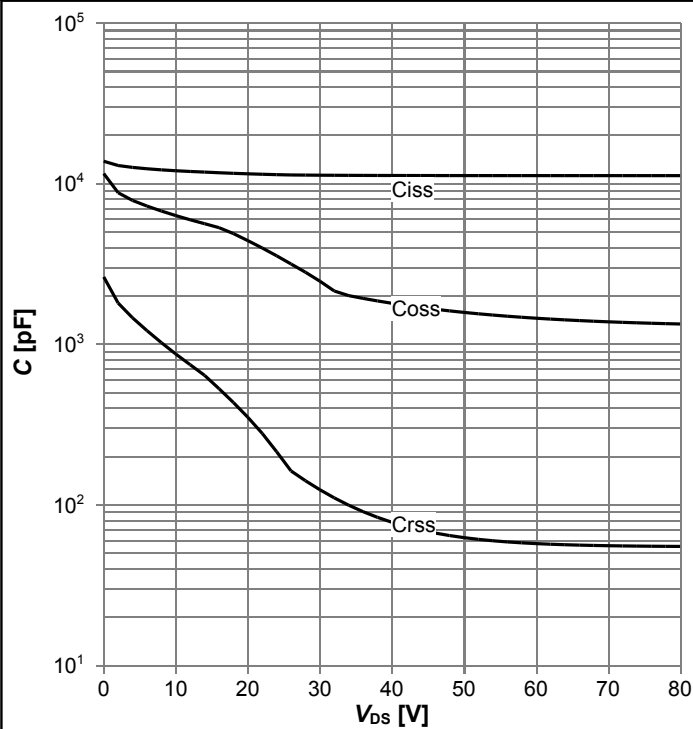
$R_{DS(on)} = f(T_j)$, $I_D = 150$ A, $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



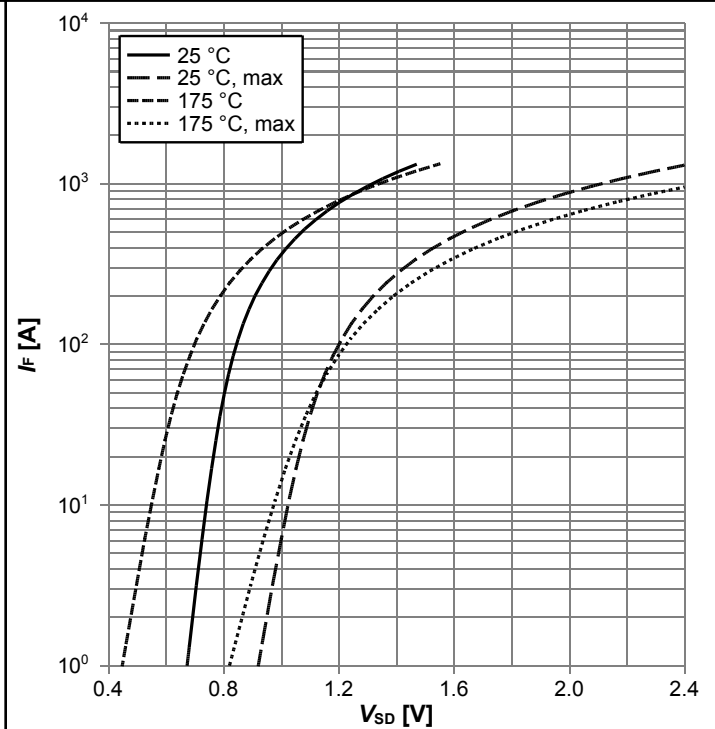
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



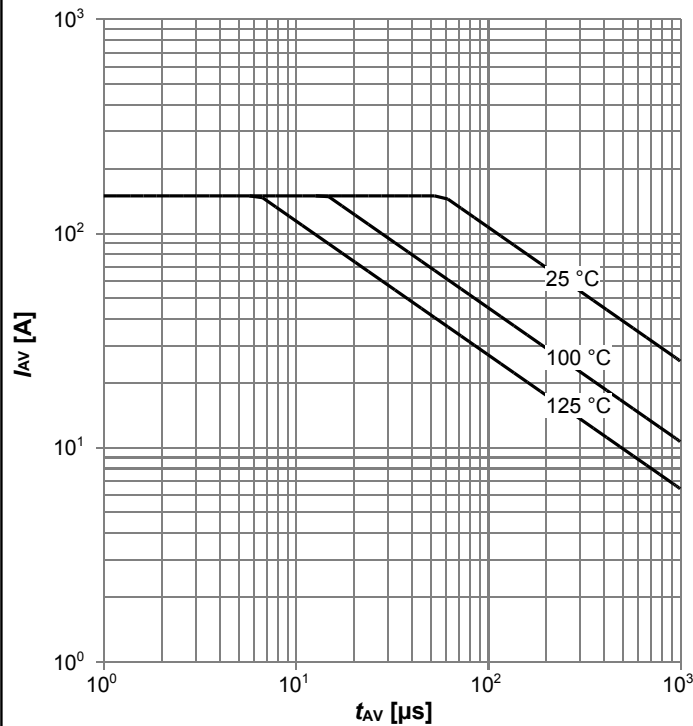
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



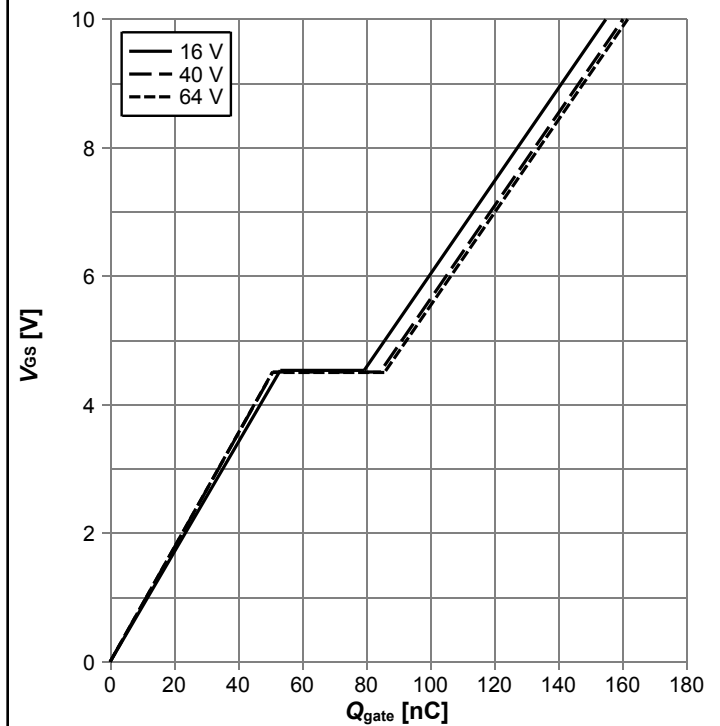
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



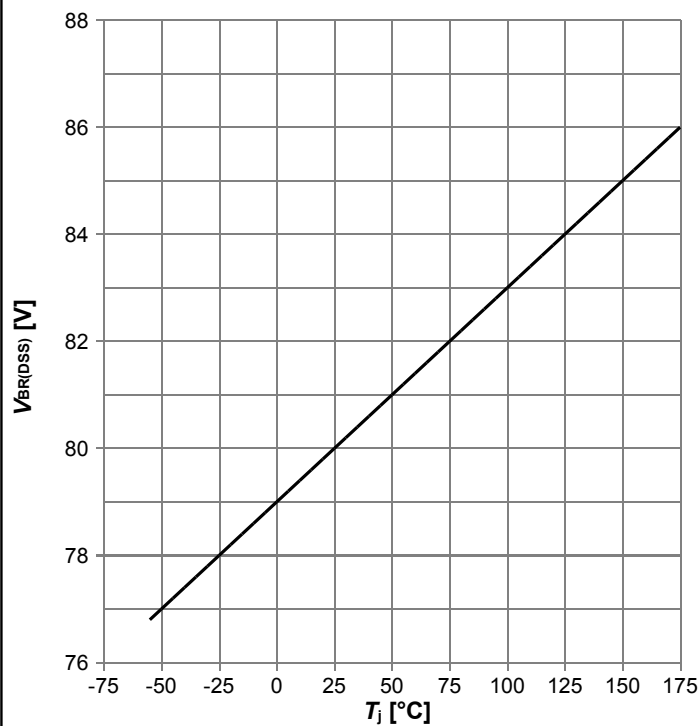
$I_{AS}=f(t_{AV})$; $R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



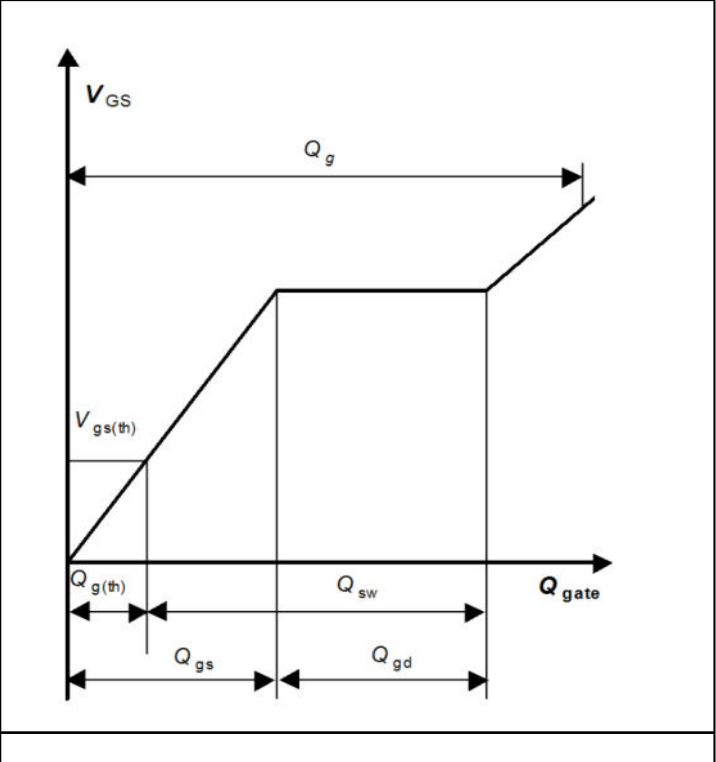
$V_{GS}=f(Q_{gate})$, $I_D=100$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines

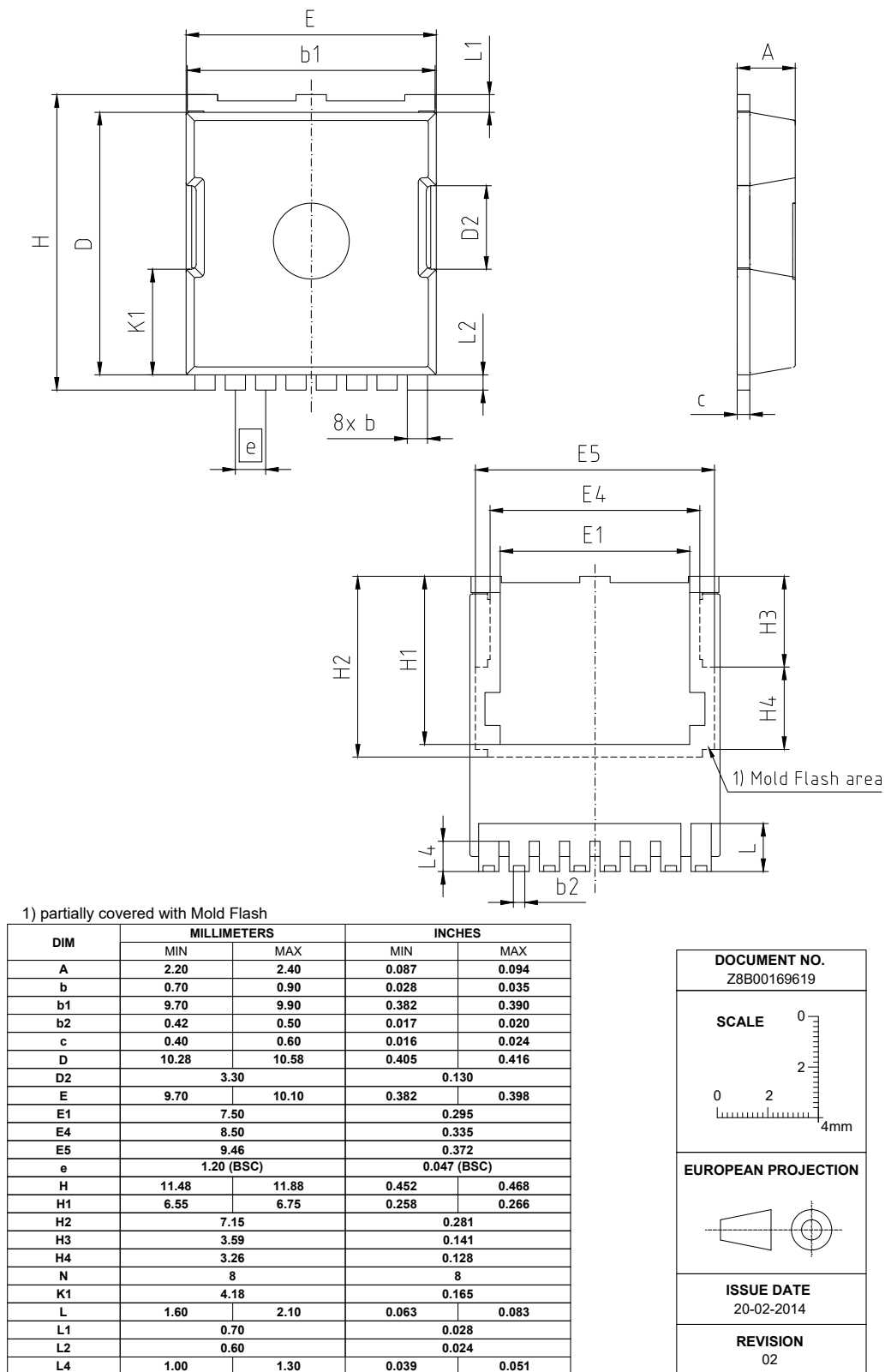


Figure 1 Outline PG-HSOF-8, dimensions in mm/inches

Revision History

IPT014N08NM5

Revision: 2020-12-18, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2020-12-18	Release of final version

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