

MOSFET

StrongIRFET™ Power MOSFET, 100 V

Features

- Very low on-resistance $R_{ds(on)}$
- Excellent gate charge x $R_{ds(on)}$ (FOM)
- Optimized Q_{rr}
- 175°C operating temperature
- Product validation according to JEDEC standard
- Optimized for broadest availability from distribution partners

Benefits

- Reduced conduction losses
- Ideal for high switching frequency
- Lower overshoot voltage
- Increased reliability versus 150°C rated parts
- Pb-free lead plating; RoHS compliant
- Lead free, Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	1.7	mΩ
I_D	203	A
Q_{oss}	213	nC
Q_G (0V..10V)	168	nC

Type / Ordering code	Package	Marking	Related links
IRF100P219	PG-TO247-3	IRF100P219	-

PG-TO247-3

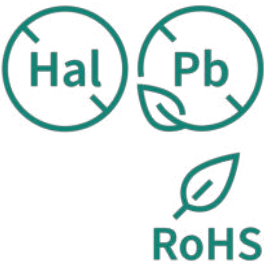
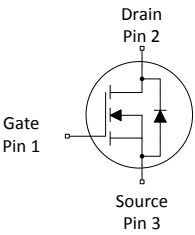
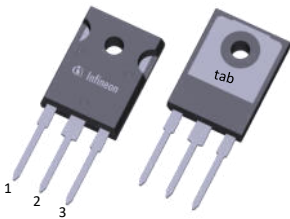




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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	203 156 33	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	812	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	464	mJ	$I_D=100\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	341 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information.

⁴⁾ See Diagram 13 for more detailed information.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.3	0.44	°C/W	-
Thermal resistance, junction - ambient ⁵⁾	R_{thJA}	-	-	40	°C/W	
Case-to-Sink, Flat Greased Surface	R_{thCS}	-	0.24	-	°C/W	

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.3	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D=278\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.4 1.7	1.7 2.1	m Ω	$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=50\text{ A}$
Gate resistance	R_G	-	1.2	-	Ω	-
Transconductance ⁶⁾	g_{fs}	135	270	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=100\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁷⁾	C_{iss}	-	12000	16000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}	-	1800	2300	pF	
Reverse transfer capacitance ⁷⁾	C_{rss}	-	80	140	pF	
Turn-on delay time	$t_{d(on)}$	-	67	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	106	-	ns	
Turn-off delay time	$t_{d(off)}$	-	132	-	ns	
Fall time	t_f	-	47	-	ns	

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	53	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	36	-	nC	
Gate to drain charge ⁹⁾	Q_{gd}	-	34	51	nC	
Switching charge	Q_{sw}	-	51	-	nC	
Gate charge total ⁹⁾	Q_g	-	168	210	nC	
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	146	-	nC	
Output charge ⁹⁾	Q_{oss}	-	213	320	nC	

⁸⁾ See figure 16 for gate charge parameter definition.

⁹⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	173	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	812	A	
Diode forward voltage	V_{SD}	-	0.86	1.0	V	$V_{GS}=0\text{ V}$, $I_F=100\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	63	-	ns	$V_R=50\text{ V}$, $I_F=100\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	111	-	nC	

4 Electrical characteristics diagrams

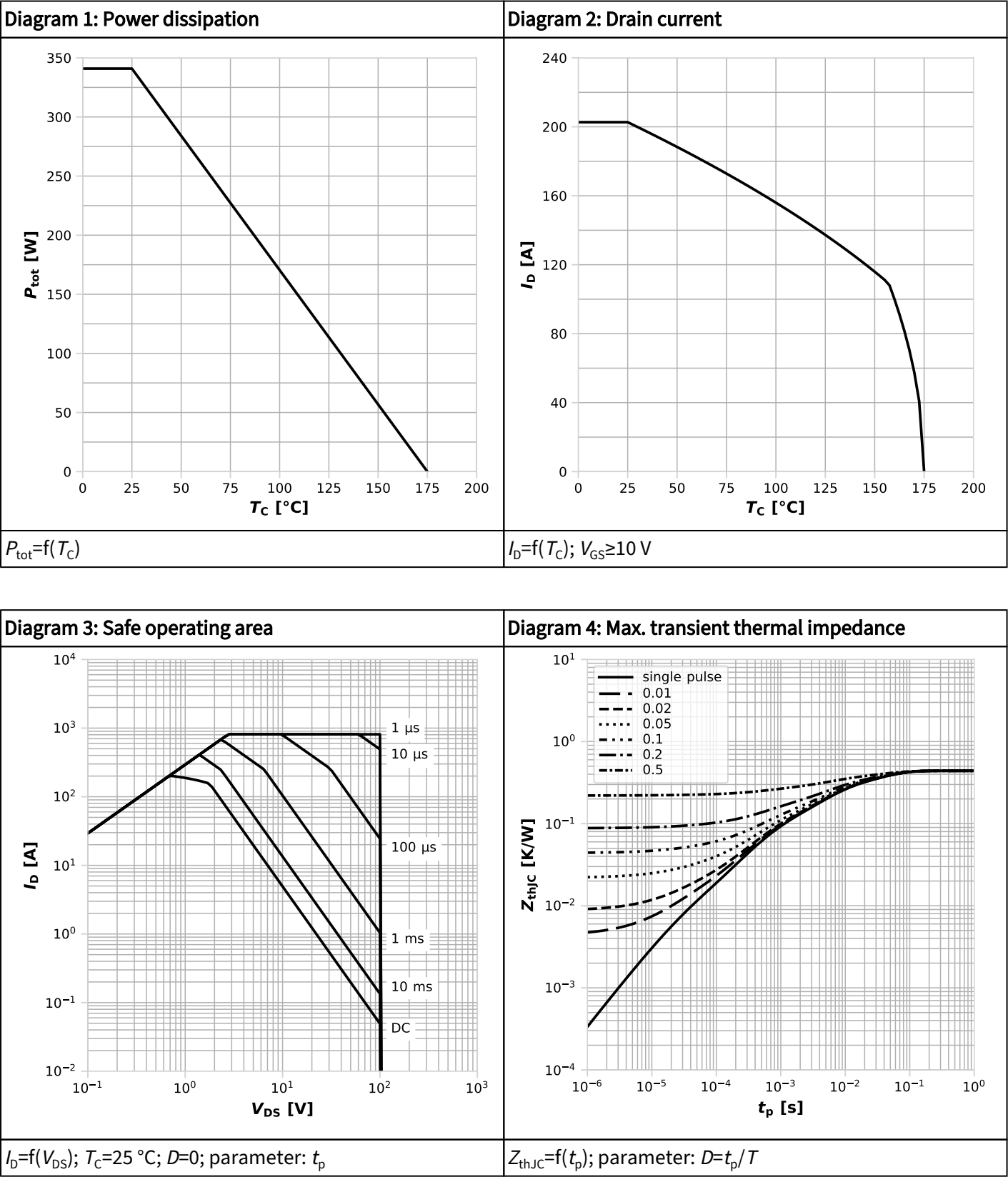
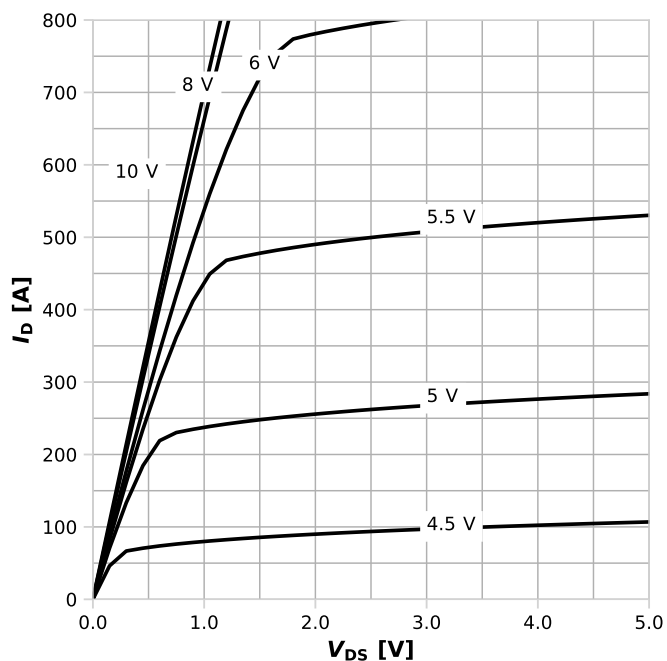
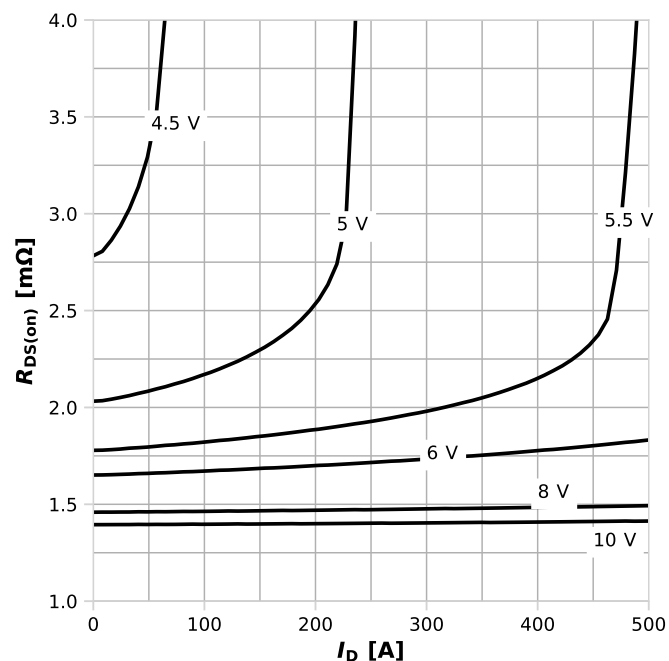


Diagram 5: Typ. output characteristics



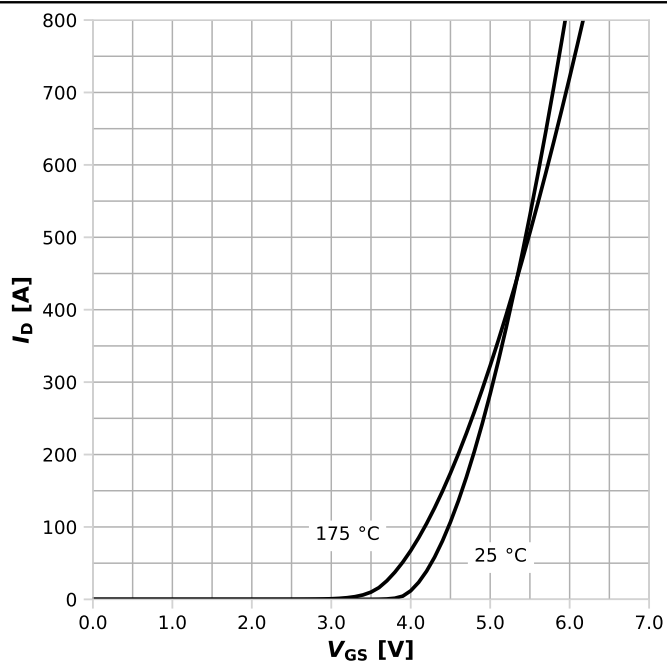
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



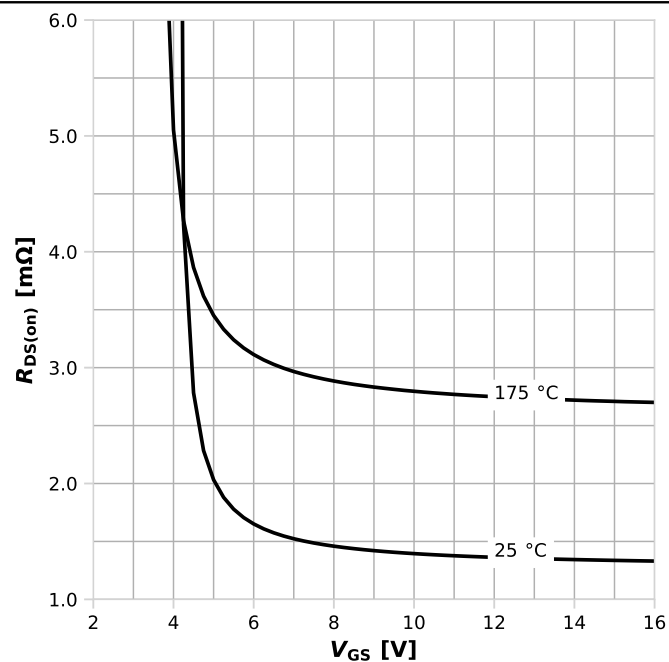
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



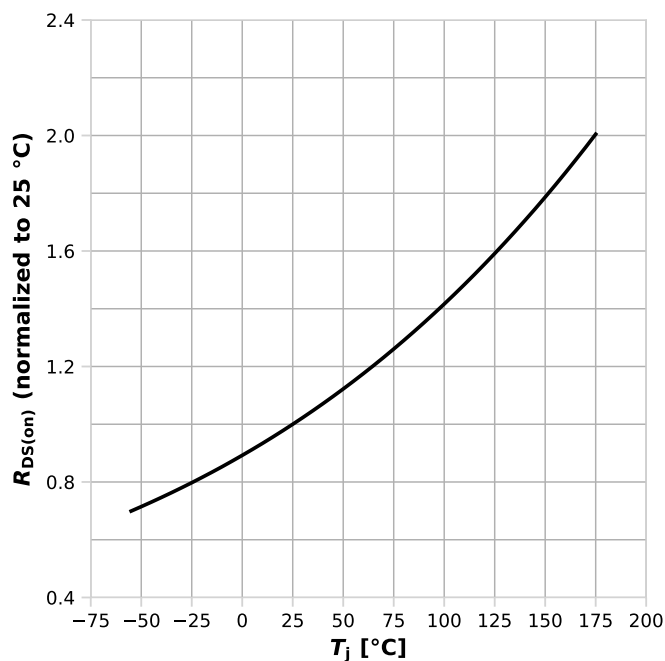
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)\max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



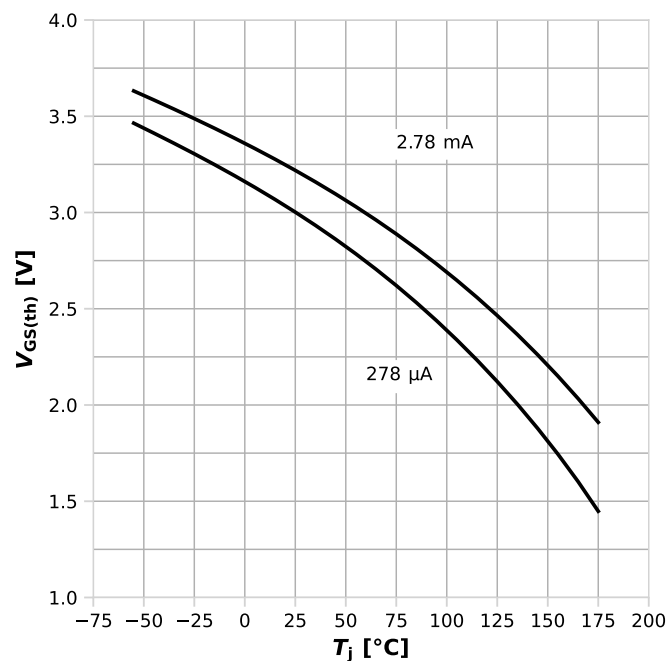
$R_{DS(on)} = f(V_{GS})$, $I_D = 0$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



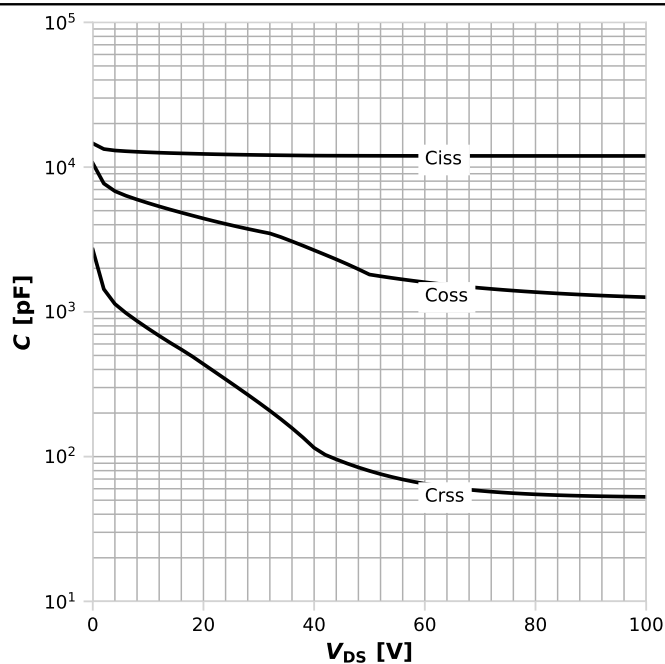
$$R_{DS(on)} = f(T_j), I_D = 0 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



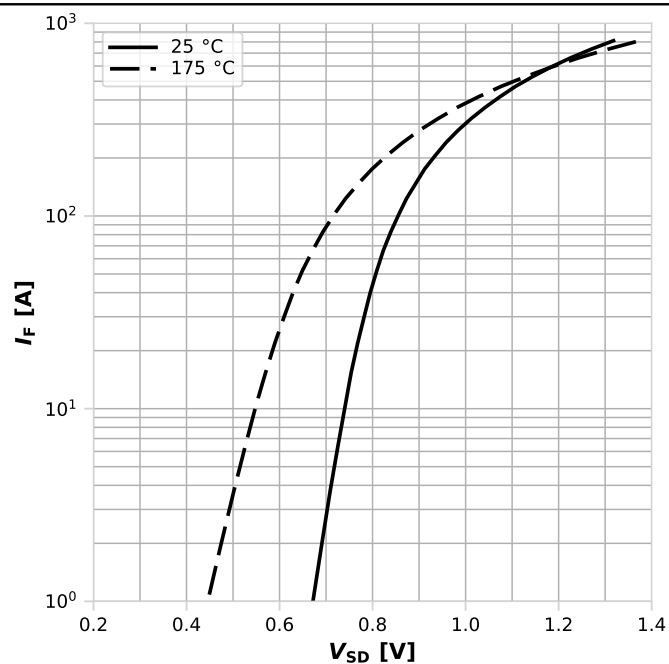
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances

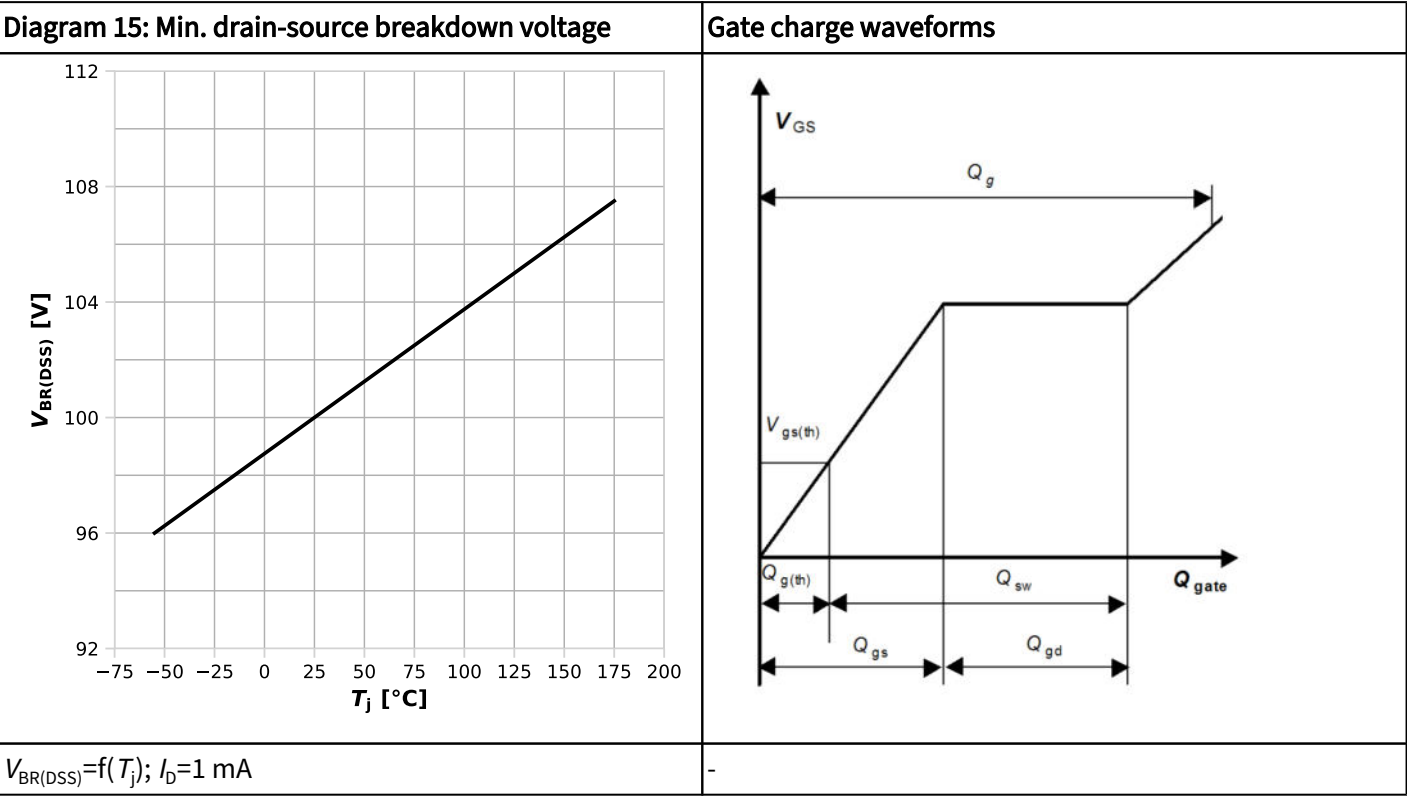
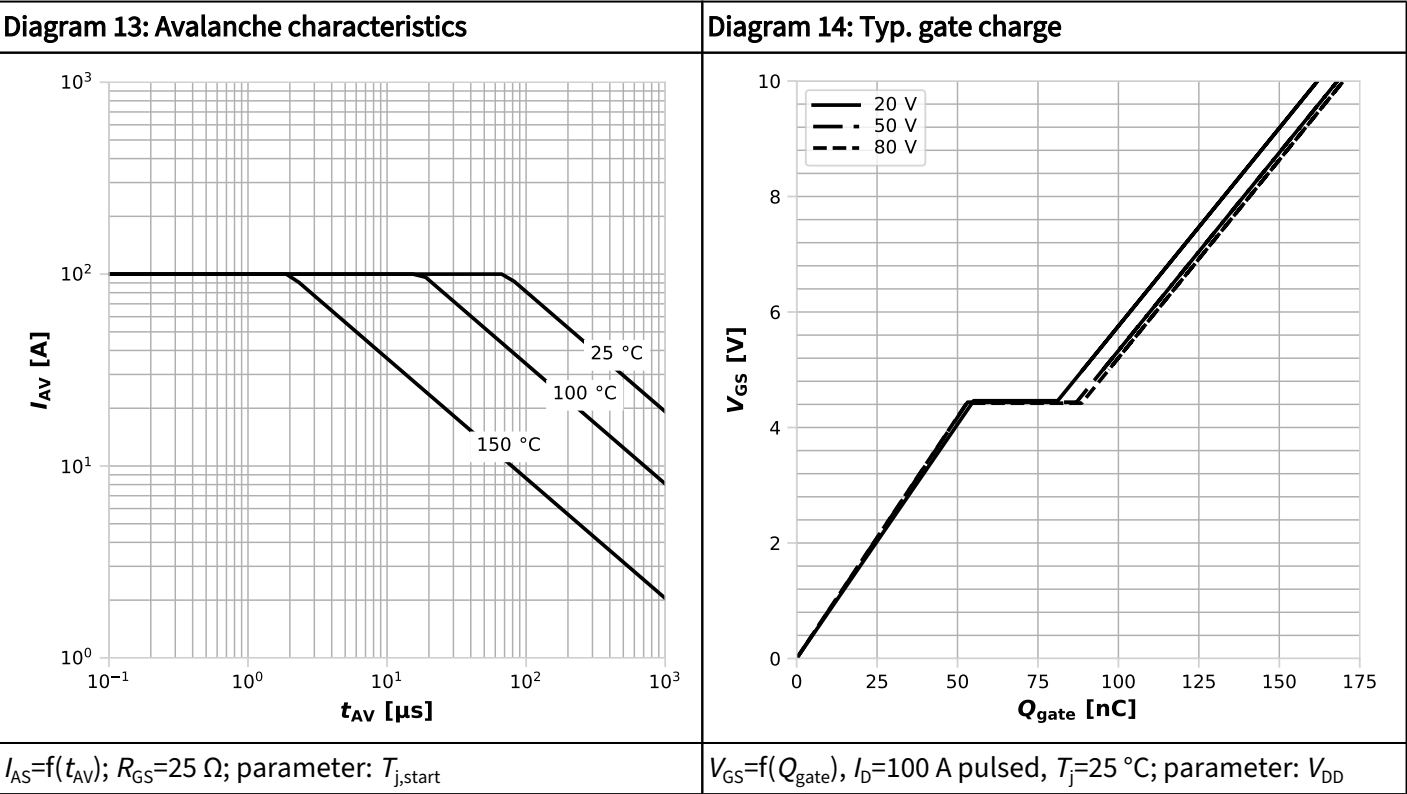


$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

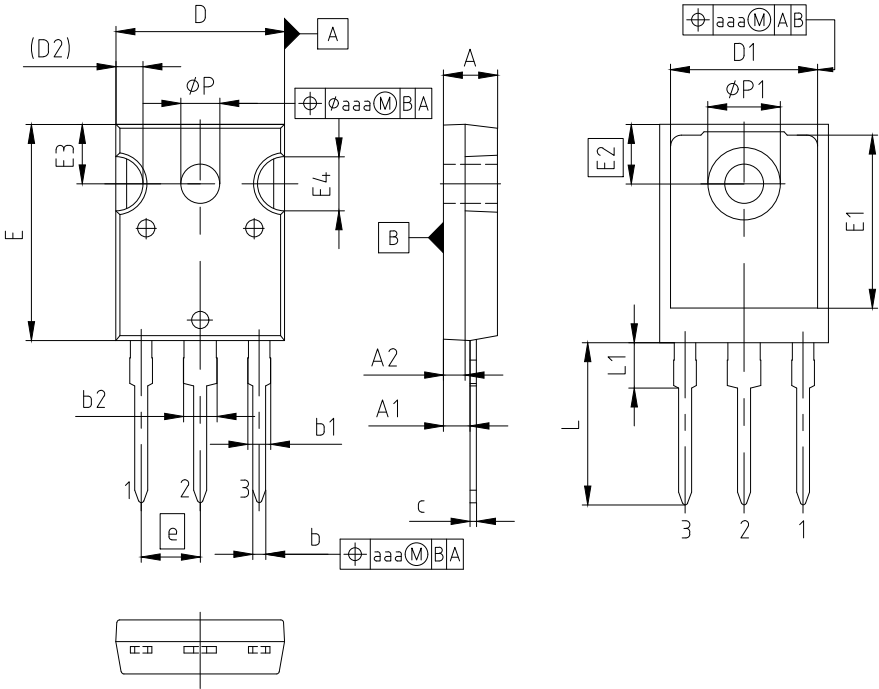
Diagram 12: Forward characteristics of reverse diode



$$I_F = f(V_{SD}); \text{ parameter: } T_j$$



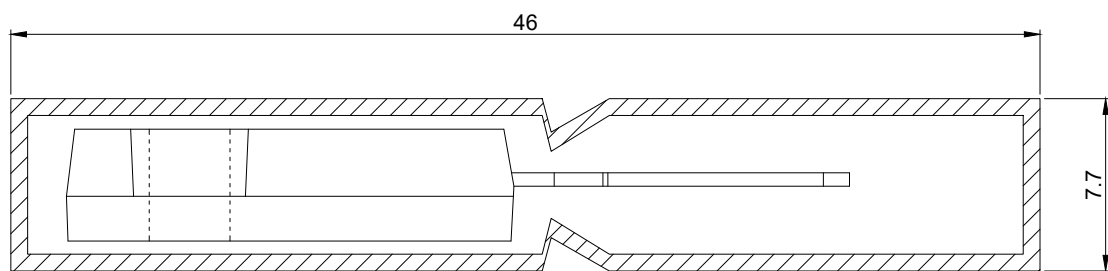
5 Package outlines



PACKAGE - GROUP NUMBER: PG-T0247-3-U03					
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	4.83	5.13	E2	5.51	
A1	2.21	2.59	E3	5.31	5.69
A2	1.50	2.50	E4	4.50	5.50
b	0.99	1.41	e	5.46	
b1	1.65	2.39	L	14.20	16.10
b2	2.59	3.43	L1	3.71	4.29
c	0.38	0.89	N	3	
D	15.29	15.87	ØP	3.56	3.66
D1	13.46	13.66	ØP1	7.19	7.39
D2	2.50		aaa	0.25	
E	19.70	20.70			
E1	13.08	13.28			

NOTES: (1) DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
(2) N IS THE NUMBER OF LEADS

Figure 1 Outline PG-T0247-3, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 2 Packaging variant PG-T0247-3, dimensions in mm

Revision history

IRF100P219

Revision 2025-01-09, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2018-10-16	Release of final version
2.1	2020-01-20	Update from IR MOSFT/StrongIRFET™ to StrongIRFET™
2.2	2025-01-09	updated switch time and trr

Trademarks

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81726 München, Germany
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