

# International IR Rectifier

- Advanced Process Technology
- Ultra Low On-Resistance
- P-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

## Description

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and dual-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	-4.6	
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	-3.7	A
$I_{DM}$	Pulsed Drain Current ①	-15	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	2.5	W
	Linear Derating Factor	0.020	W/ $^\circ\text{C}$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$dv/dt$	Peak Diode Recovery $dv/dt$ ②	-3.0	V/nS
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to + 150	$^\circ\text{C}$

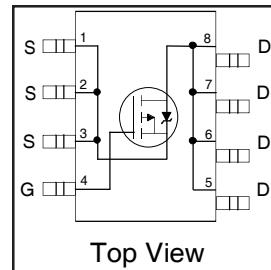
## Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	—	50	$^\circ\text{C/W}$

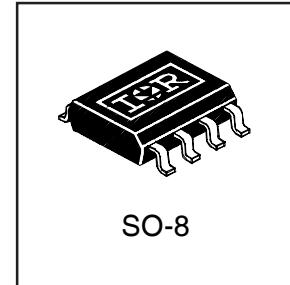
PD - 95021

# IRF7205PbF

HEXFET® Power MOSFET



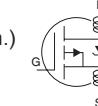
$V_{DSS} = -30\text{V}$   
 $R_{DS(on)} = 0.070\Omega$   
 $I_D = -4.6\text{A}$



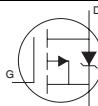
# IRF7205PbF

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## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	-30	---	---	V	$V_{\text{GS}} = 0\text{V}$ , $I_D = -250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/T_J}$	Breakdown Voltage Temp. Coefficient	---	-0.024	---	$\text{V}/^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = -1\text{mA}$
$R_{\text{DS}(\text{ON})}$	Static Drain-to-Source On-Resistance	---	0.070	$\Omega$	$V_{\text{GS}} = -10\text{V}$ , $I_D = -4.6\text{A}$ ③	
		---	0.130		$V_{\text{GS}} = -4.5\text{V}$ , $I_D = -2.0\text{A}$ ③	
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	-1.0	---	-3.0	V	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = -250\mu\text{A}$
$g_{\text{fs}}$	Forward Transconductance	---	6.6	---	S	$V_{\text{DS}} = -15\text{V}$ , $I_D = -4.6\text{A}$ ③
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	---	---	-1.0	$\mu\text{A}$	$V_{\text{DS}} = -24\text{V}$ , $V_{\text{GS}} = 0\text{V}$
		---	---	-5.0		$V_{\text{DS}} = -15\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $T_J = 70^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	---	---	-100	$\text{nA}$	$V_{\text{GS}} = -20\text{V}$
	Gate-to-Source Reverse Leakage	---	---	100		$V_{\text{GS}} = 20\text{V}$
$Q_g$	Total Gate Charge	---	27	40	nC	$I_D = -4.6\text{A}$
$Q_{\text{gs}}$	Gate-to-Source Charge	---	5.2	---		$V_{\text{DS}} = -15\text{V}$
$Q_{\text{gd}}$	Gate-to-Drain ("Miller") Charge	---	7.5	---		$V_{\text{GS}} = -10\text{V}$ ③
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	---	14	30	ns	$V_{\text{DD}} = -15\text{V}$
$t_r$	Rise Time	---	21	60		$I_D = -1.0\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	---	97	150		$R_G = 6.0\Omega$
$t_f$	Fall Time	---	71	100		$R_D = 10\Omega$ ③
$L_D$	Internal Drain Inductance	---	2.5	---	nH	Between lead, 6mm(0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	---	4.0	---		
$C_{\text{iss}}$	Input Capacitance	---	870	---	pF	$V_{\text{GS}} = 0\text{V}$
$C_{\text{oss}}$	Output Capacitance	---	720	---		$V_{\text{DS}} = -10\text{V}$
$C_{\text{rss}}$	Reverse Transfer Capacitance	---	220	---		$f = 1.0\text{MHz}$

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	---	---	-2.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{\text{SM}}$	Pulsed Source Current (Body Diode) ①	---	---	-15		
$V_{\text{SD}}$	Diode Forward Voltage	---	---	-1.2	V	$T_J = 25^\circ\text{C}$ , $I_S = -1.25\text{A}$ , $V_{\text{GS}} = 0\text{V}$ ③
$t_{\text{rr}}$	Reverse Recovery Time	---	70	100	ns	$T_J = 25^\circ\text{C}$ , $I_F = -4.6\text{A}$
$Q_{\text{rr}}$	Reverse Recovery Charge	---	100	180	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ③
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

③ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

②  $I_{\text{SD}} \leq -4.6\text{A}$ ,  $dI/dt \leq 90\text{A}/\mu\text{s}$ ,  $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$ ,  $T_J \leq 150^\circ\text{C}$

④ Surface mounted on FR-4 board,  $t \leq 10\text{sec}$ .

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## IRF7205PbF

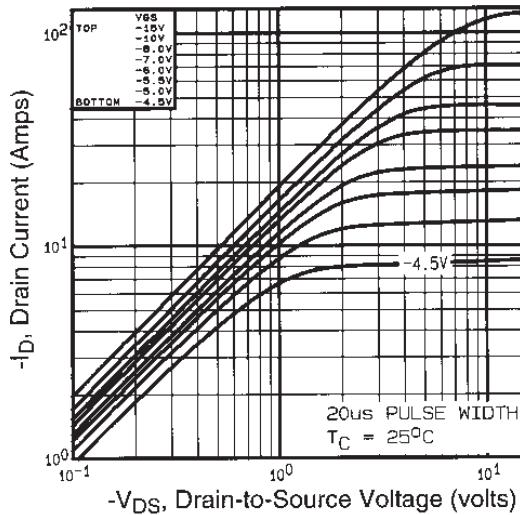


Fig 1. Typical Output Characteristics,

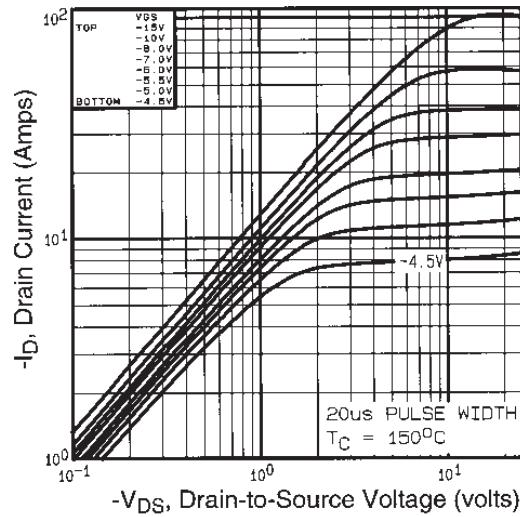


Fig 2. Typical Output Characteristics,

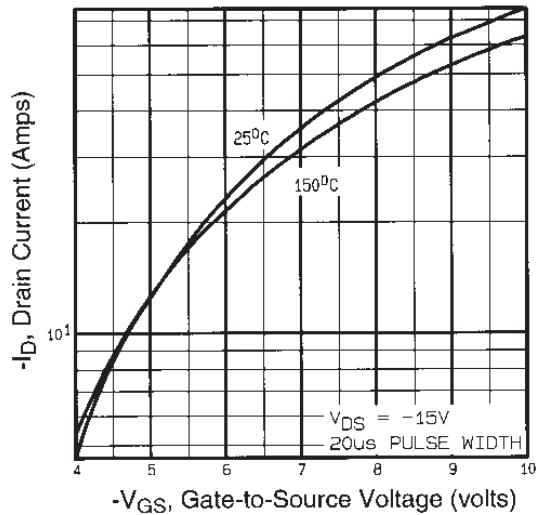


Fig 3. Typical Transfer Characteristics

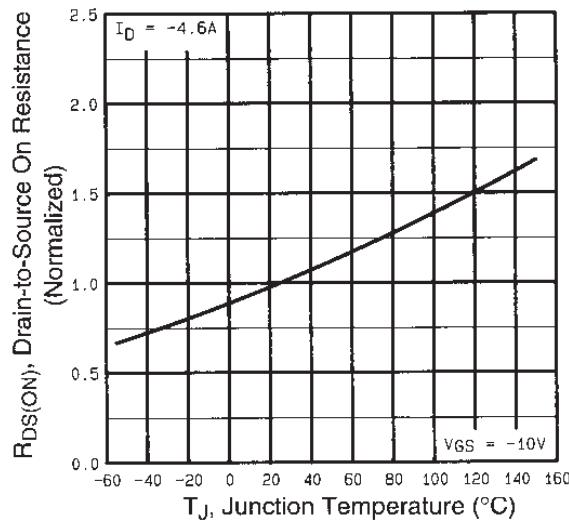
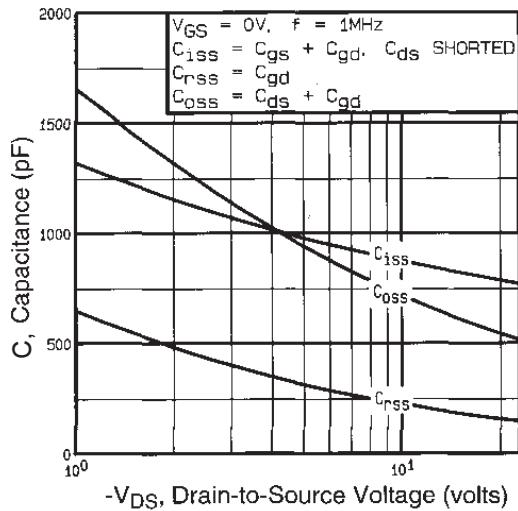


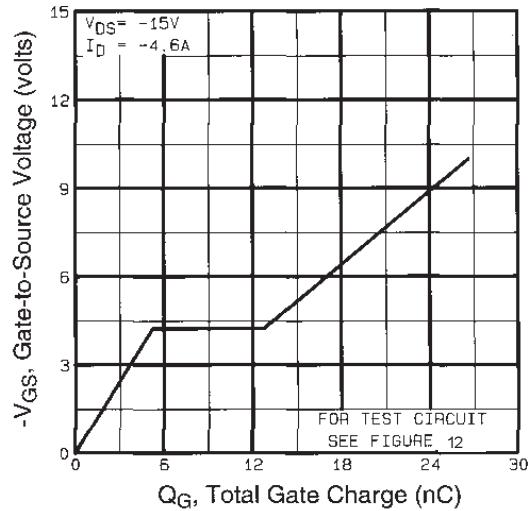
Fig 4. Normalized On-Resistance  
Vs. Temperature

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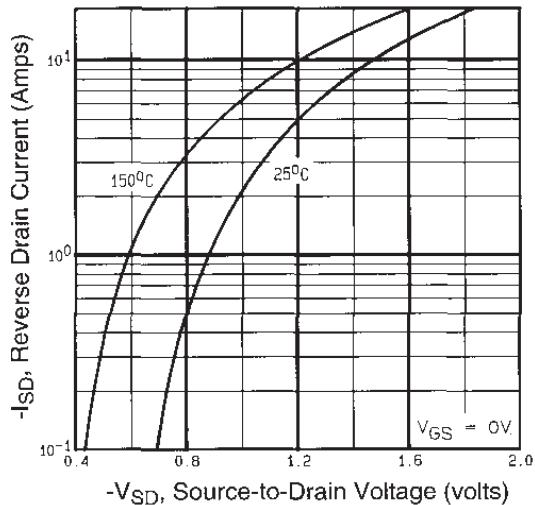
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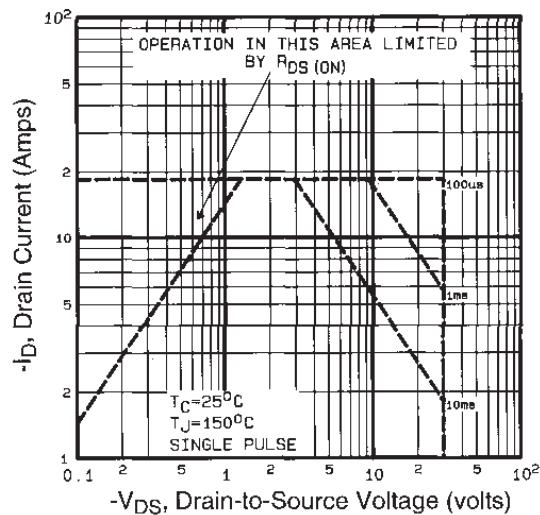
**Fig 5.** Typical Capacitance Vs.  
Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs.  
Gate-to-Source Voltage

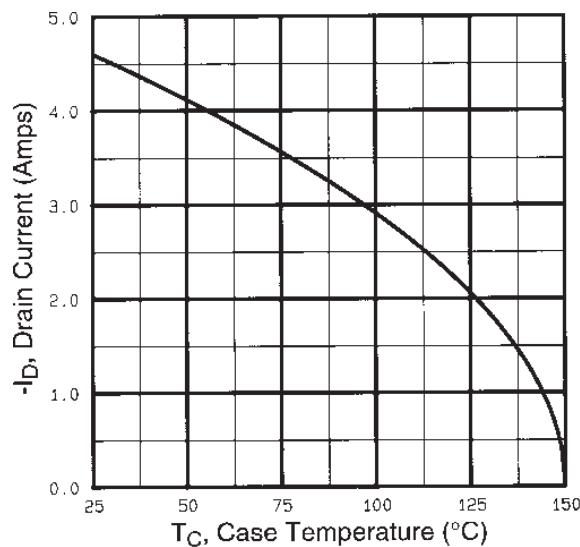


**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



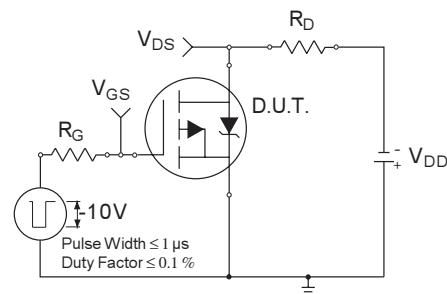
**Fig 8.** Maximum Safe Operating Area

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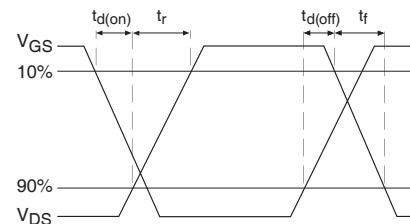


**Fig 9.** Maximum Drain Current Vs.  
Case Temperature

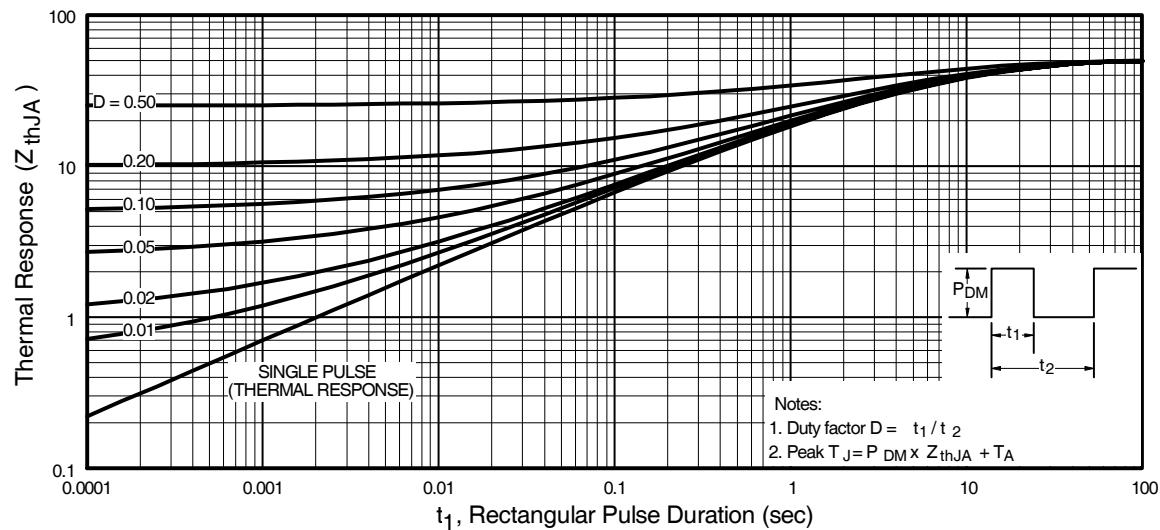
**IRF7205PbF**



**Fig 10a.** Switching Time Test Circuit



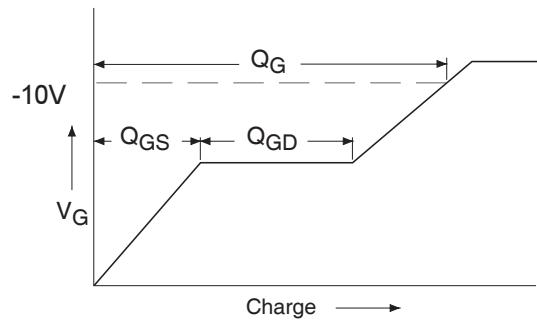
**Fig 10b.** Switching Time Waveforms



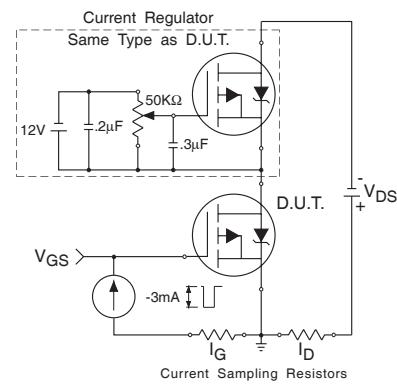
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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**Fig 12a.** Basic Gate Charge Waveform

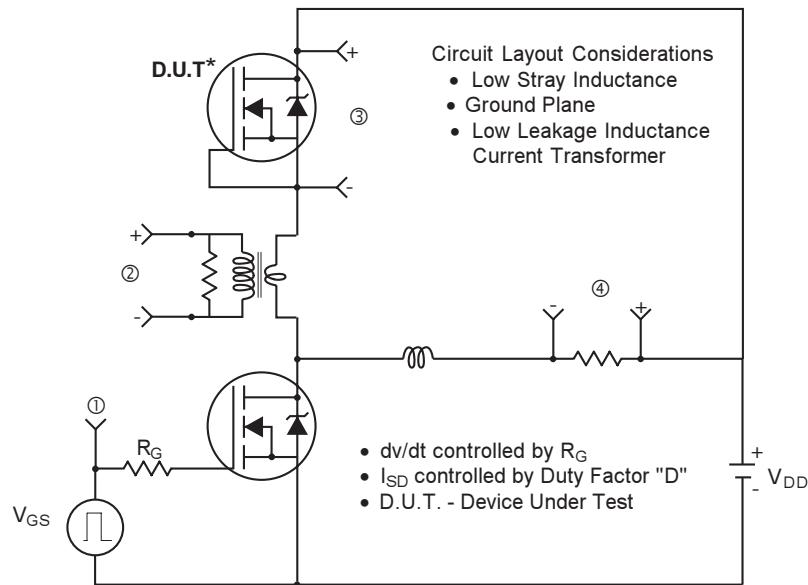


**Fig 12b.** Gate Charge Test Circuit

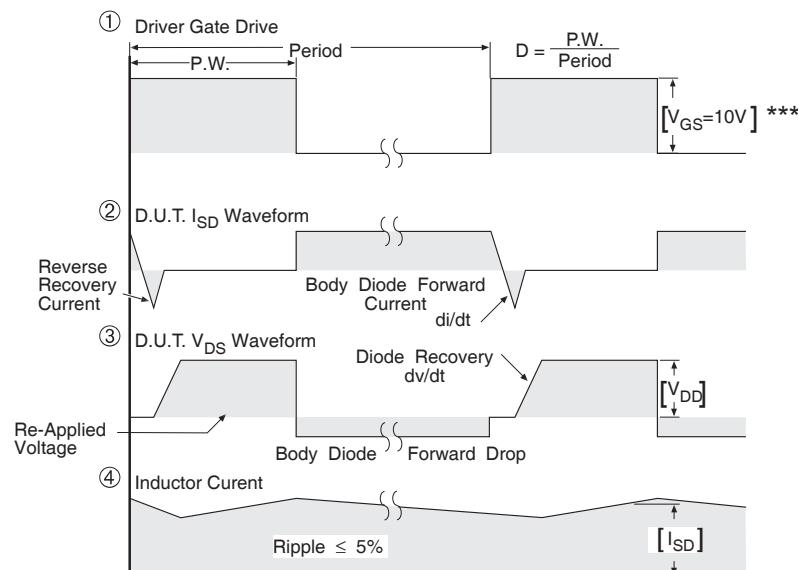
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**Peak Diode Recovery dv/dt Test Circuit**



\* Reverse Polarity of D.U.T for P-Channel

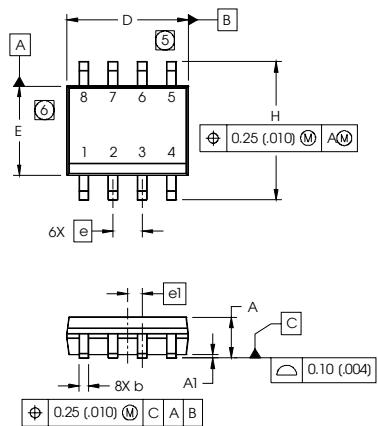


\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

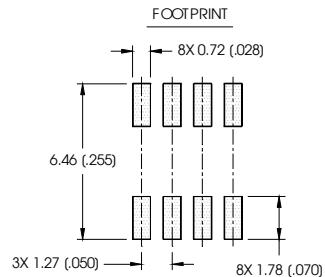
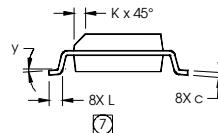
**Fig 13. For P-Channel HEXFETs**

## SO-8 Package Outline

Dimensions are shown in millimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e1	.050	BASIC	1.27	BASIC
e2	.025	BASIC	0.635	BASIC
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

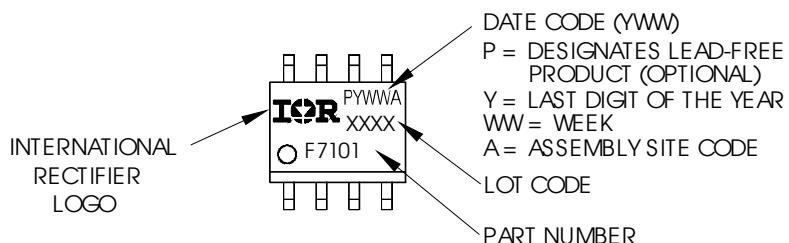


NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

## SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

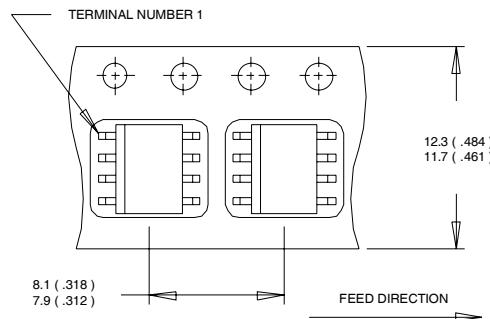


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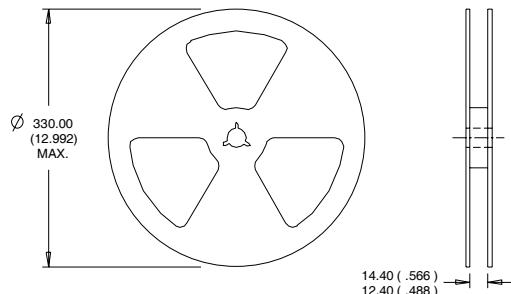
## SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.

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