

International
IR Rectifier

PD - 97173A

IRF7855PbF

HEXFET® Power MOSFET

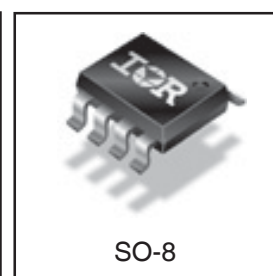
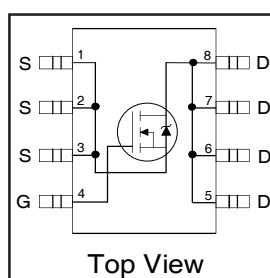
Applications

- Primary Side Switch in Bridge Topology in Isolated DC-DC Converters
- Primary Side Switch in Push-Pull Topology for 18-36Vin Isolated DC-DC Converters
- Secondary Side Synchronous Rectification Switch for 15Vout
- Suitable for 48V Non-Isolated Synchronous Buck DC-DC Applications

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

V_{DS}	$R_{DS(on)}$ max	I_D
60V	9.4mΩ @ $V_{GS} = 10V$	12A

**Absolute Maximum Ratings**

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	12	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V	8.7	
I_{DM}	Pulsed Drain Current ①	97	
P_D @ $T_A = 25^\circ C$	Maximum Power Dissipation ③	2.5	W
	Linear Derating Factor	0.02	W/°C
dv/dt	Peak Diode Recovery dv/dt ⑥	9.9	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	—	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ③ ⑦	—	50	

Notes ① through ⑦ are on page 8

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	72	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.4	9.4	m Ω	$V_{GS} = 10V, I_D = 12A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	4.9	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 60V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	14	—	—	S	$V_{DS} = 25V, I_D = 7.2A$
Q_g	Total Gate Charge	—	26	39	nC	$I_D = 7.2A$
Q_{gs}	Gate-to-Source Charge	—	6.8	—		$V_{DS} = 30V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	9.6	—		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	8.7	—	ns	$V_{DD} = 30V$
t_r	Rise Time	—	13	—		$I_D = 7.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	12	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	1560	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	440	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	120	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	1910	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	320	—		$V_{GS} = 0V, V_{DS} = 48V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	520	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V$ ⑤

Avalanche Characteristics

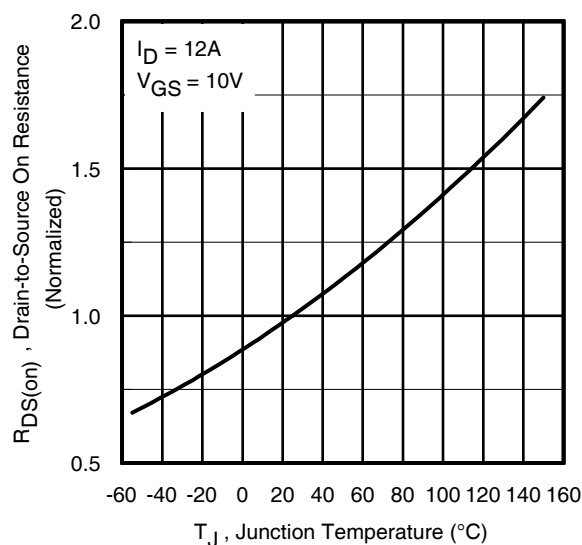
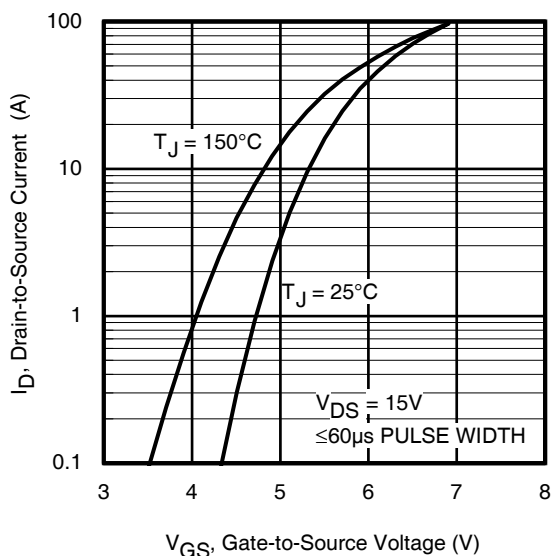
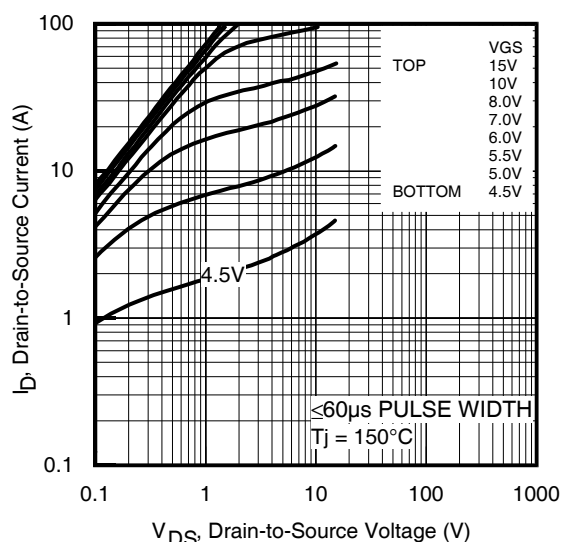
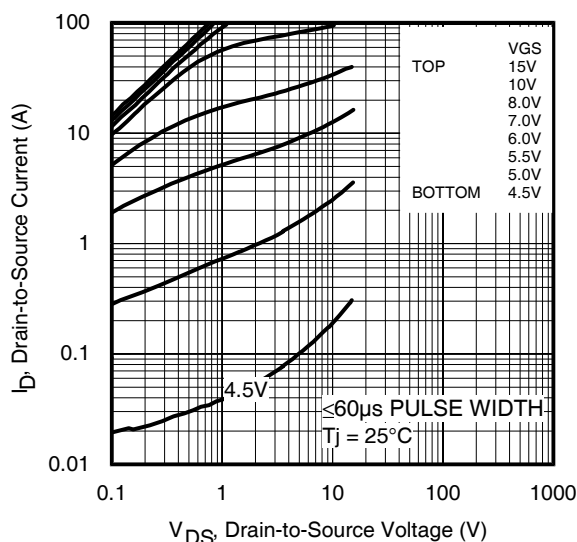
	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	540	mJ
I_{AR}	Avalanche Current ①	—	7.2	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.3	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	97		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 7.2A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	33	50	ns	$T_J = 25^\circ\text{C}, I_F = 7.2A, V_{DD} = 25V$
Q_{rr}	Reverse Recovery Charge	—	38	57	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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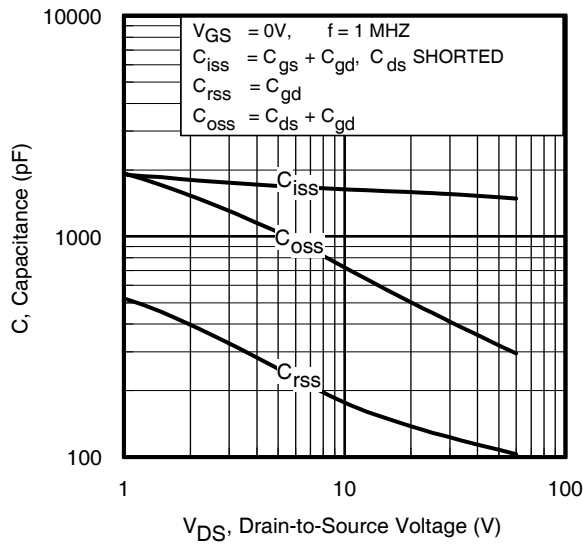


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

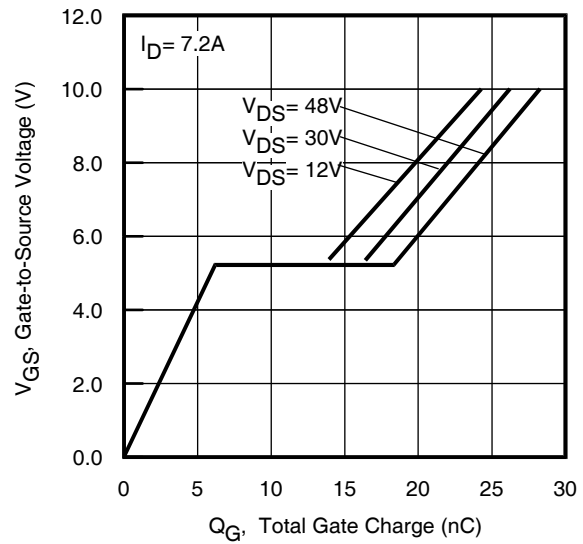


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

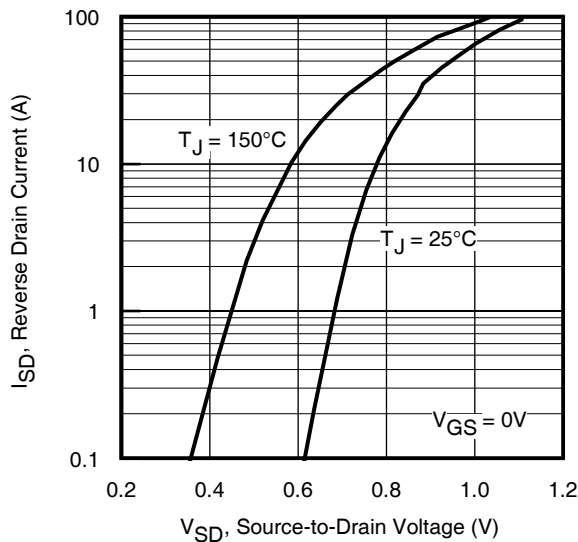


Fig 7. Typical Source-Drain Diode Forward Voltage

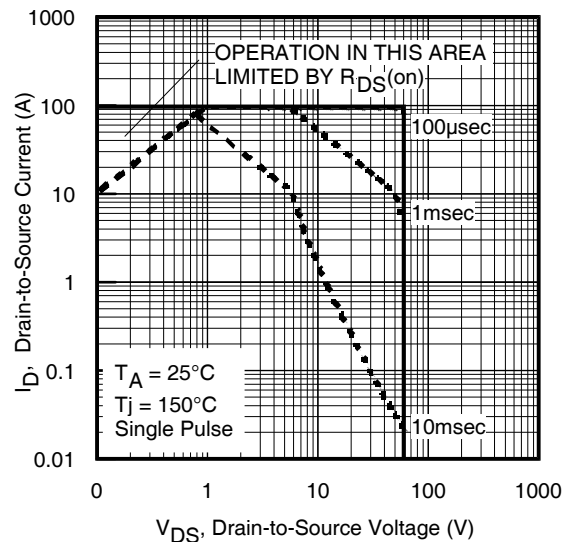


Fig 8. Maximum Safe Operating Area

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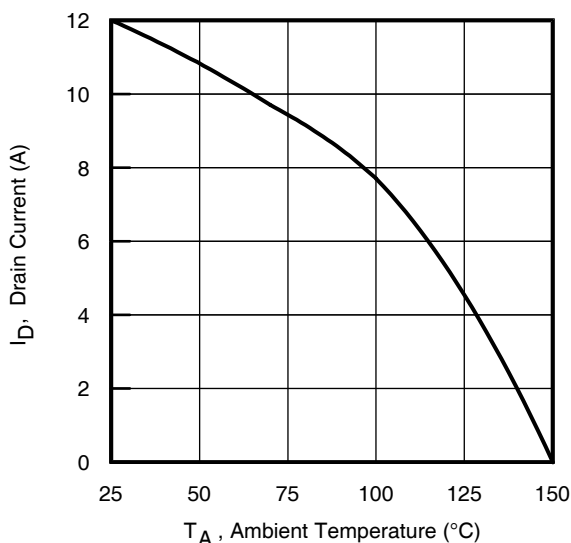


Fig 9. Maximum Drain Current vs. Ambient Temperature

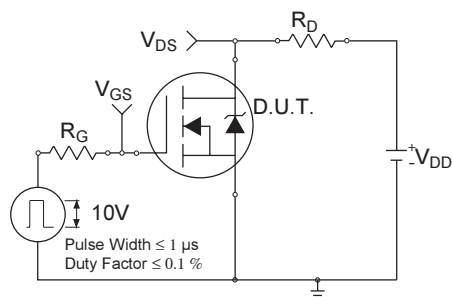


Fig 10a. Switching Time Test Circuit

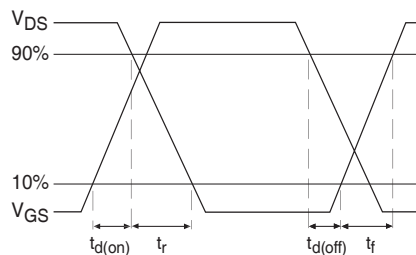


Fig 10b. Switching Time Waveforms

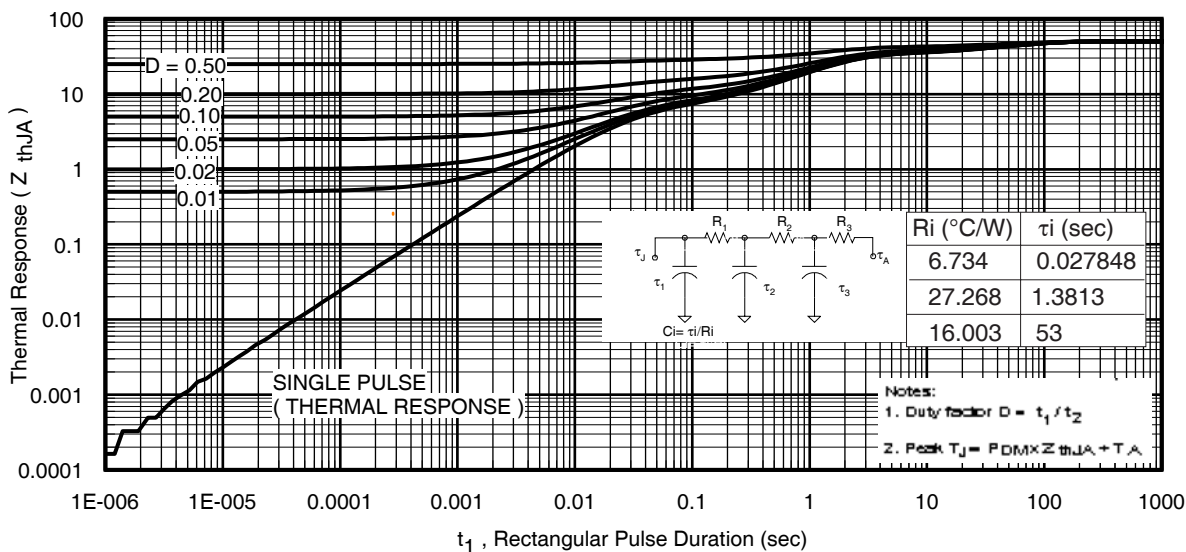


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

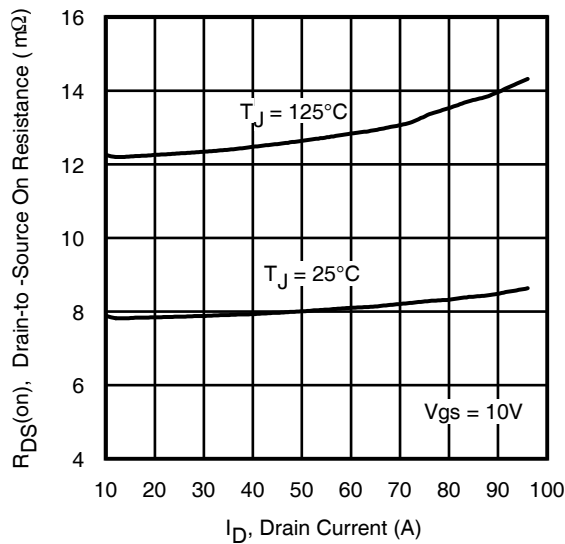


Fig 12. On-Resistance vs. Drain Current

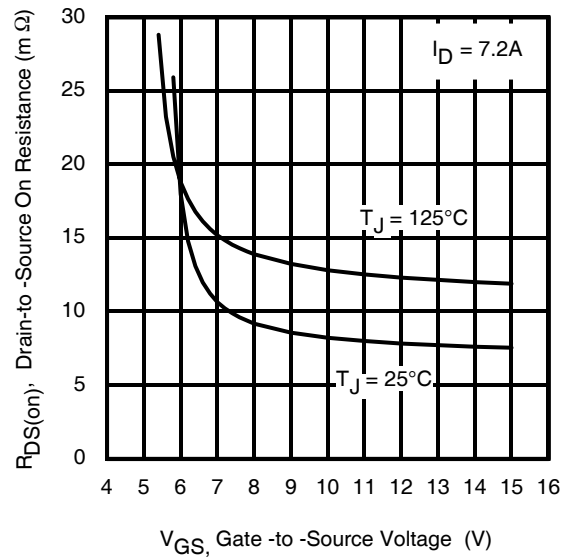


Fig 13. On-Resistance vs. Gate Voltage

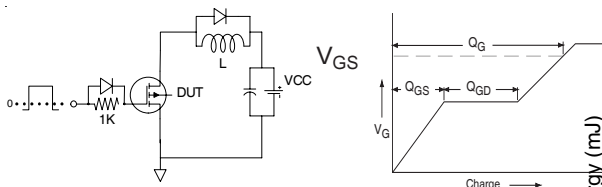


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

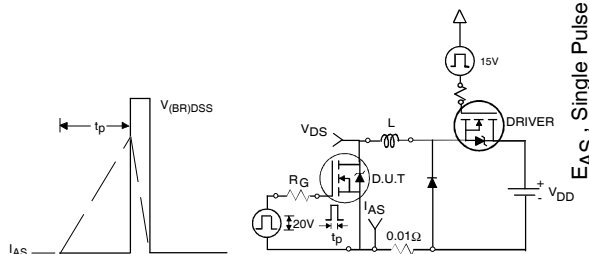


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

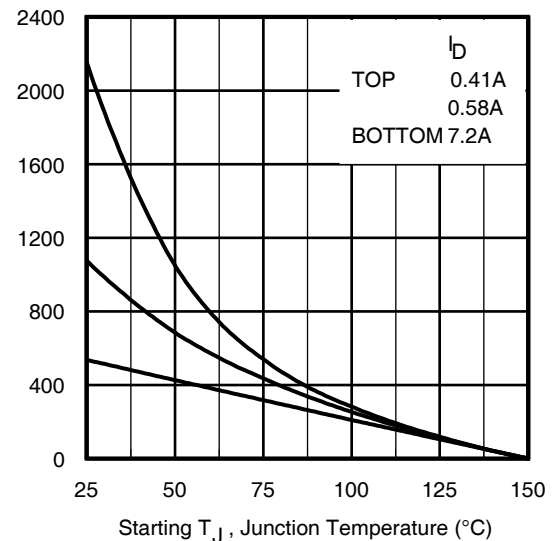
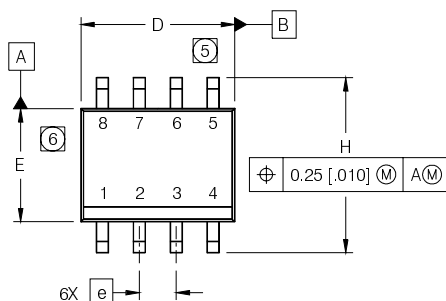
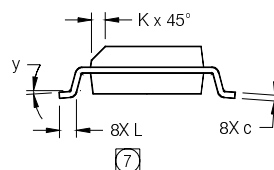
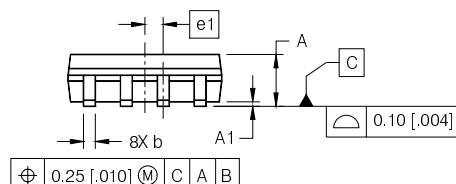


Fig 15c. Maximum Avalanche Energy vs. Drain Current

SO-8 Package Details



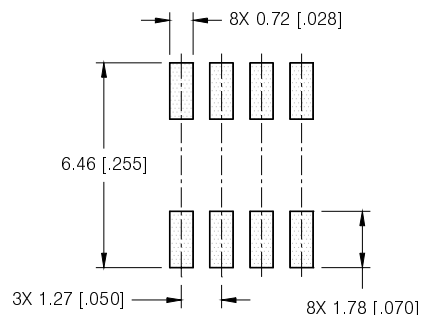
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

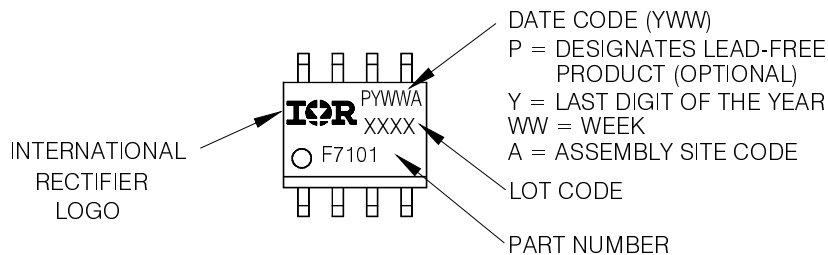
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking

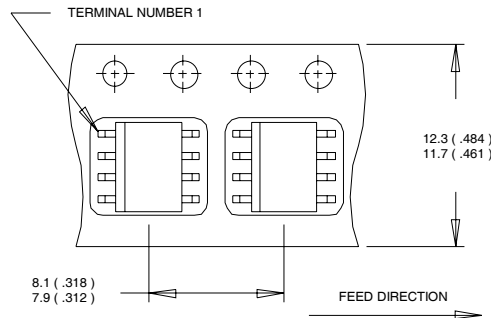
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



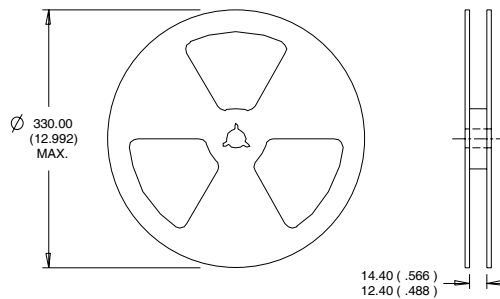
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SO-8 Tape and Reel



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 21\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 7.2\text{A}$.
- ③ When mounted on 1 inch square copper board, $t \leq 10$ sec.
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $I_{SD} \leq 7.2\text{A}$, $di/dt \leq 650\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.
- ⑦ R_{θ} is measured at T_J of approximately 90°C .

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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