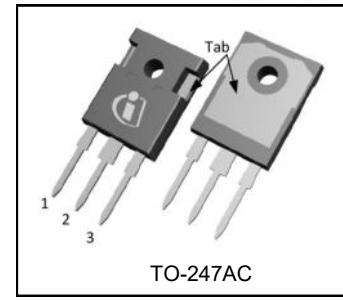
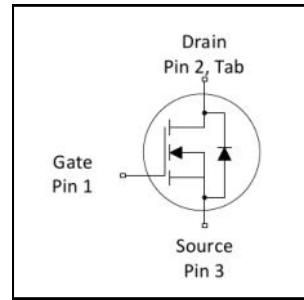


$V_{(BR)DSS}$	55V
$R_{DS(on)}$ max.	5.3m Ω
I_D	95A



Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free

Description

This HEXFET Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP1405PbF	TO-247AC	Tube	25	IRFP1405PbF

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	160	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	110	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	95	
I_{DM}	Pulsed Drain Current ①	640	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	310	W
	Linear Derating Factor	2.0	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	530	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy ⑥	1060	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	300	
		10 lbf·in (1.1N·m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case *	—	0.49	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient *	—	40	

* R_{θ} is measured at T_J approximately 90°C

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.058	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	4.2	5.3	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}, I_D = 95\text{A}$ ③
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$
g_{fs}	Forward Trans conductance	77	—	—	S	$V_{\text{DS}} = 25\text{V}, I_D = 95\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{\text{DS}} = 55\text{V}, V_{\text{GS}} = 0\text{V}$
				250		$V_{\text{DS}} = 55\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 20\text{V}$
				-200		$V_{\text{GS}} = -20\text{V}$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Q_g	Total Gate Charge	—	120	180	nC	$I_D = 95\text{A}$ $V_{\text{DS}} = 44\text{V}$ $V_{\text{GS}} = 10\text{V}$ ③
Q_{gs}	Gate-to-Source Charge	—	30	—		
Q_{gd}	Gate-to-Drain Charge	—	53	—		
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	12	—		
t_r	Rise Time	—	160	—	ns	$V_{\text{DD}} = 28\text{V}$ $I_D = 95\text{A}$ $R_G = 2.6\Omega$ $V_{\text{GS}} = 10\text{V}$ ③
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	140	—		
t_f	Fall Time	—	150	—		
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	5600	—	pF	$V_{\text{GS}} = 0\text{V}$ $V_{\text{DS}} = 25\text{V}$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	1310	—		
C_{rss}	Reverse Transfer Capacitance	—	350	—		
C_{oss}	Output Capacitance	—	6550	—	pF	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 1.0\text{V}, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	920	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 44\text{V}, f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	1750	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V to } 44\text{V}$ ④

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	95	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	640		
V_{SD}	Diode Forward Voltage	—	—	1.3		$T_J = 25^\circ\text{C}, I_S = 95\text{A}, V_{\text{GS}} = 0\text{V}$ ③
t_{rr}	Reverse Recovery Time	—	70	110	ns	$T_J = 25^\circ\text{C}, I_F = 95\text{A}, V_{\text{DD}} = 28\text{V}$
Q_{rr}	Reverse Recovery Charge	—	170	260		
					μC	$dI/dt = 100\text{A}/\mu\text{s}$ ③

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.12\text{mH}$, $R_G = 25\Omega$, $I_{\text{AS}} = 95\text{A}$, $V_{\text{GS}} = 10\text{V}$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{\text{oss eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.

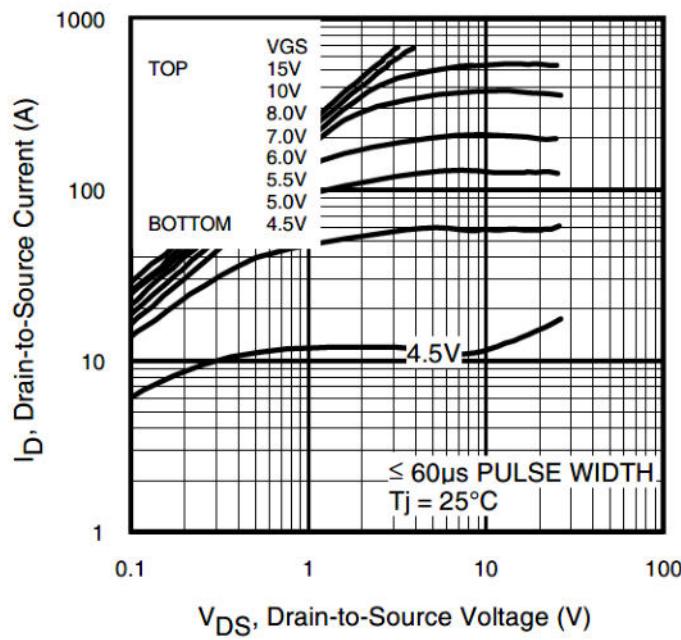


Fig. 1 Typical Output Characteristics

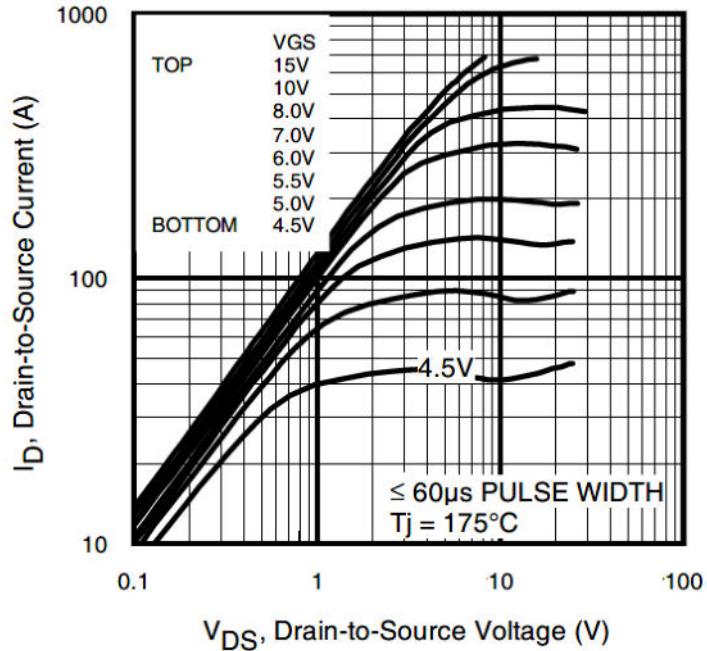


Fig. 2 Typical Output Characteristics

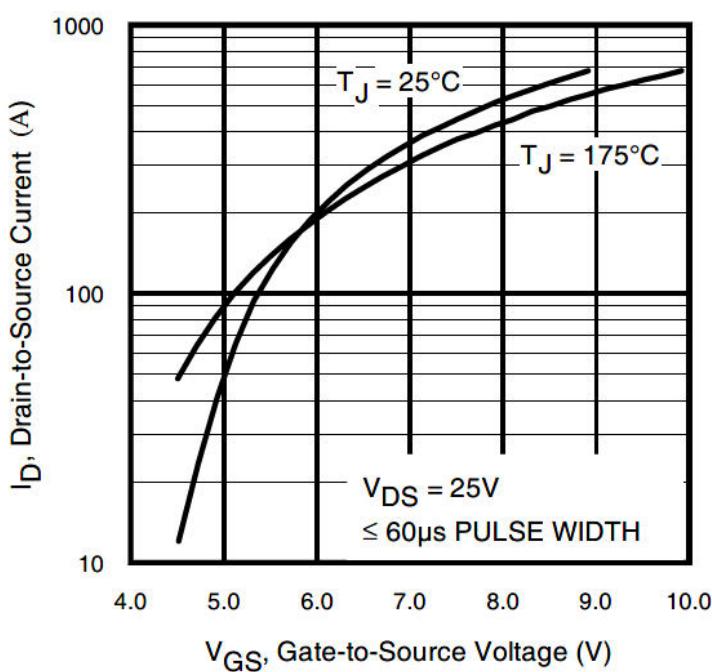


Fig. 3 Typical Transfer Characteristics

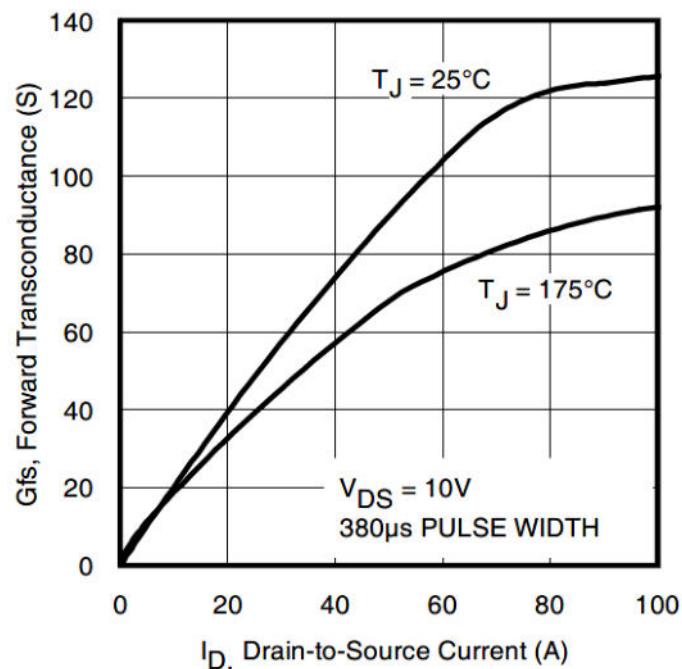


Fig. 4 Typical Forward Transconductance Vs. Drain Current

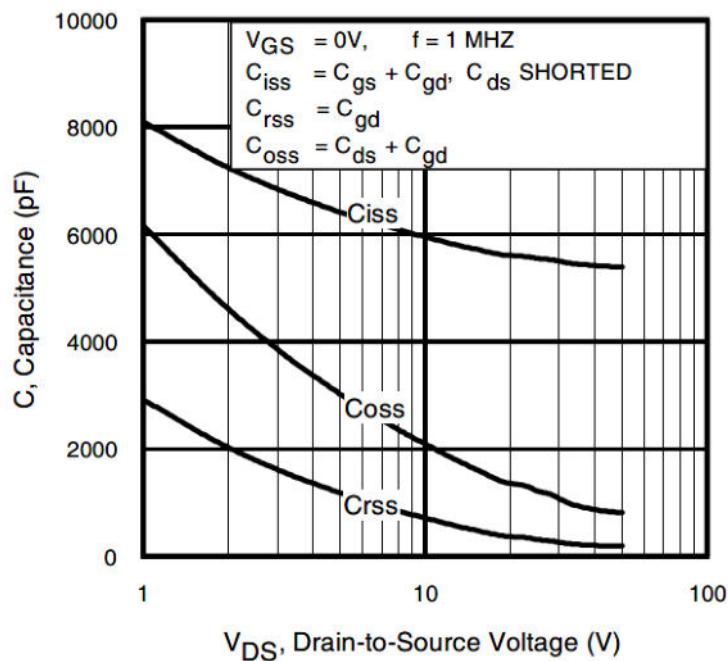


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

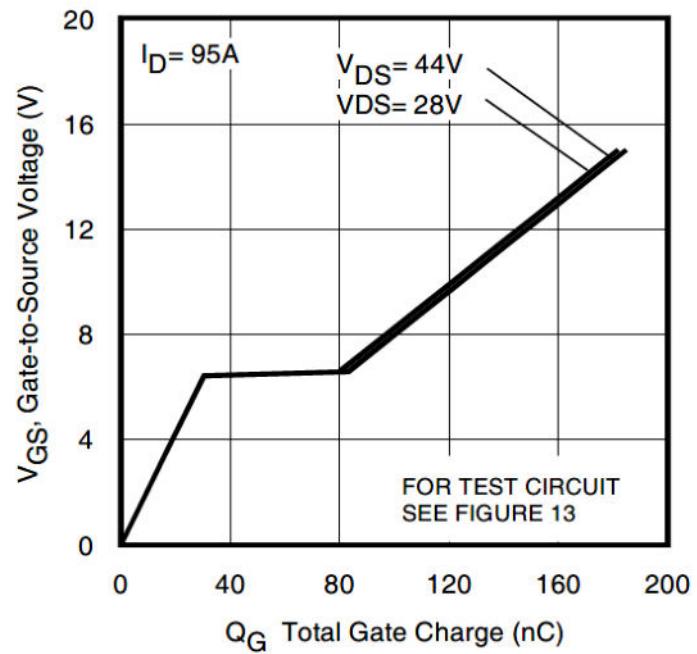


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

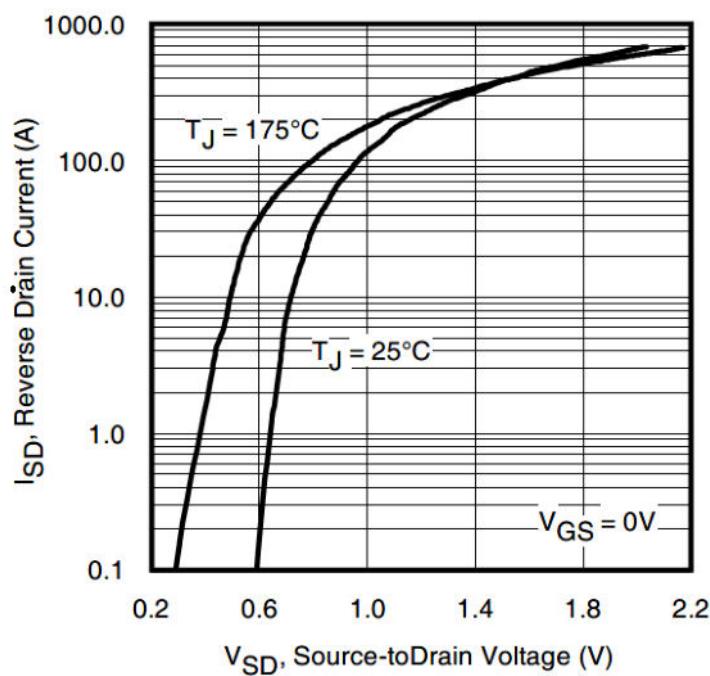


Fig 7 Typical Source-to-Drain Diode
Forward Voltage

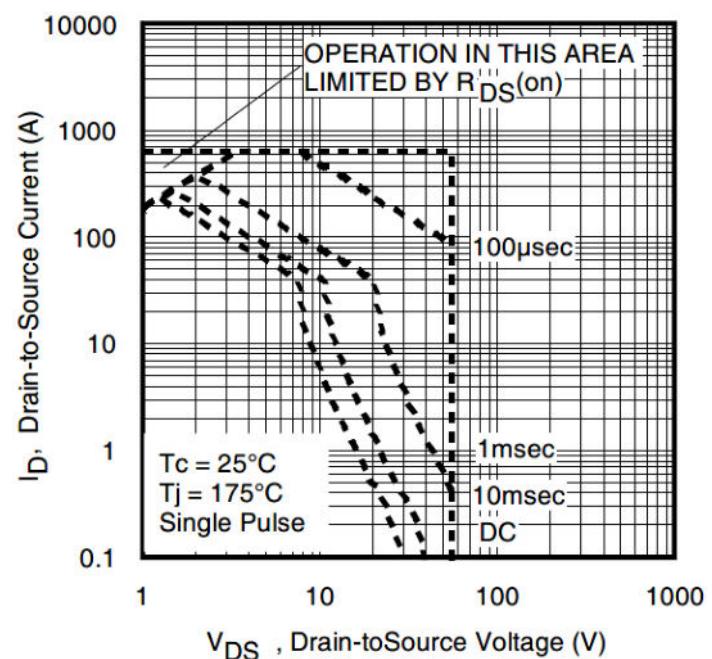


Fig 8. Maximum Safe Operating Area

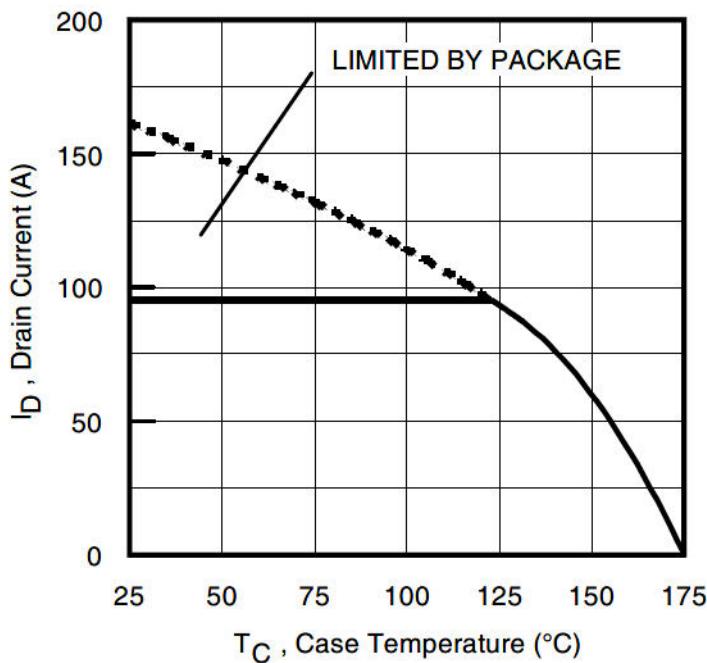


Fig 9. Maximum Drain Current vs. Case Temperature

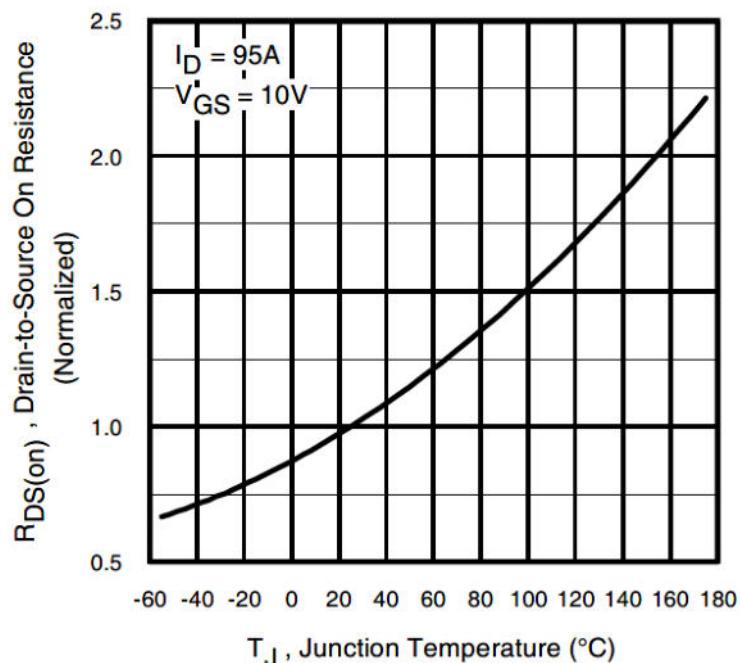


Fig 10. Normalized On-Resistance vs. Temperature

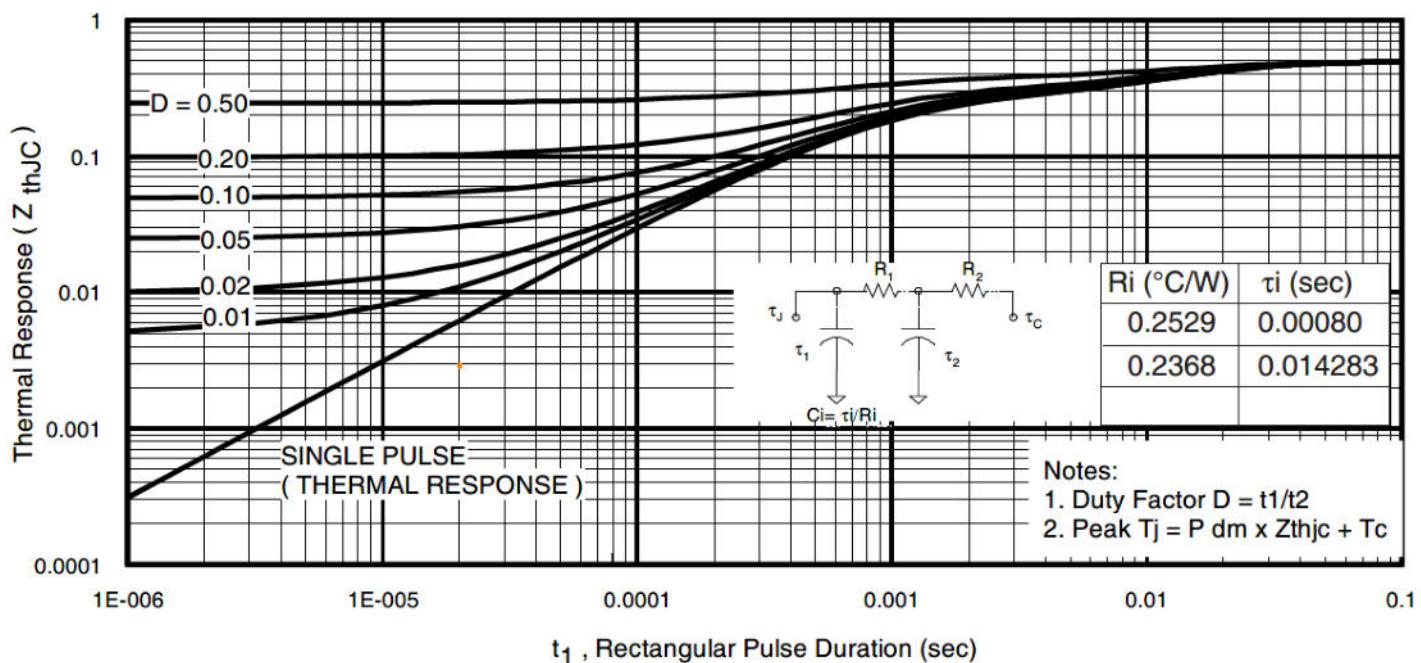


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

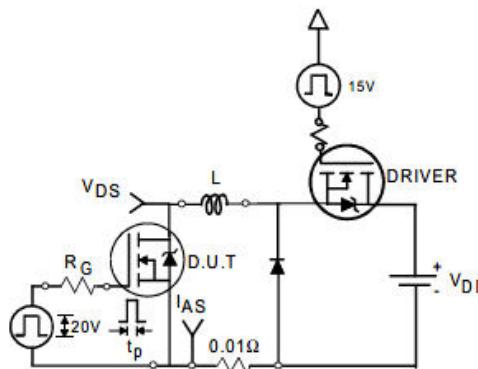


Fig. 12a. Unclamped Inductive Test Circuit

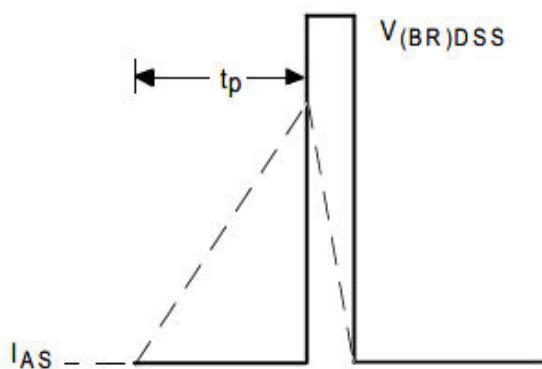


Fig. 12b. Unclamped Inductive Waveforms

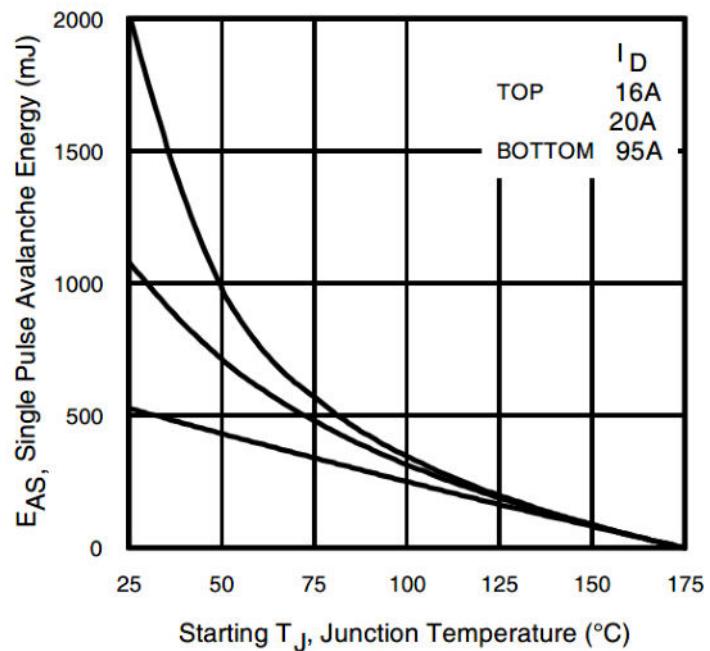


Fig 12c. Maximum Avalanche Energy vs. Drain Current

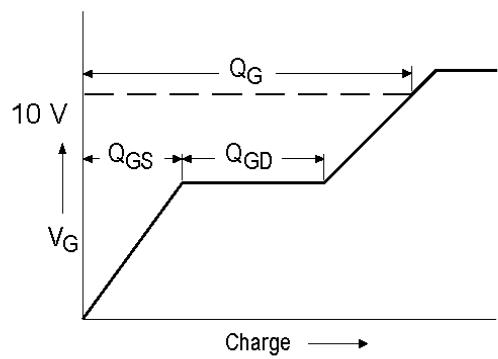


Fig 13a. Basic Gate Charge Waveform

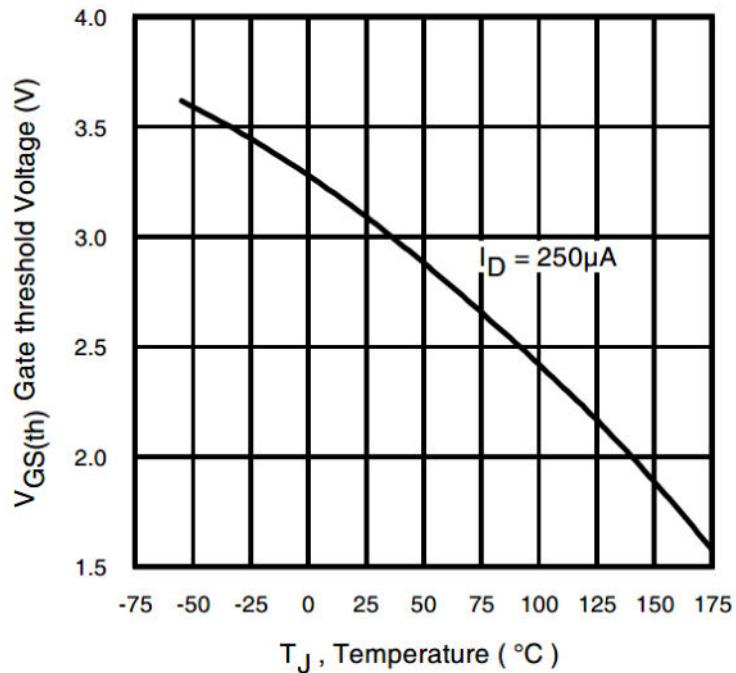


Fig 14. Threshold Voltage Vs. Temperature

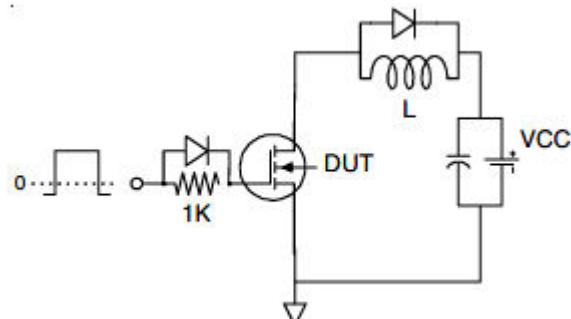


Fig 13b. Gate Charge Test Circuit

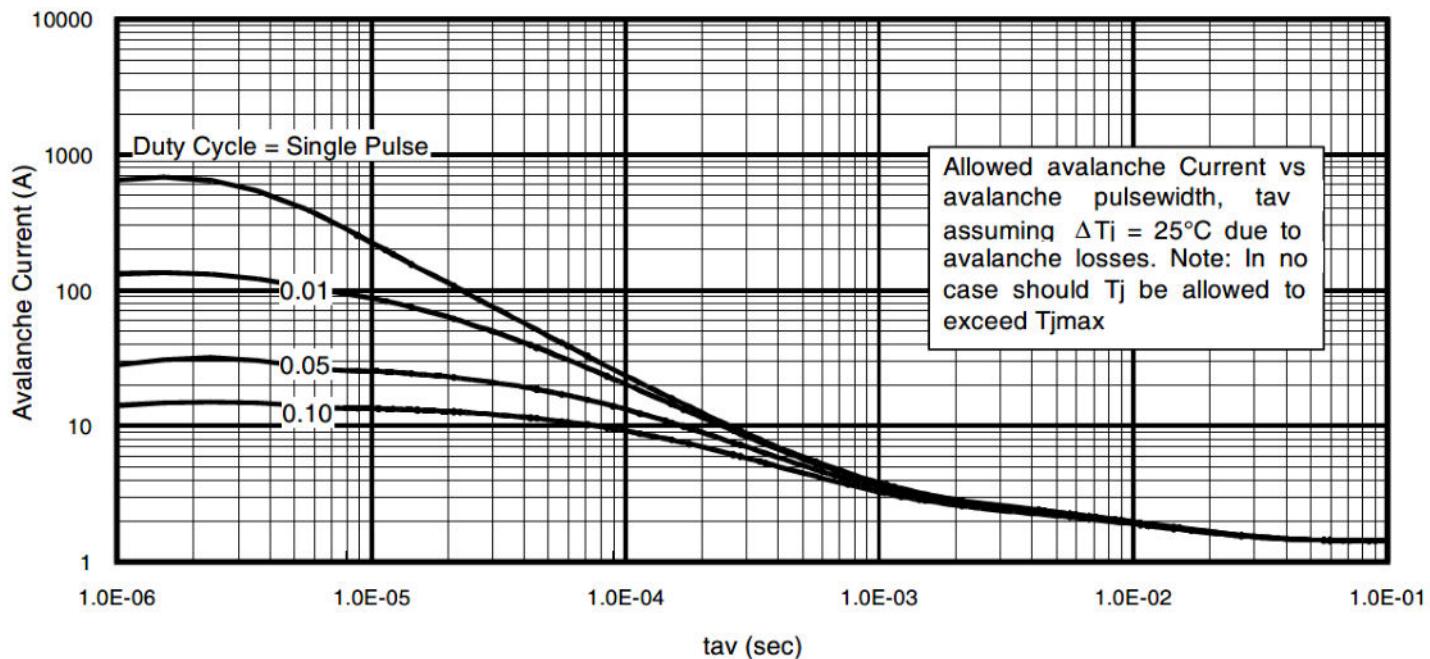
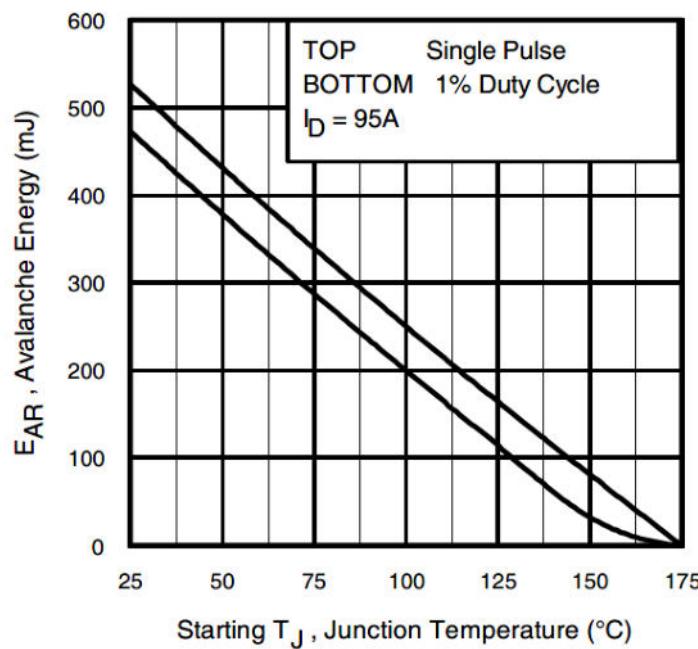


Fig. 15. Typical Avalanche Current Vs.Pulsewidth



Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).

t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{th,JC}(D, t_{av})$ = Transient thermal resistance, see Figures 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{th,JC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 16. Maximum Avalanche Energy vs. Temperature

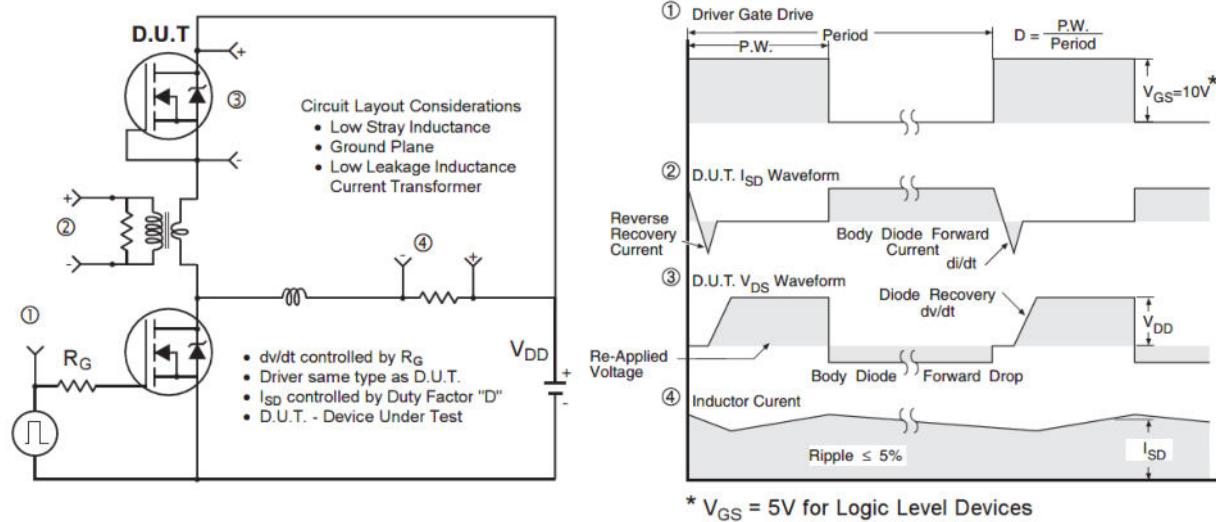


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

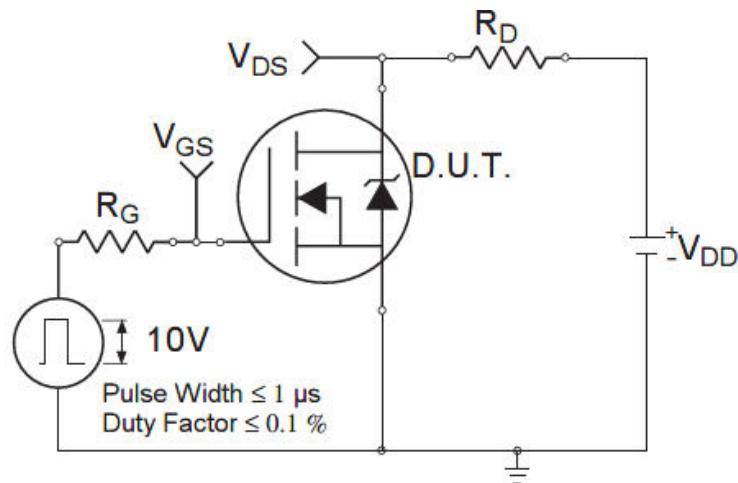


Fig 18a. Switching Time Test Circuit

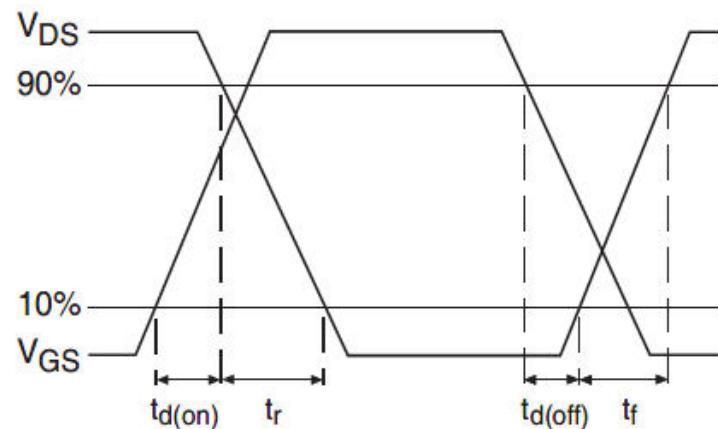
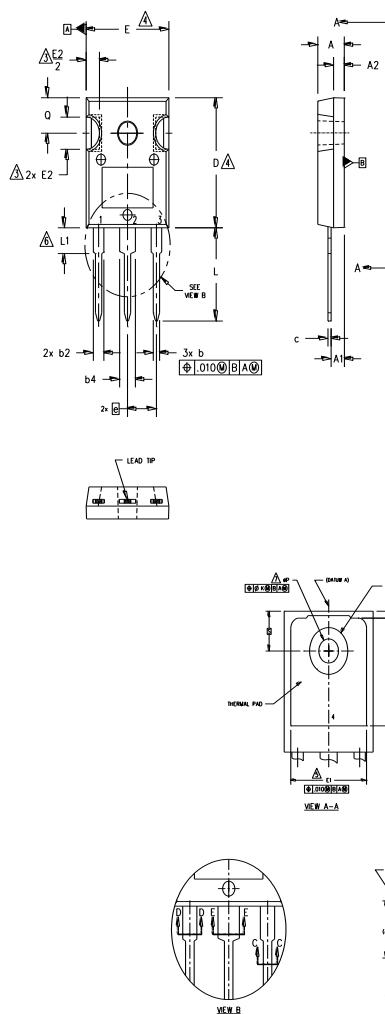


Fig 18b. Switching Time Waveforms

TO-247AC Package Outline (Dimensions are



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. OP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES	
	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.		
A	.183	.209	4.65	5.31		
A1	.087	.102	2.21	2.59		
A2	.059	.098	1.50	2.49		
b	.039	.055	0.99	1.40		
b1	.039	.053	0.99	1.35		
b2	.065	.094	1.65	2.39		
b3	.065	.092	1.65	2.34		
b4	.102	.135	2.59	3.43		
b5	.102	.133	2.59	3.38		
c	.015	.035	0.38	0.89		
c1	.015	.033	0.38	0.84		
D	.776	.815	19.71	20.70	4	
D1	.515	—	13.08	—	5	
D2	.020	.053	0.51	1.35		
E	.602	.625	15.29	15.87	4	
E1	.530	—	13.46	—		
E2	.178	.216	4.52	5.49		
e	.215 BSC		5.46 BSC			
Øk	.010		0.25			
L	.559	.634	14.20	16.10		
L1	.146	.169	3.71	4.29		
OP	.140	.144	3.56	3.66		
ØP1	—	.291	—	7.39		
Q	.209	.224	5.31	5.69		
S	.217 BSC		5.51 BSC			

LEAD ASSIGNMENTSHEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

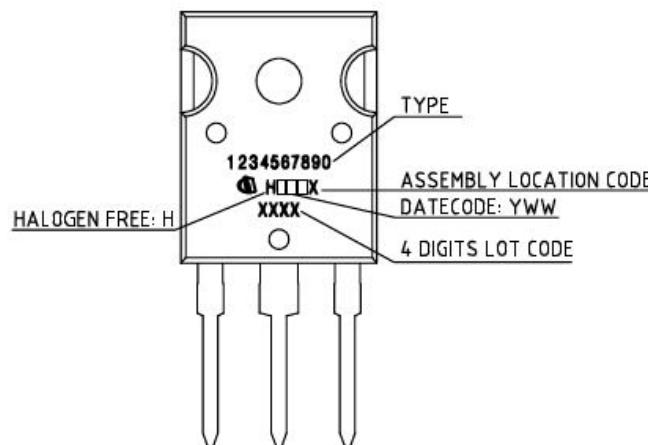
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- Emitter
- 4.- COLLECTOR

DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information



TO-247AC package is not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
2024-10-09	2.1	<ul style="list-style-type: none"> Update datasheet to Infineon format Updated Part marking –page 9 Added disclaimer on last page.

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: erratum@infineon.com

Published by

Infineon Technologies AG
81726 München, Germany

© 2024 Infineon Technologies AG

All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”).

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

The Infineon Technologies component described in this Data Sheet may be used in life support devices or systems and or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.