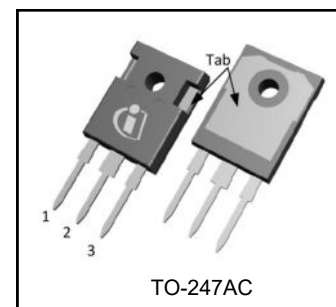
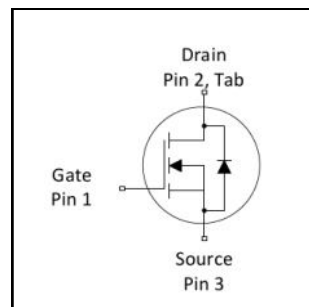


V_{DSS}	100V
$R_{DS(on)}$ typ.	3.7mΩ
max.	4.5mΩ
I_D (Silicon Limited)	180A^①
I_D (Package Limited)	120A



Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP4110PbF	TO-247	Tube	25	IRFP4110PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	180 ^①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	130 ^①	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	120	
I_{DM}	Pulsed Drain Current ^②	670	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ^④	5.3	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf.in (1.1N.m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^③	190	mJ
I_{AR}	Avalanche Current ^②	108	A
E_{AR}	Repetitive Avalanche Energy ^⑤	37	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^⑧	—	0.402	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ^⑨	—	40	

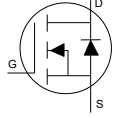
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.108	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5\text{mA}$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.7	4.5	m Ω	$V_{GS} = 10\text{V}$, $I_D = 75\text{A}$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	160	—	—	S	$V_{DS} = 50\text{V}$, $I_D = 75\text{A}$
Q_g	Total Gate Charge	—	150	210	nC	$I_D = 75\text{A}$
Q_{gs}	Gate-to-Source Charge	—	35	—		$V_{DS} = 50\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	43	—		$V_{GS} = 10\text{V}$ ⑤
R_G	Gate Resistance	—	1.3	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	$V_{DD} = 65\text{V}$
t_r	Rise Time	—	67	—		$I_D = 75\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	78	—		$R_G = 2.6\Omega$
t_f	Fall Time	—	88	—		$V_{GS} = 10\text{V}$ ⑤
C_{iss}	Input Capacitance	—	9620	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output Capacitance	—	670	—		$V_{DS} = 50\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	250	—		$f = 1.0\text{MHz}$, See Fig. 5
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related) ⑦	—	820	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 80V ⑦
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related) ⑥	—	950	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 80V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	170 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	670		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 75\text{A}$, $V_{GS} = 0\text{V}$ ⑤
t_{rr}	Reverse Recovery Time	—	50	75	ns	$T_J = 25^\circ\text{C}$
		—	60	90		$T_J = 125^\circ\text{C}$
Q_{rr}	Reverse Recovery Charge	—	94	140	nC	$T_J = 25^\circ\text{C}$
		—	140	210		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	3.5	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. Junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.033\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 108\text{A}$, $V_{GS} = 10\text{V}$. Part not Recommended for use above this value.
- ④ $I_{SD} \leq 75\text{A}$, $di/dt \leq 630\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss\text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ R_θ is measured at T_J approximately 90°C .
- ⑨ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-0994

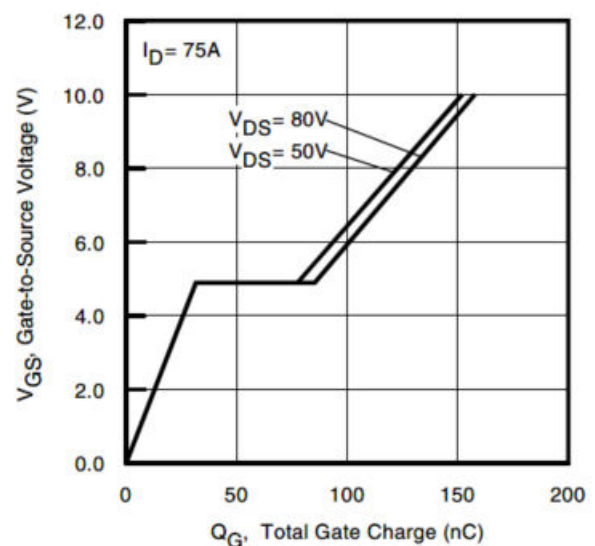
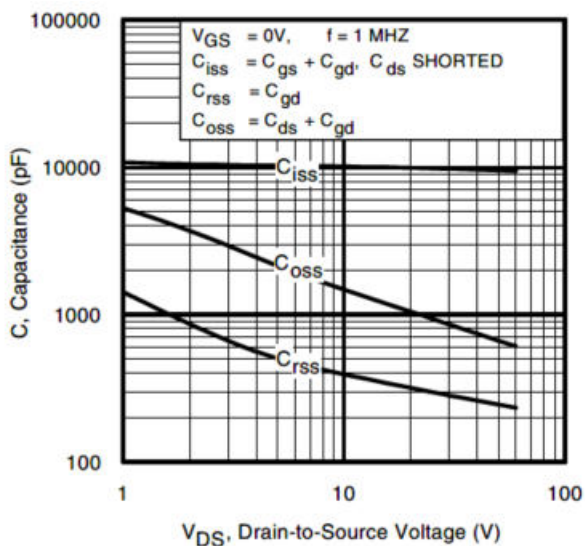
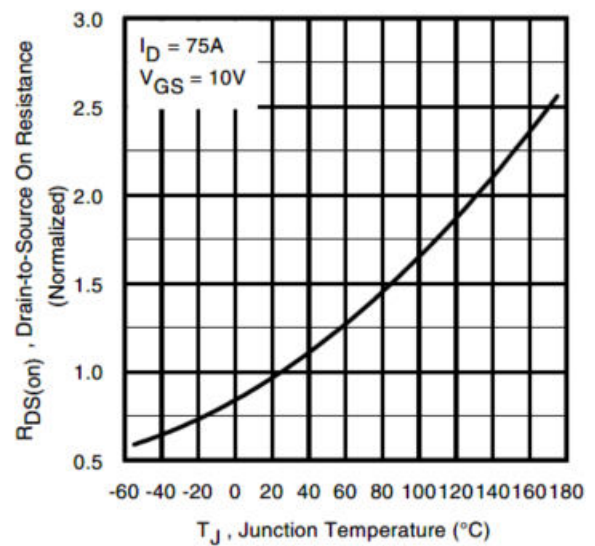
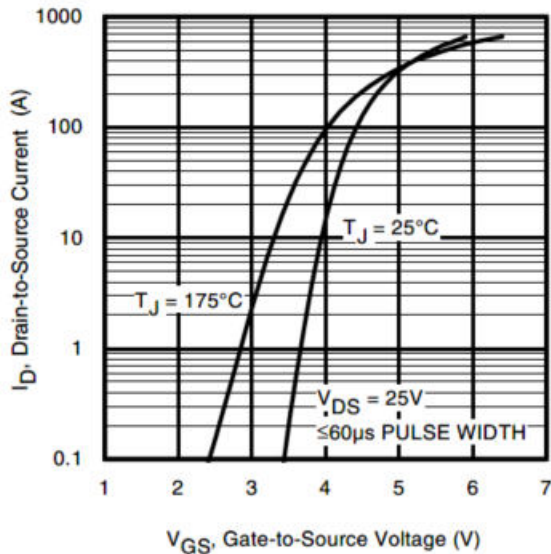
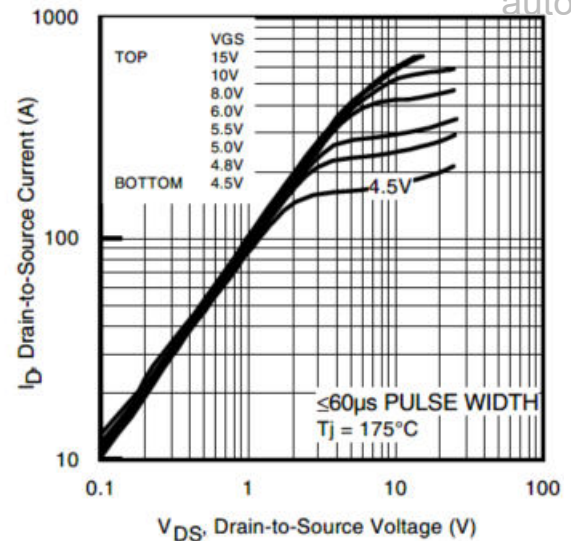
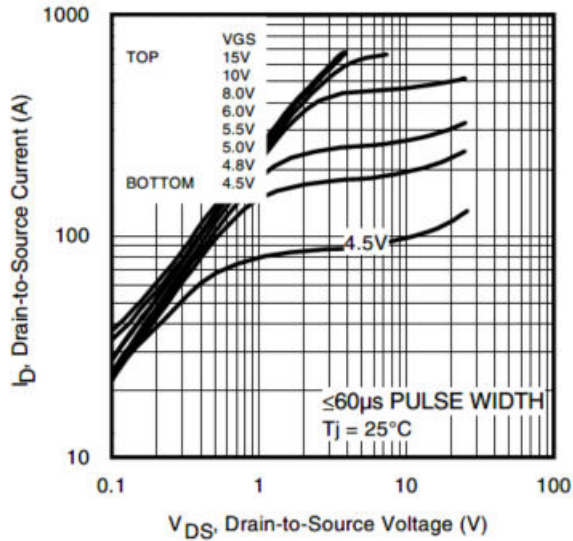


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

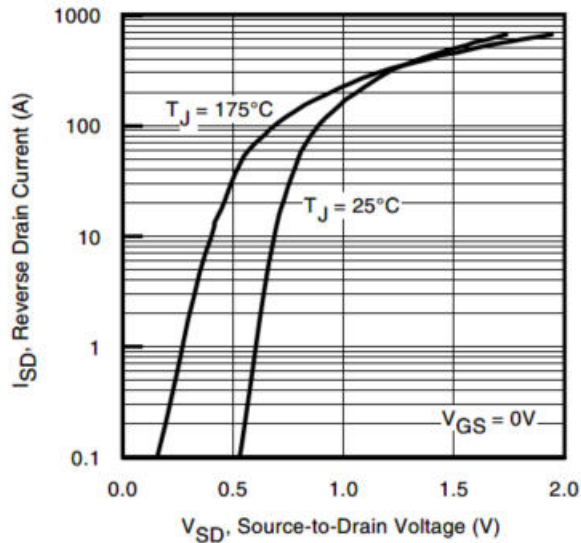


Fig 7. Typical Source-to-Drain Diode Forward Voltage

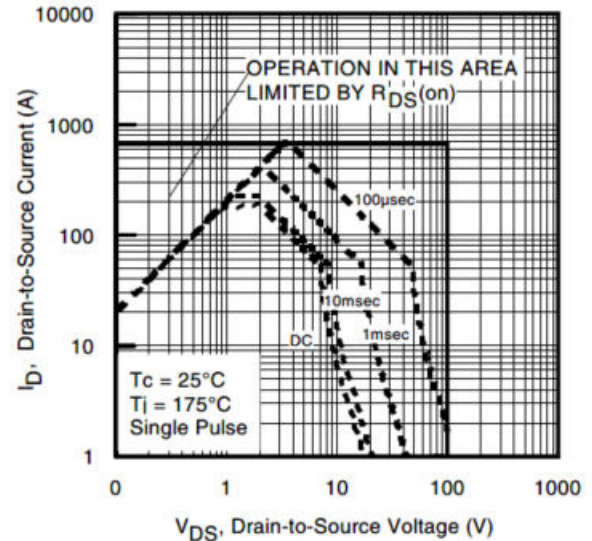


Fig 8. Maximum Safe Operating Area

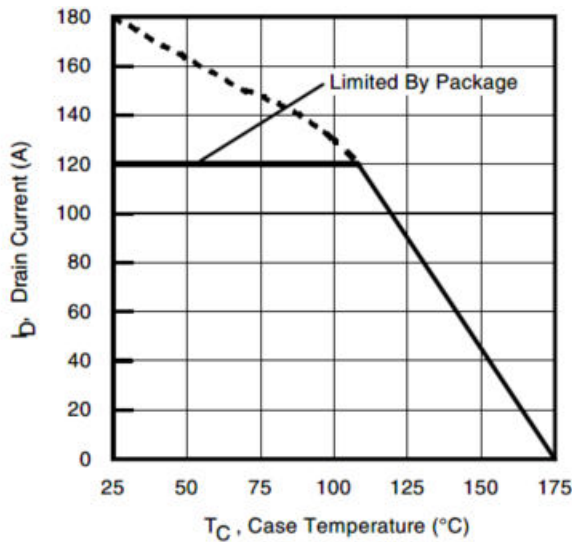


Fig 9. Maximum Drain Current vs. Case Temperature

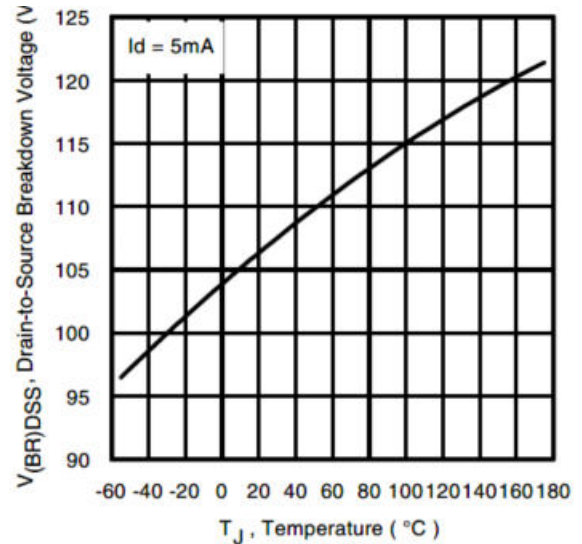


Fig 10. Drain-to-Source Breakdown Voltage

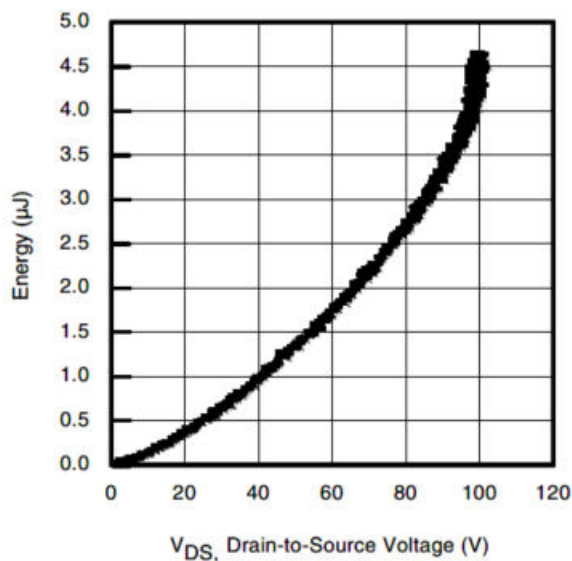


Fig 11. Typical Coss Stored Energy

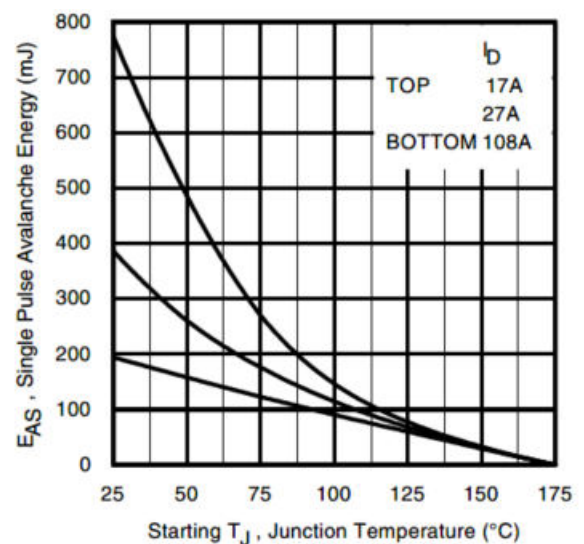


Fig 12. Maximum Avalanche Energy vs. Drain Current

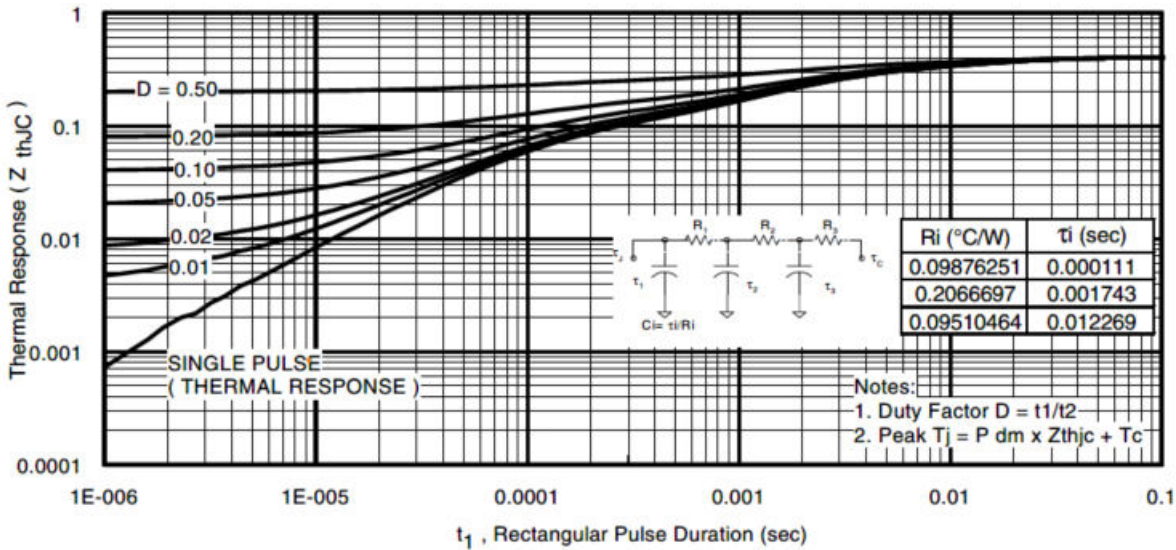


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

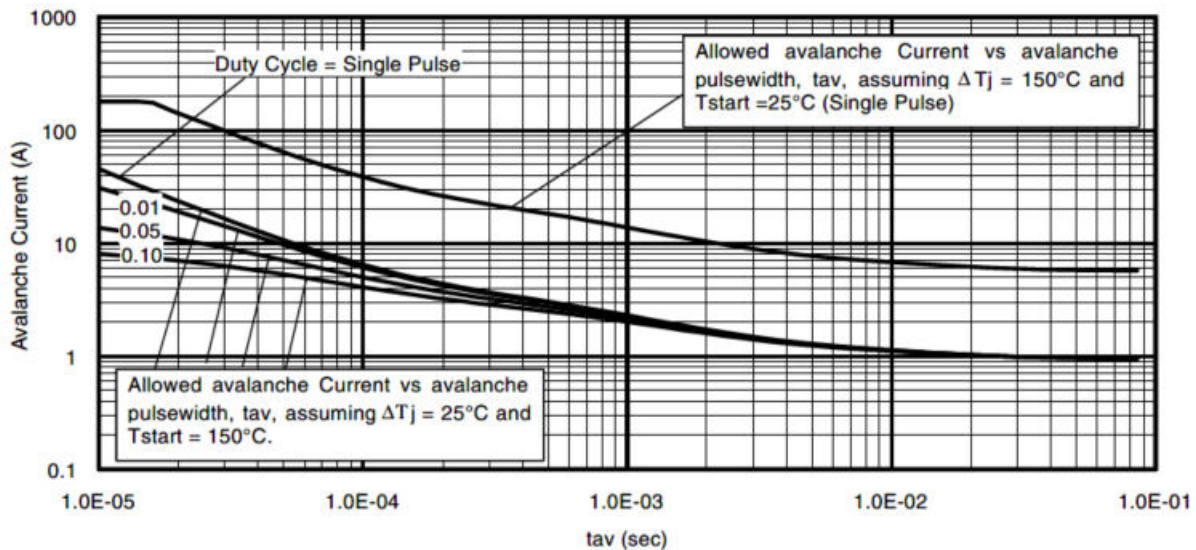
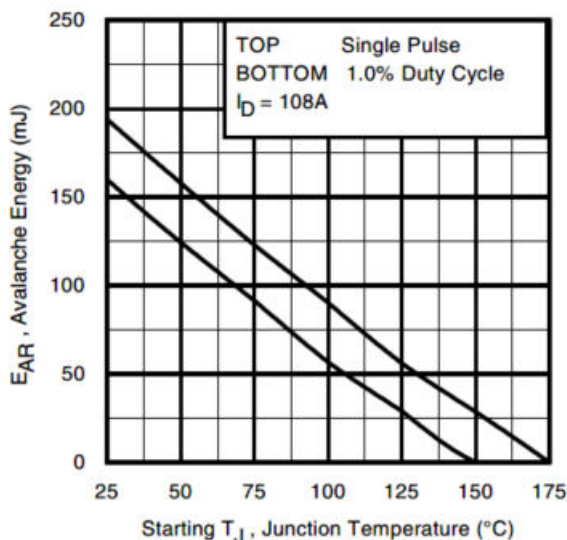


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

- Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
- Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
- Equation below based on circuit and waveforms shown in Figures 16a, 16b.
- $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- I_{av} = Allowable avalanche current.
- ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

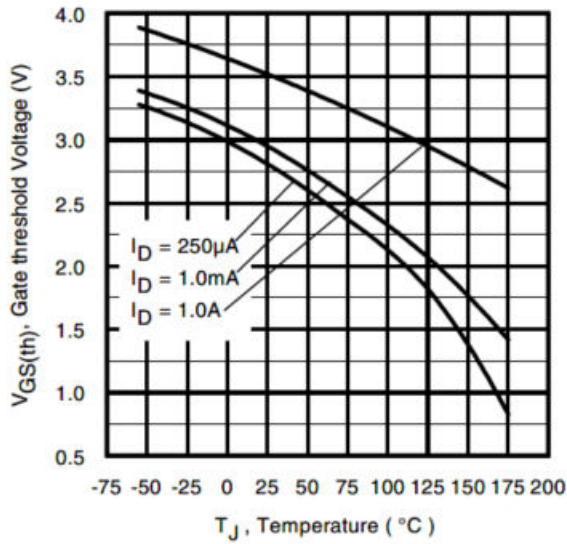
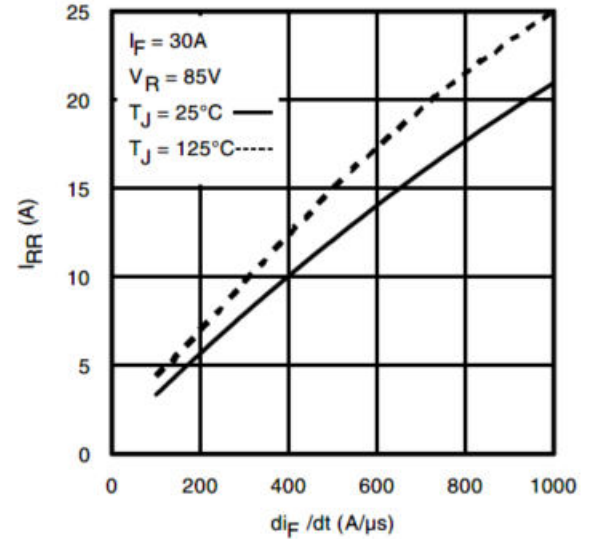
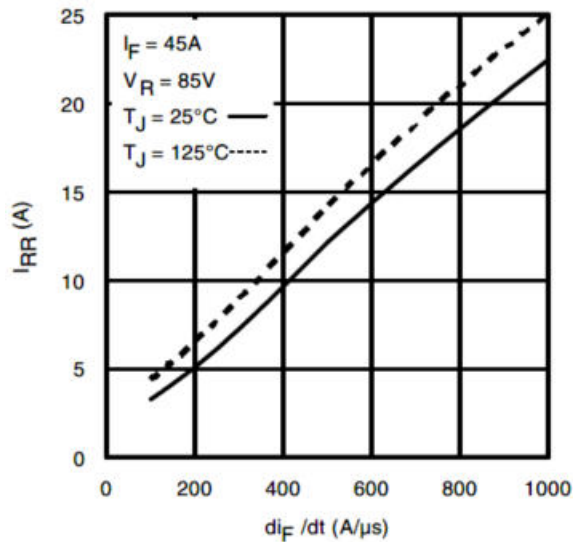
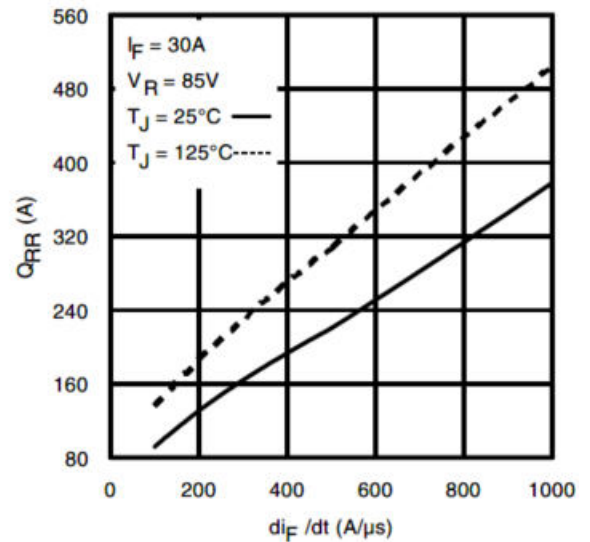
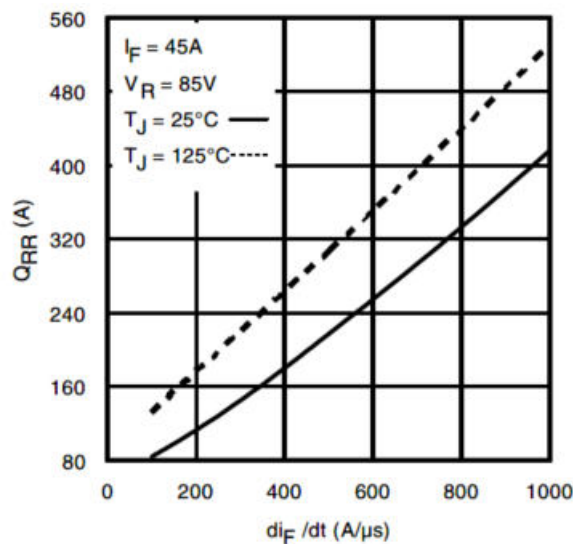


Fig. 16 Threshold Voltage vs. Temperature

Fig. 17 Typical Recovery Current vs. di_F/dt Fig 18. Typical Recovery Current vs. di_F/dt Fig 19. Typical Stored Charge vs. di_F/dt Fig 20. Typical Stored Charge vs. di_F/dt

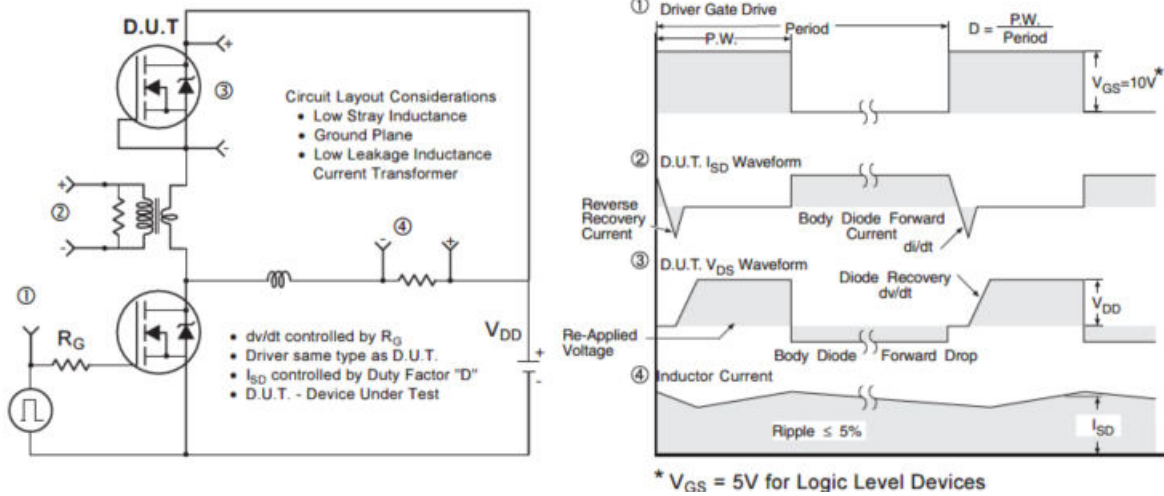


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

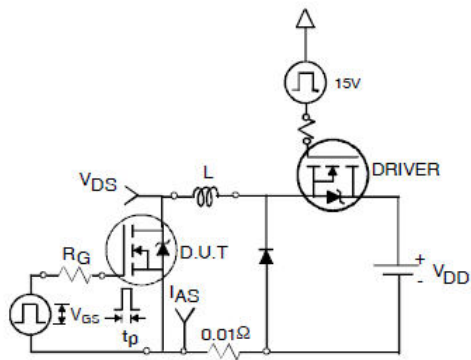


Fig 22a. Unclamped Inductive Test Circuit

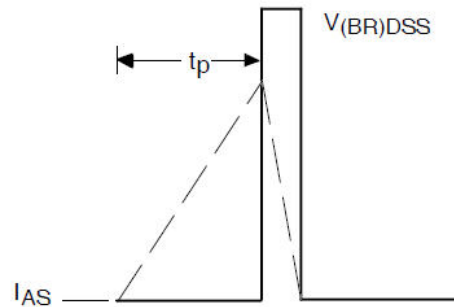


Fig 22b. Unclamped Inductive Waveforms

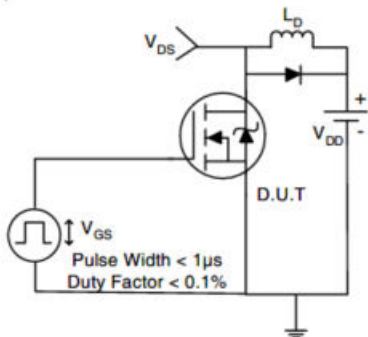


Fig 23a. Switching Time Test Circuit

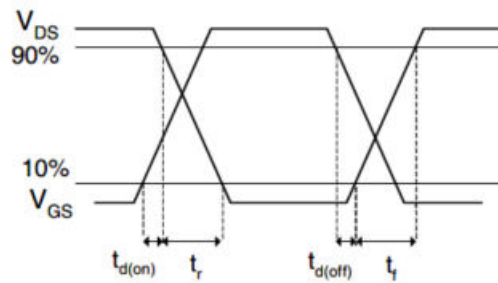


Fig 23b. Switching Time Waveforms

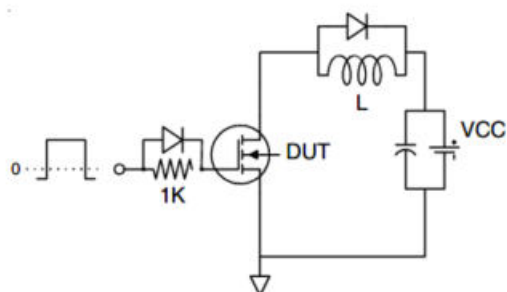


Fig 24a. Gate Charge Test Circuit

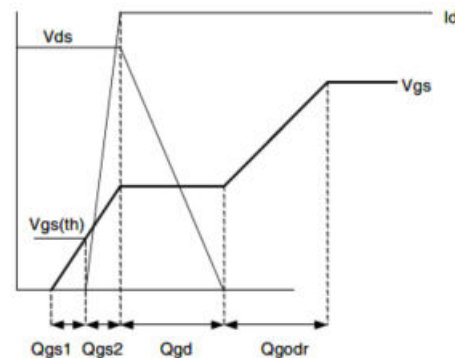


Fig 24b. Gate Charge Waveform

Revision History

Date	Rev.	Comments
2013-09-06	2.0	Final data sheet
2024-12-04	2.1	- Update datasheet to Infineon format - Updated Part marking –page 8 - Added disclaimer on last page.

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