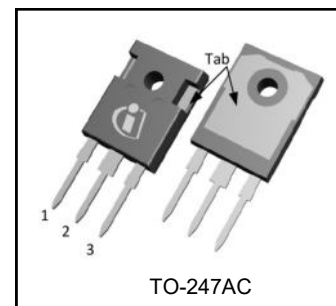
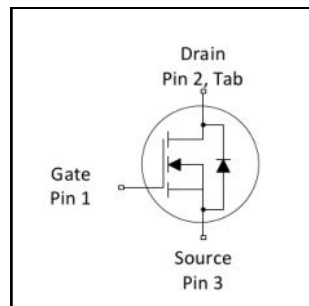


PDP SWITCH

Key Parameters		
V_{DS} max	250	V
V_{DS} (Avalanche) typ.	300	V
$R_{DS(ON)}$ typ. @ 10V	38	m Ω
I_{RP} max @ $T_C = 100^\circ\text{C}$	87	A
T_J max	175	$^\circ\text{C}$



Features

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low E_{PULSE} Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low Q_G for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 175°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

Description

This HEXFET[®] Power MOSFET is specifically designed for Sustain; Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low E_{PULSE} rating. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications

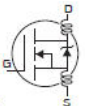
Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 30	V
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	44	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	31	
I_{DM}	Pulsed Drain Current ①	180	
I_{RP} @ $T_C = 100^\circ\text{C}$	Repetitive Peak Current ⑤	87	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	310	W
P_D @ $T_C = 100^\circ\text{C}$	Maximum Power Dissipation	150	
	Linear Derating Factor	2.0	W/ $^\circ\text{C}$
T_J	Operating Junction and	-40 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	0.49	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ④	—	40	

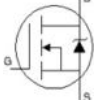
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	250	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	210	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	38	46	$m\Omega$	$V_{GS} = 10V, I_D = 26A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	—	-14	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 250V, V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = 250V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Trans conductance	83	—	—	S	$V_{DS} = 25V, I_D = 26A$
Q_g	Total Gate Charge	—	72	110	nC	$I_D = 26A, V_{DS} = 125V$ ③
Q_{gd}	Gate-to-Drain Charge	—	26	—		$V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	$V_{DD} = 125V, V_{GS} = 10V$ ③
t_r	Rise Time	—	27	—		$I_D = 26A$
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		$R_G = 5.0\Omega$
t_f	Fall Time	—	19	—		See Fig. 22
t_{st}	Shoot Through Blocking Time	100	—	—	ns	$V_{DD} = 200V, V_{GS} = 15V, R_G = 4.7\Omega$
E_{PULSE}	Energy per Pulse	—	790	—	μJ	$L = 220nH, C = 0.3\mu F, V_{GS} = 15V$ $V_{DD} = 200V, R_G = 4.7\Omega, T_J = 25^\circ\text{C}$
		—	1390	—		$L = 220nH, C = 0.3\mu F, V_{GS} = 15V$ $V_{DD} = 200V, R_G = 4.7\Omega, T_J = 100^\circ\text{C}$
C_{iss}	Input Capacitance	—	4560	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	390	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	100	—		$f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	290	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 200V$
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact : 
L_S	Internal Source Inductance	—	13	—		

Avalanche Characteristics

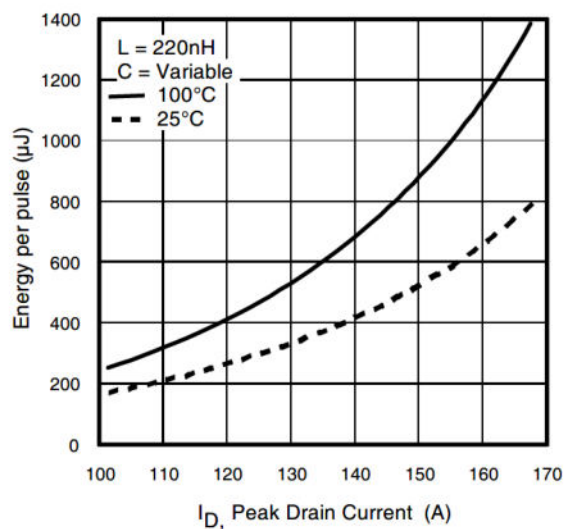
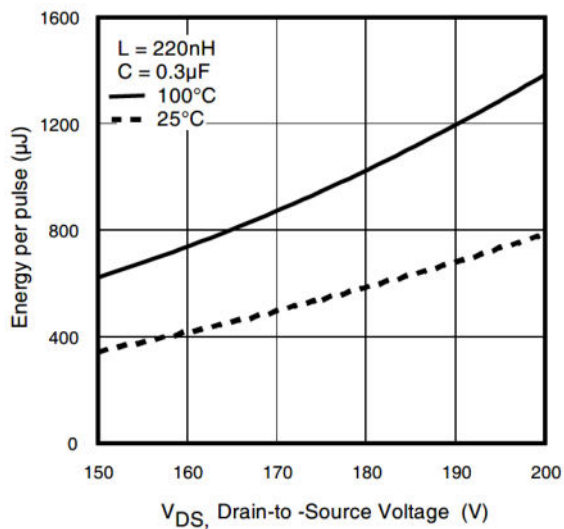
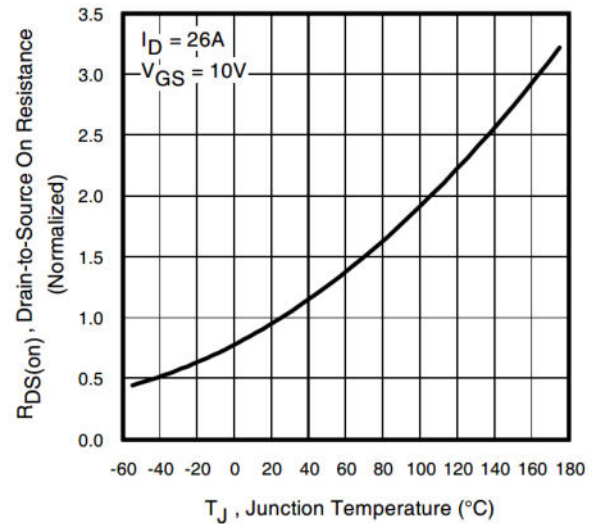
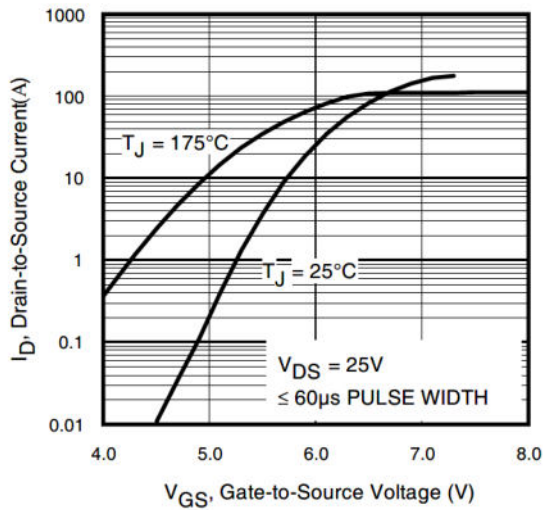
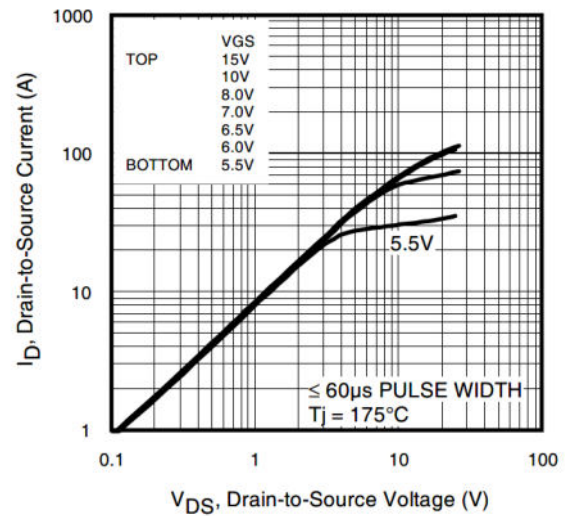
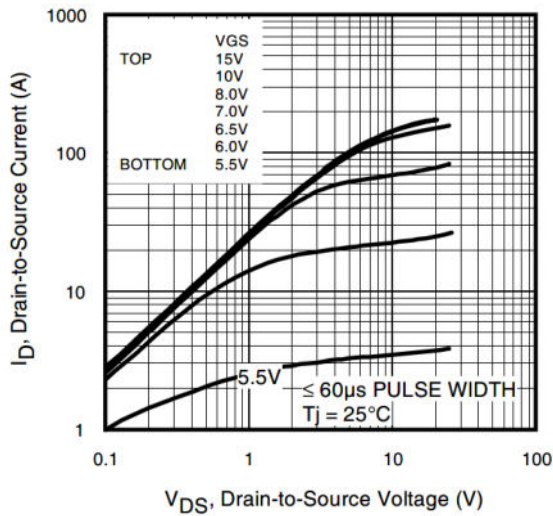
	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	300	mJ
E_{AR}	Repetitive Avalanche Energy ①	—	31	
$V_{DS(Avalanche)}$	Repetitive Avalanche Voltage ①	300	—	V
I_{AS}	Avalanche Current ②	—	26	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	44	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 26A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	190	290	ns	$T_J = 25^\circ\text{C}, I_F = 26A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge	—	840	1260	nC	$di/dt = 100A/\mu s$ ③

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② starting $T_J = 25^\circ\text{C}$, $L = 0.85\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 26A$.
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ Half sine wave with duty cycle = 0.25, $t_{on} = 1\mu s$.



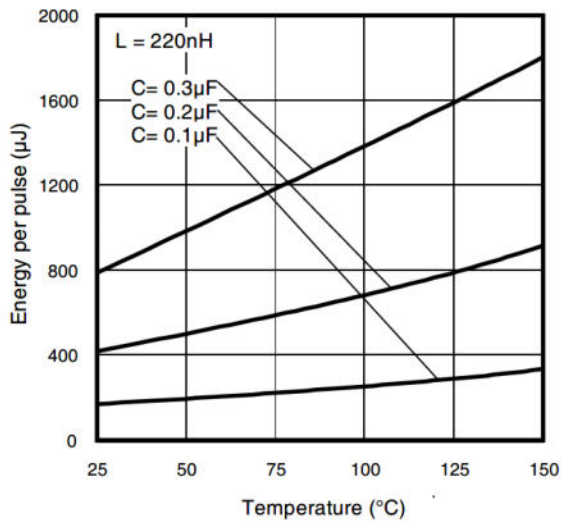
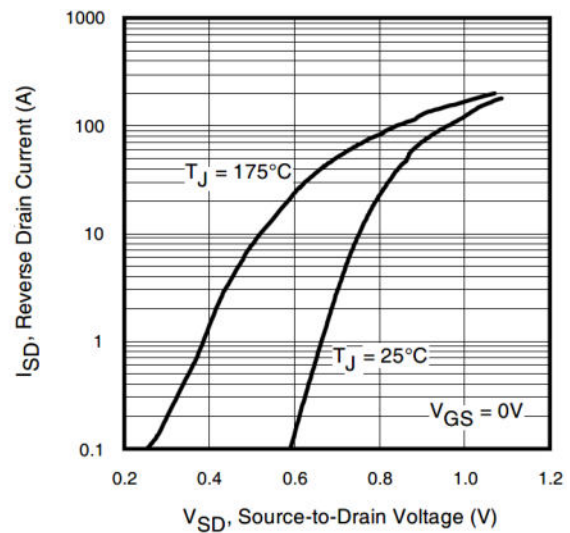
Fig. 7. Typical E_{PULSE} vs. Temperature

Fig. 8. Typical Source-Drain Diode Forward Voltage

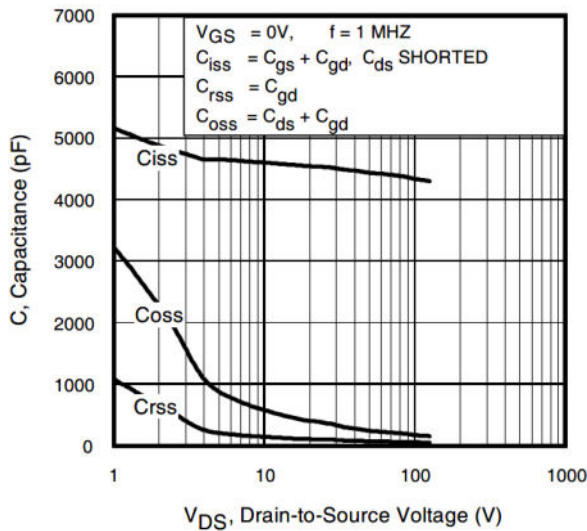


Fig. 9. Typical Capacitance vs. Drain-to-Source Voltage

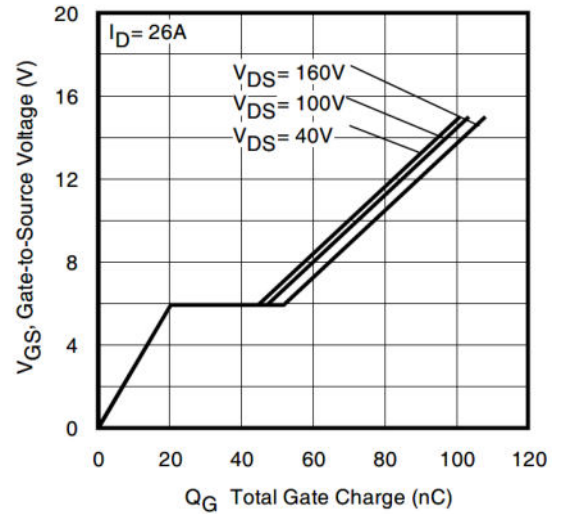


Fig. 10. Typical Gate Charge vs. Gate-to-Source Voltage

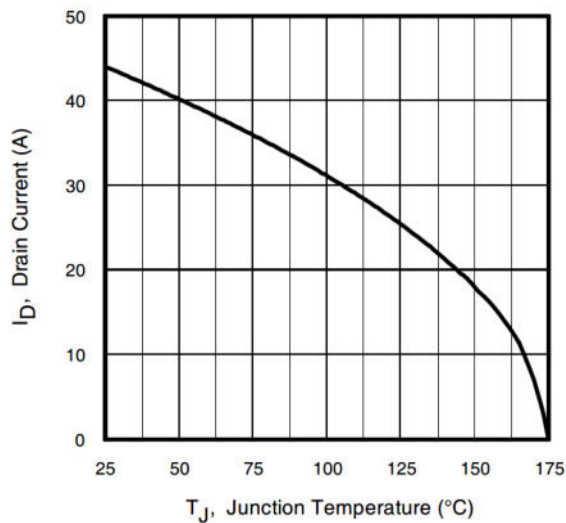


Fig. 11. Maximum Drain Current vs. Case Temperature

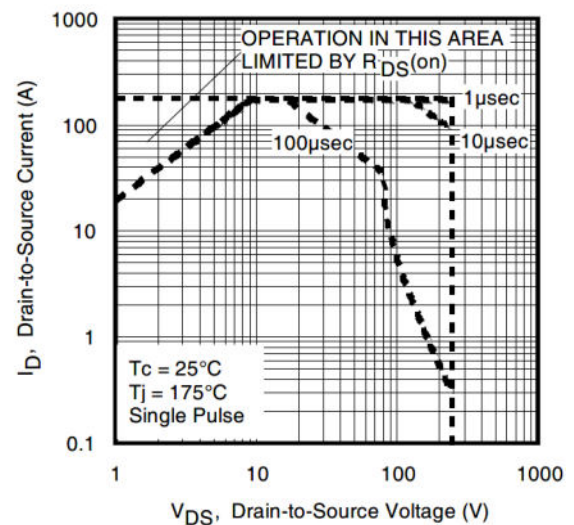


Fig. 12. Maximum Safe Operating Area

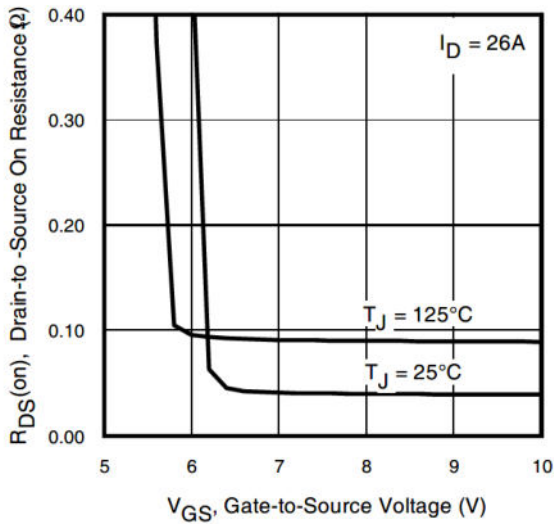


Fig. 13. On-Resistance Vs. Gate Voltage

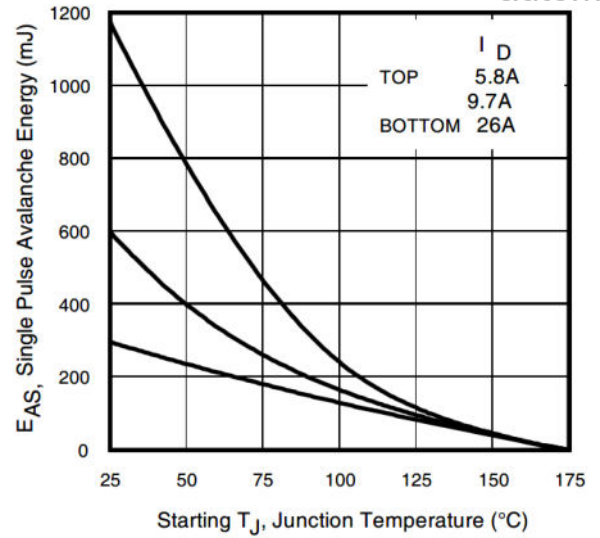


Fig. 14. Maximum Avalanche Energy Vs. Temperature

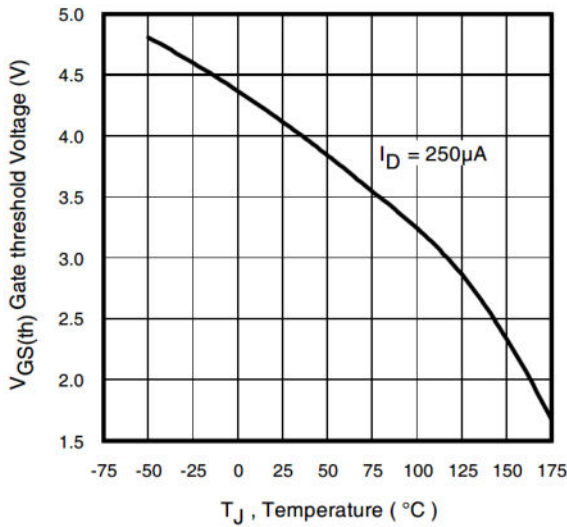


Fig. 15. Threshold Voltage vs. Temperature

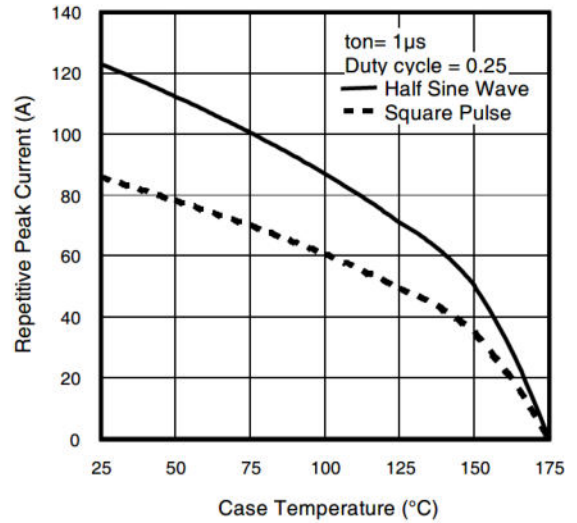


Fig. 16. Typical Repetitive peak Current vs. Case temperature

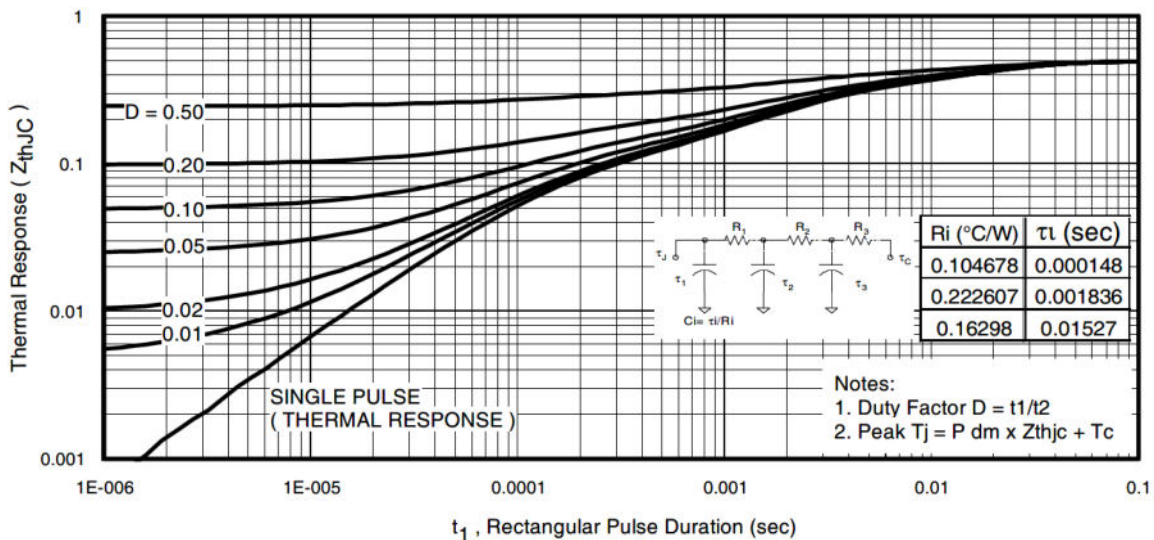


Fig 17. Maximum Effective Transient Thermal Impedance, Junction-to-Case

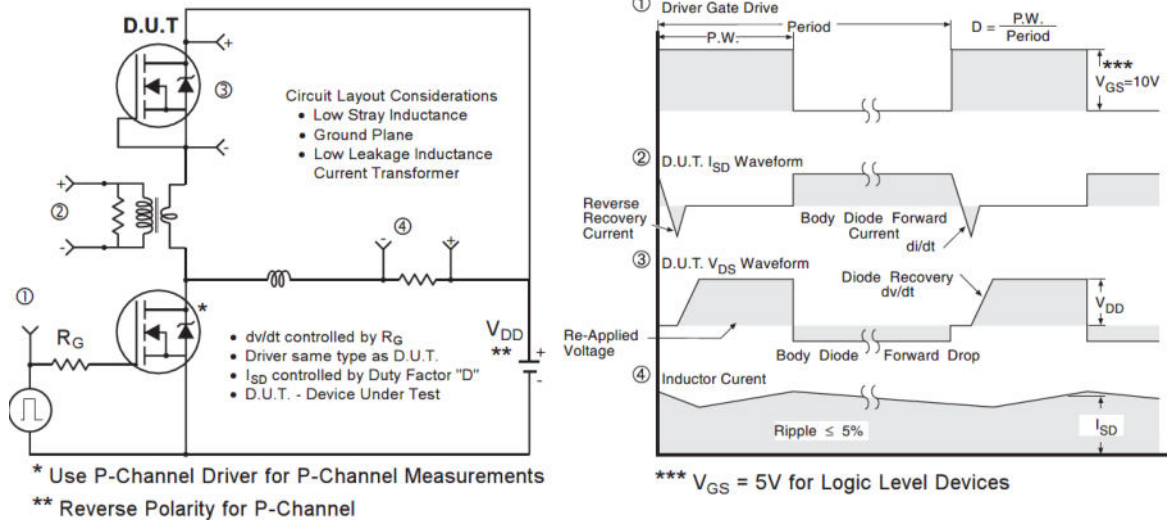


Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

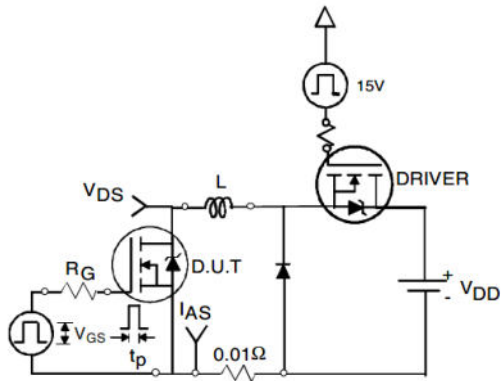


Fig 19a. Unclamped Inductive Test Circuit

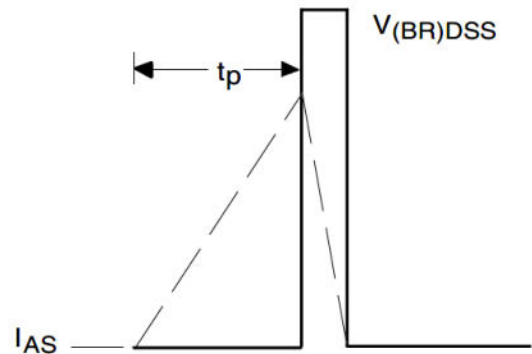


Fig 19b. Unclamped Inductive Waveforms

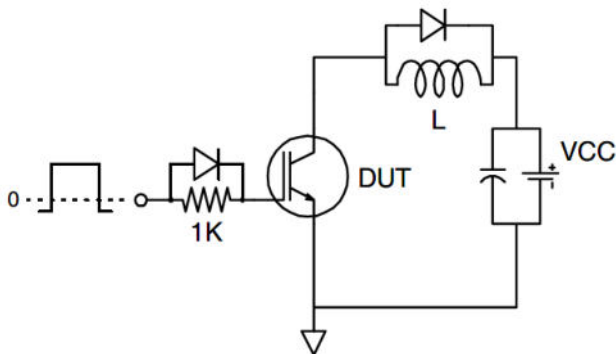


Fig 20a. Gate Charge Test Circuit

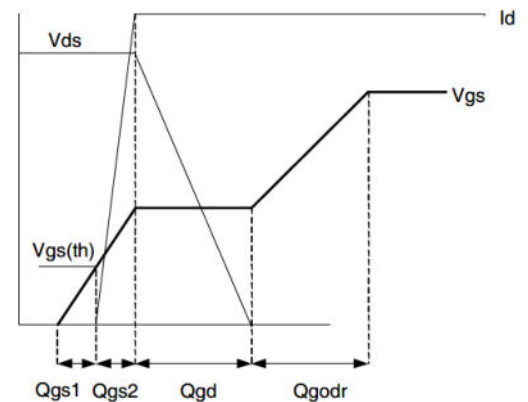


Fig 20b. Gate Charge Waveform

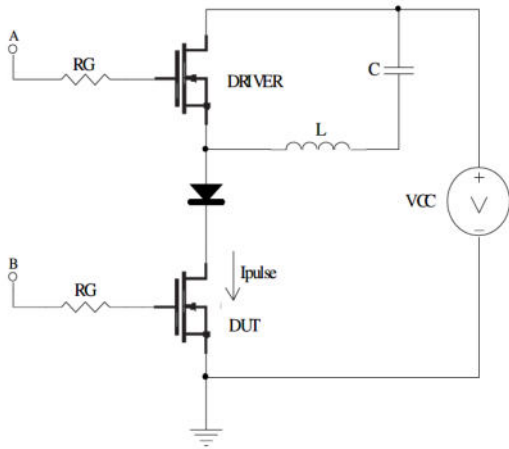


Fig 21a. t_{st} and E_{PULSE} Test Circuit

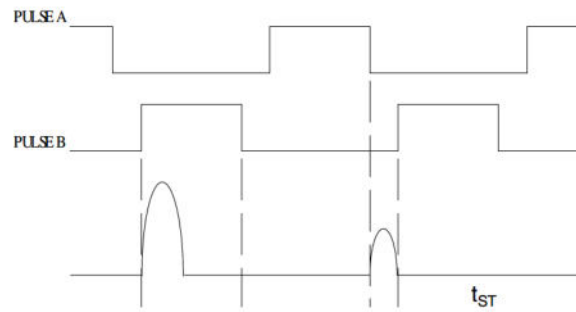


Fig 21b. t_{st} Test Waveforms

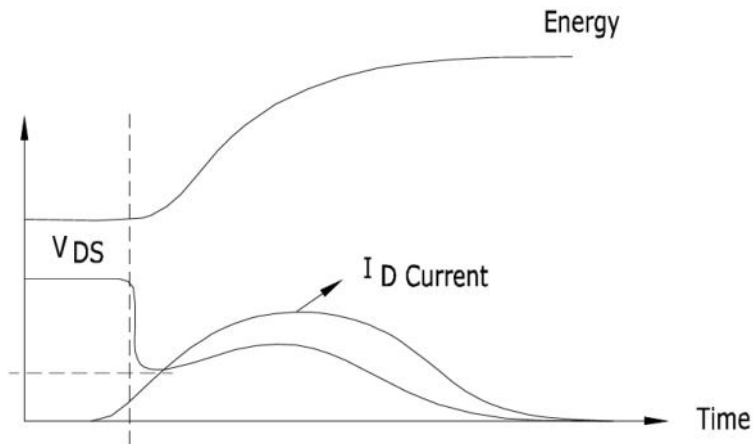


Fig 21c. E_{PULSE} Test Waveforms

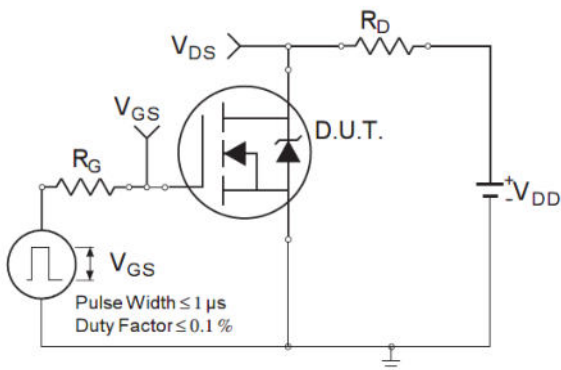


Fig 22a. Switching Time Test Circuit

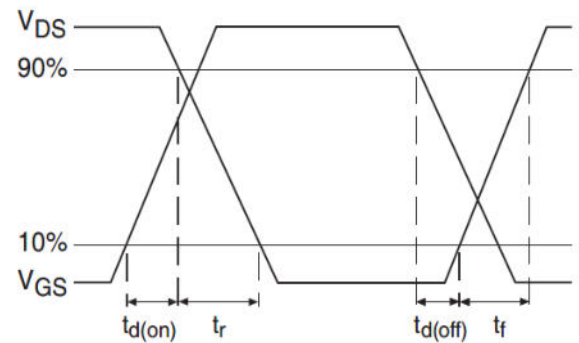
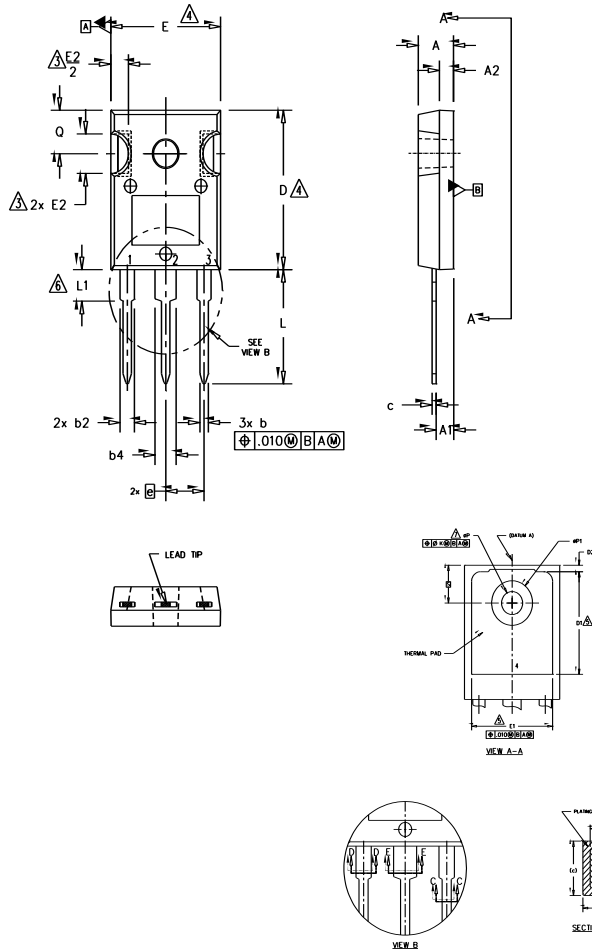


Fig 22b. Switching Time Waveforms

TO-247AC Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

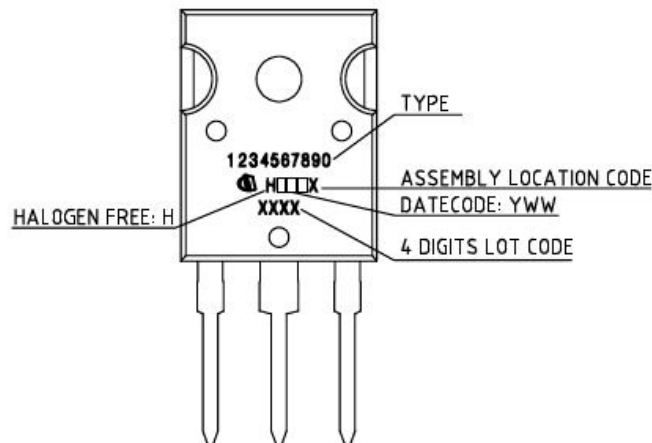
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information



TO-247AC package is not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
2013-09-06	2.0	<ul style="list-style-type: none">Final data sheet
2024-12-05	2.1	<ul style="list-style-type: none">Update datasheet to Infineon formatUpdated Part marking –page 8Added disclaimer on last page.

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