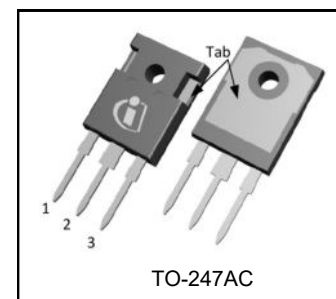
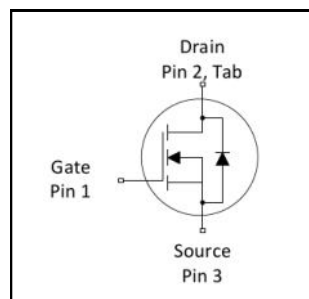


V_{DSS}	150V
$R_{DS(on)}$ typ.	12mΩ
max.	15.5mΩ
I_D	78A



Applications

- Motion Control Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- Hard Switched and High Frequency Circuits

Benefits

- Low $R_{DS(on)}$ Reduces Losses
- Low Gate Charge Improves the Switching Performance
- Improved Diode Recovery Improves Switching & EMI Performance
- 30V Gate Voltage Rating Improves Robustness
- Fully Characterized Avalanche SOA

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP4321PbF	TO-247AC	Tube	25	IRFP4321PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	78①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	55	
I_{DM}	Pulsed Drain Current ②	330	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	310	W
	Linear Derating Factor	2.0	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	210	mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf.in (1.1N.m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.49	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient⑤	—	40	

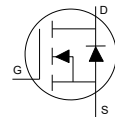
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	150	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	12	15.5	m Ω	$V_{GS} = 10V, I_D = 33A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	0.8	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	130	—	—	S	$V_{DS} = 25V, I_D = 50A$
Q_g	Total Gate Charge	—	71	110	nC	$I_D = 50A$
Q_{gs}	Gate-to-Source Charge	—	24	—		$V_{DS} = 75V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	21	—		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 75V$
t_r	Rise Time	—	60	—		$I_D = 50A$
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		$R_G = 2.5\Omega$
t_f	Fall Time	—	35	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	4460	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	390	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	82	—		$f = 1.0\text{ MHz}$

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	78①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ②	—	—	330	A	
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 50 A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	89	130	ns	I _F = 50A V _R = 128V di/dt = 100A/μs ④
Q _{rr}	Reverse Recovery Charge	—	300	450	nC	
I _{RRM}	Reverse Recovery Current	—	6.5	—	A	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ② Repetitive rating; pulse width limited by max. Junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.17\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 50A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ R_θ is measured at T_J approximately 90°C .

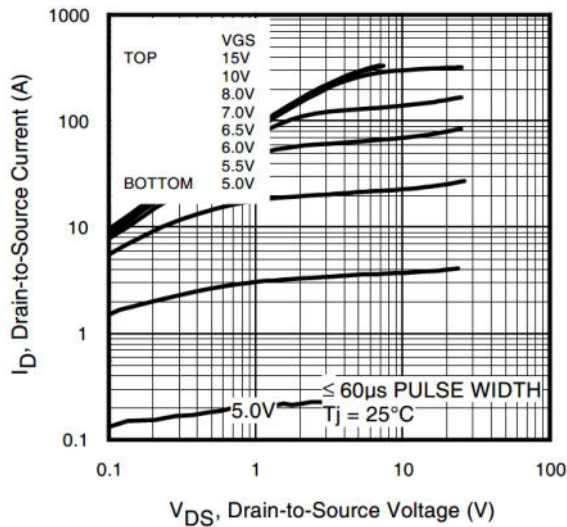


Fig 1. Typical Output Characteristics

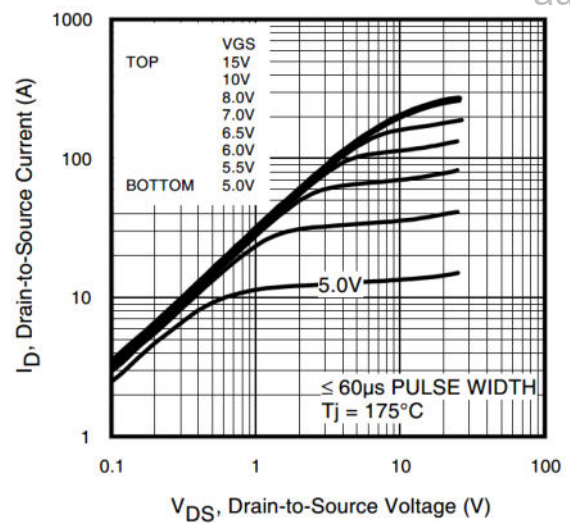


Fig 2. Typical Output Characteristics

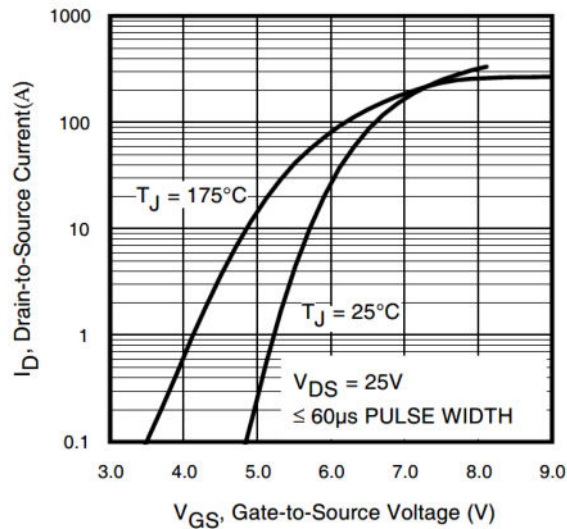


Fig 3. Typical Transfer Characteristics

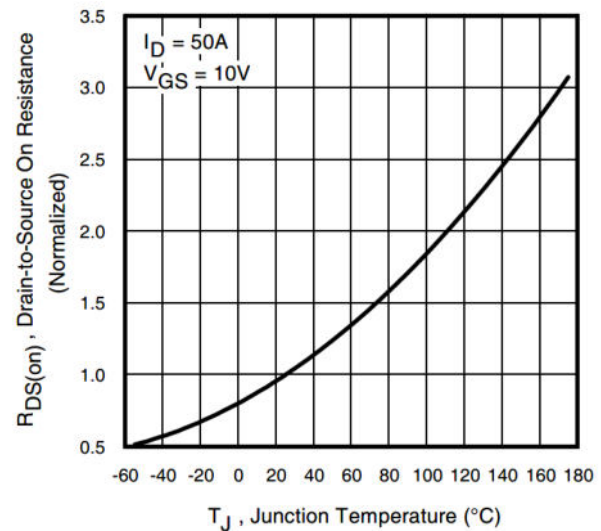


Fig 4. Normalized On-Resistance vs. Temperature

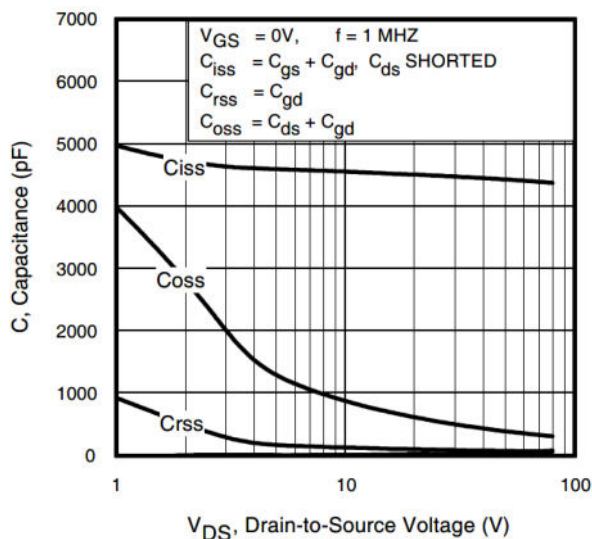


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

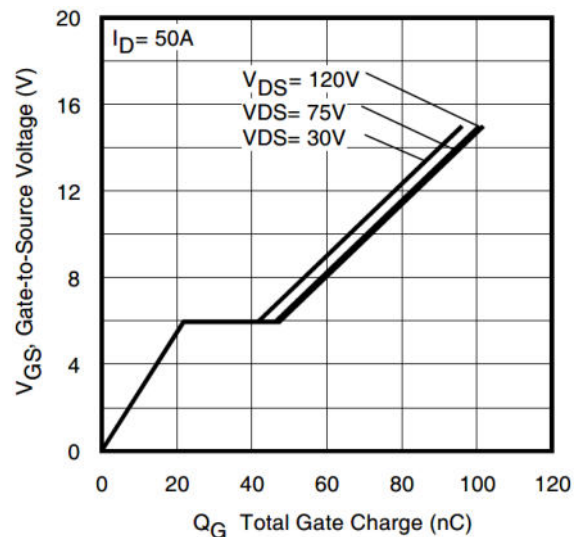


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

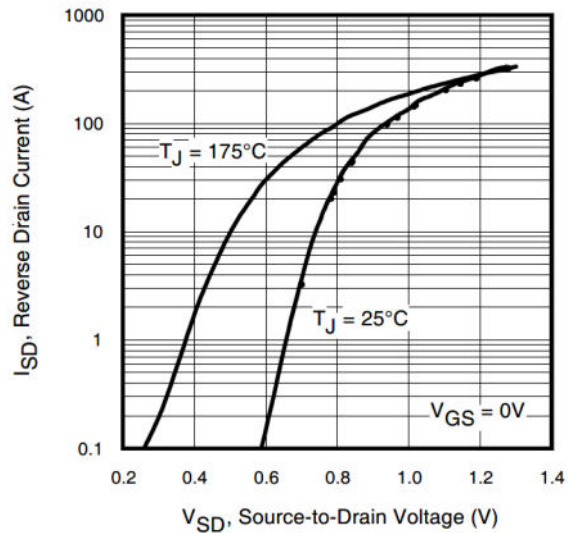


Fig 7. Typical Source-to-Drain Diode Forward Voltage

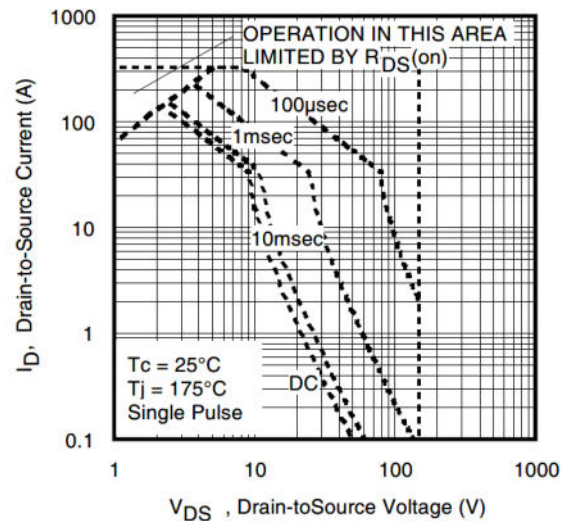


Fig 8. Maximum Safe Operating Area

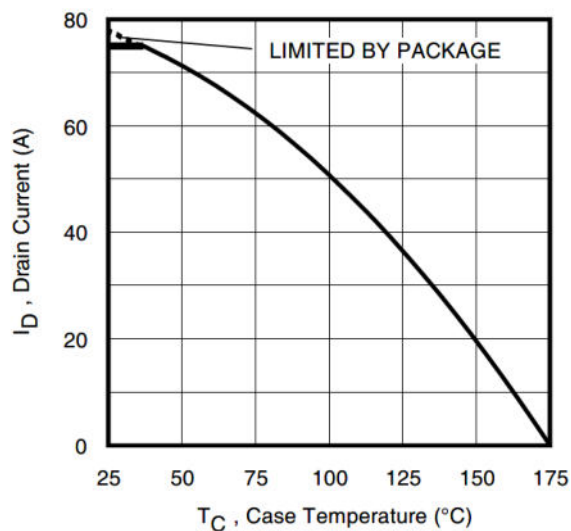


Fig 9. Maximum Drain Current vs. Case Temperature

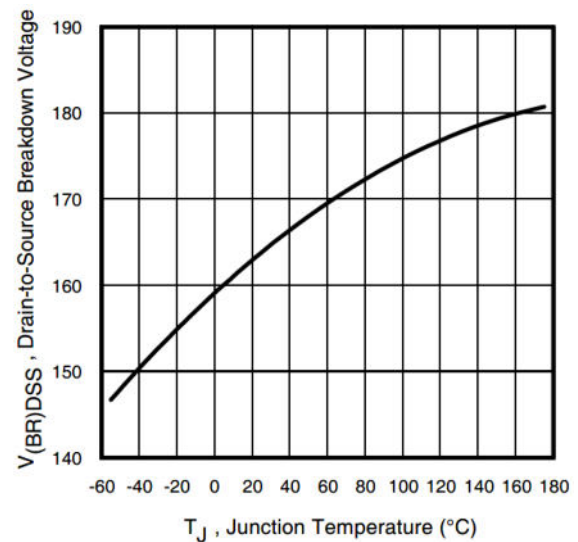


Fig 10. Drain-to-Source Breakdown Voltage

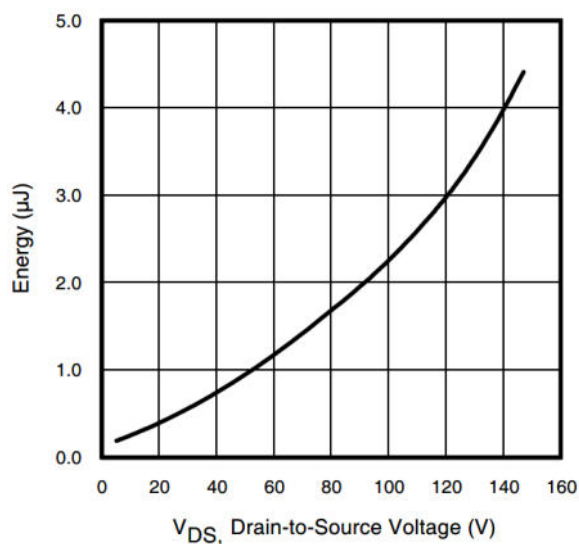


Fig 11. Typical Coss Stored Energy

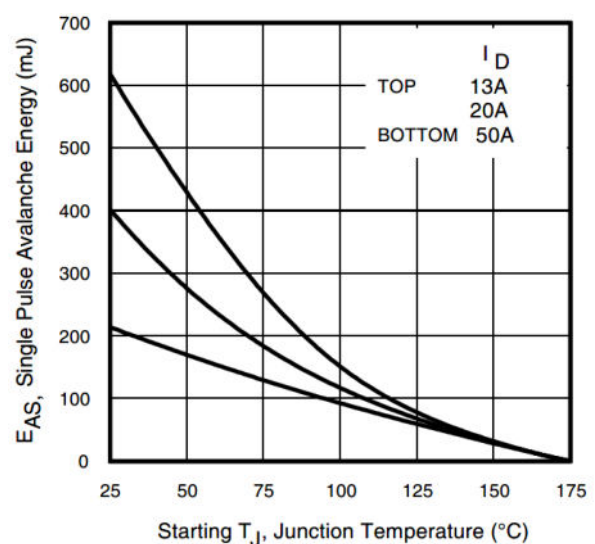


Fig 12. Maximum Avalanche Energy vs. Drain Current

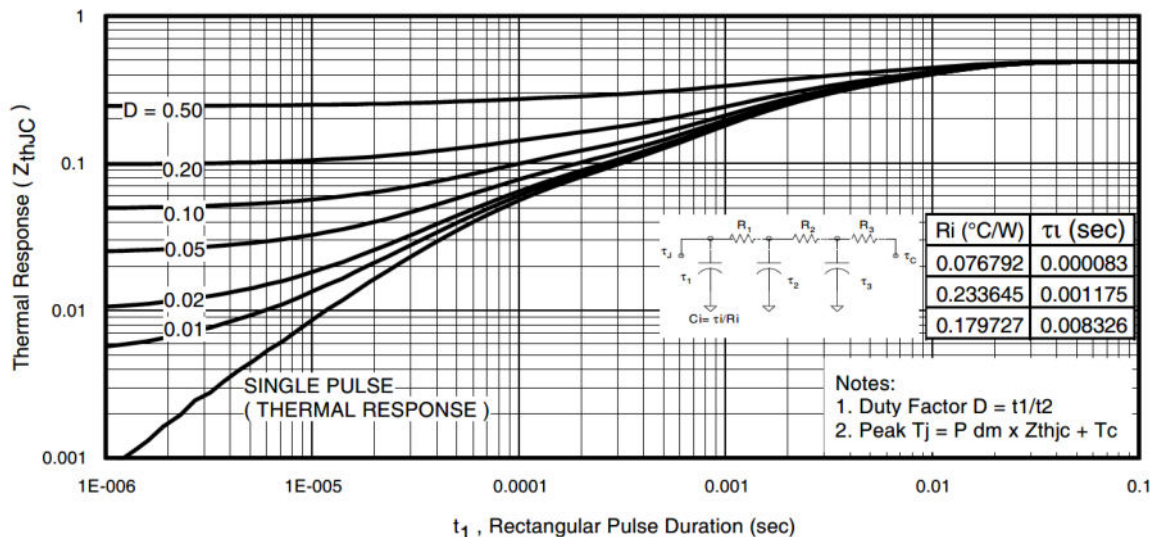


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

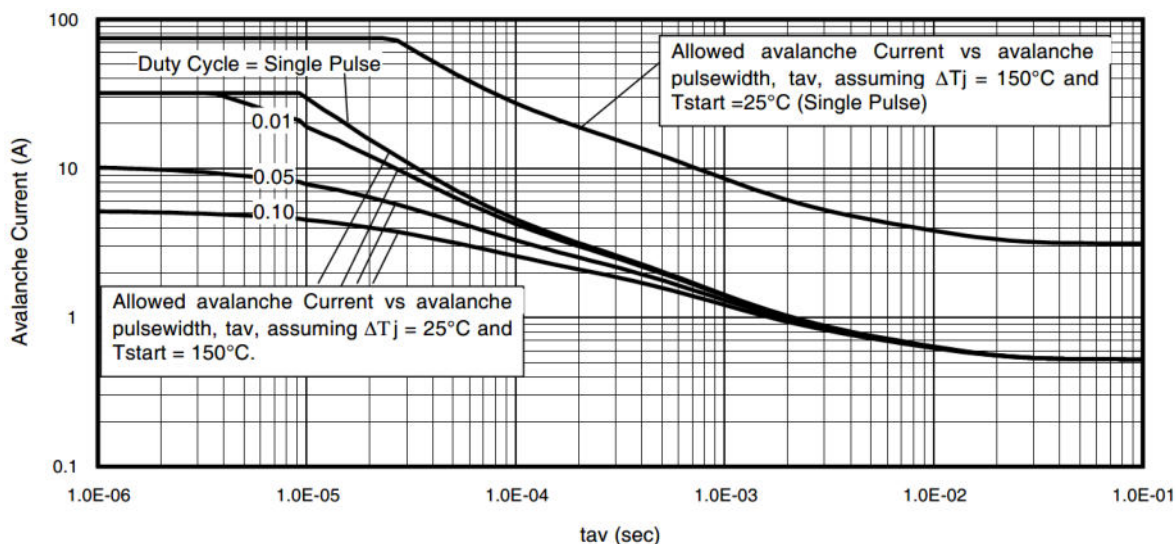


Fig 14. Typical Avalanche Current vs. Pulsewidth

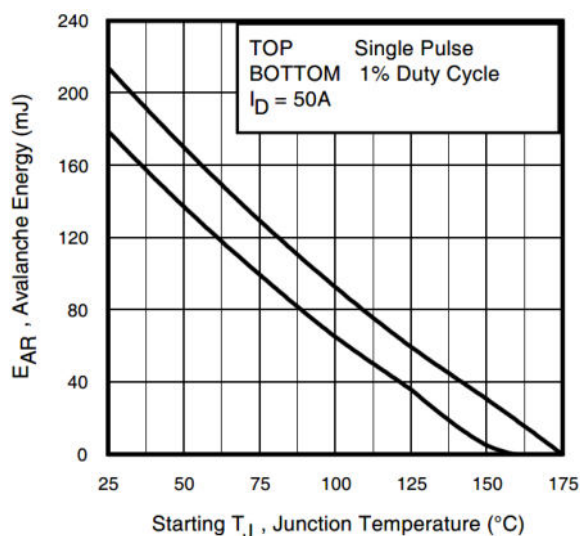


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 14, 15: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

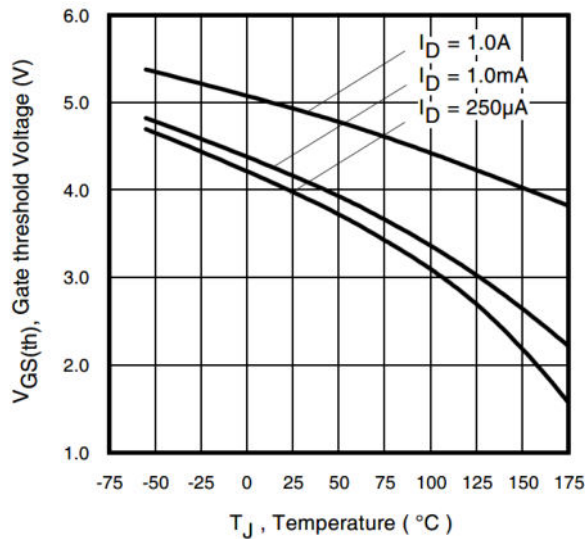
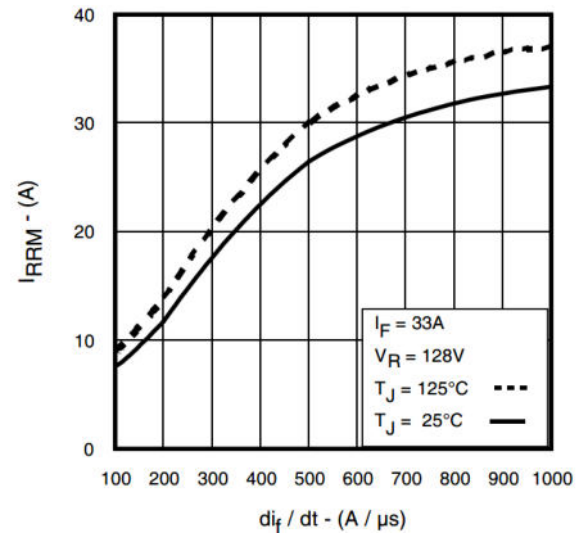
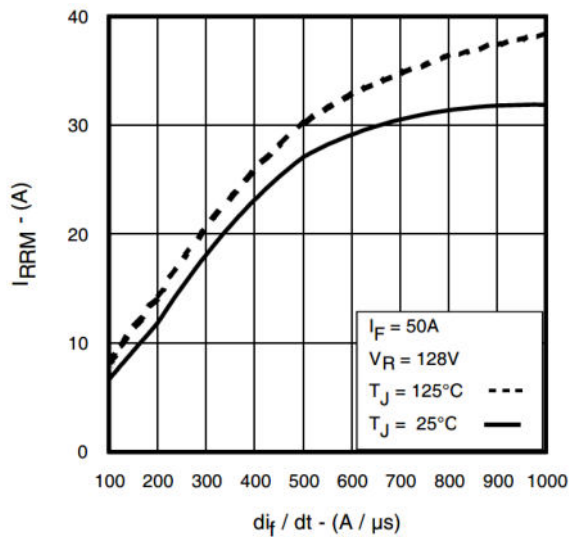
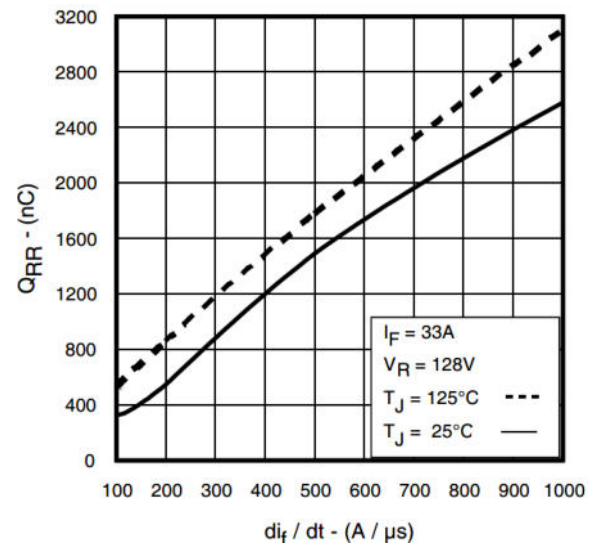
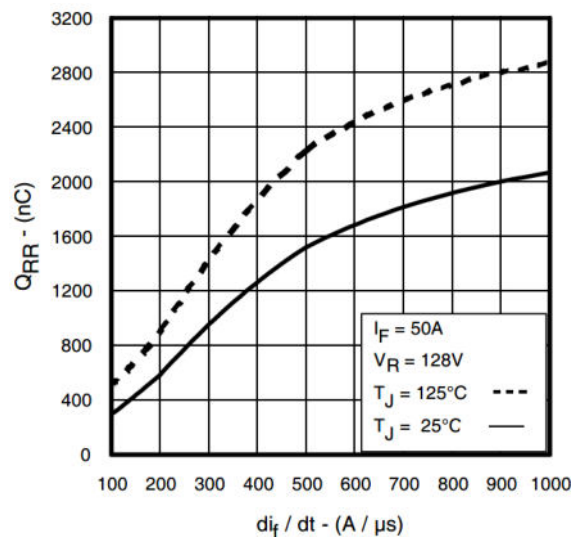


Fig. 16 Threshold Voltage vs. Temperature

Fig. 17 Typical Recovery Current vs. di/dt Fig 18. Typical Recovery Current vs. di/dt Fig 19. Typical Stored Charge vs. di/dt Fig 20. Typical Stored Charge vs. di/dt

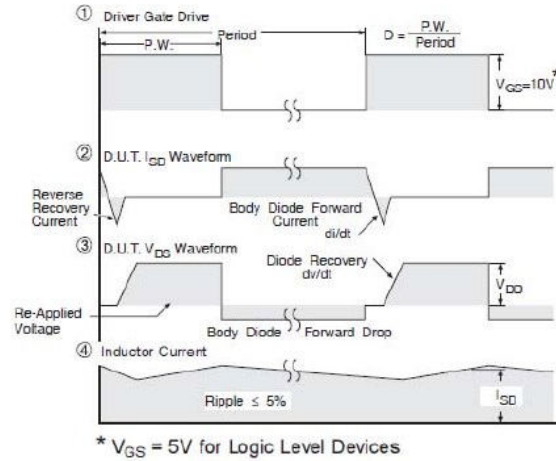
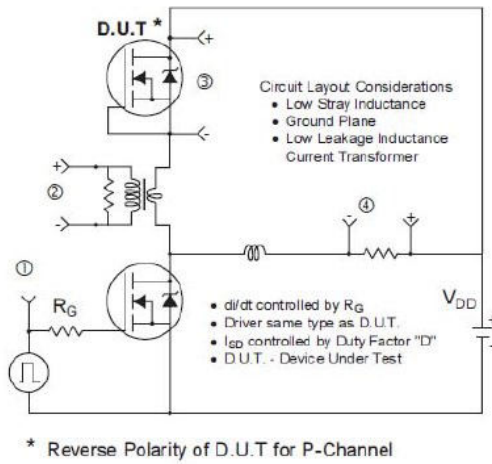


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

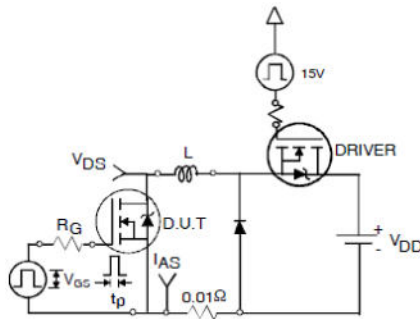


Fig 22a. Unclamped Inductive Test Circuit

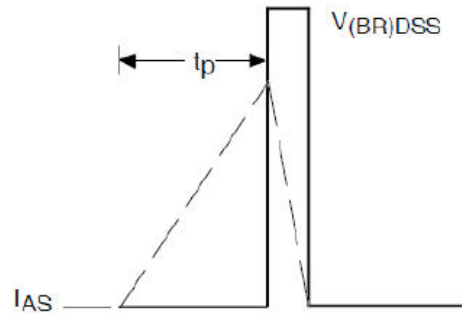


Fig 22b. Unclamped Inductive Waveforms

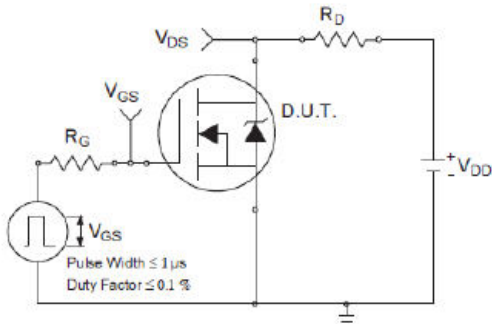


Fig 23a. Switching Time Test Circuit

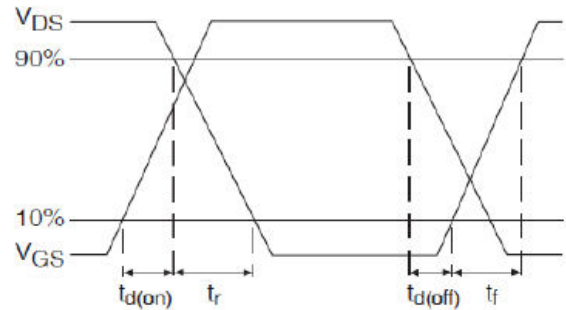


Fig 23b. Switching Time Waveforms

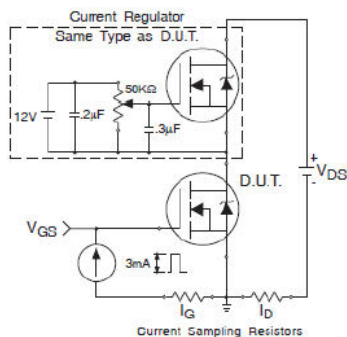


Fig 24a. Gate Charge Test Circuit

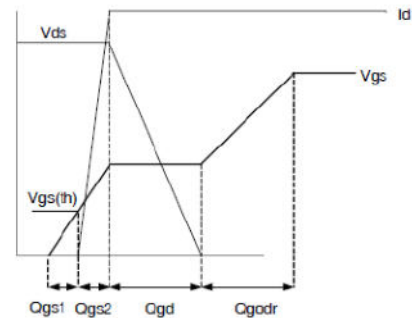
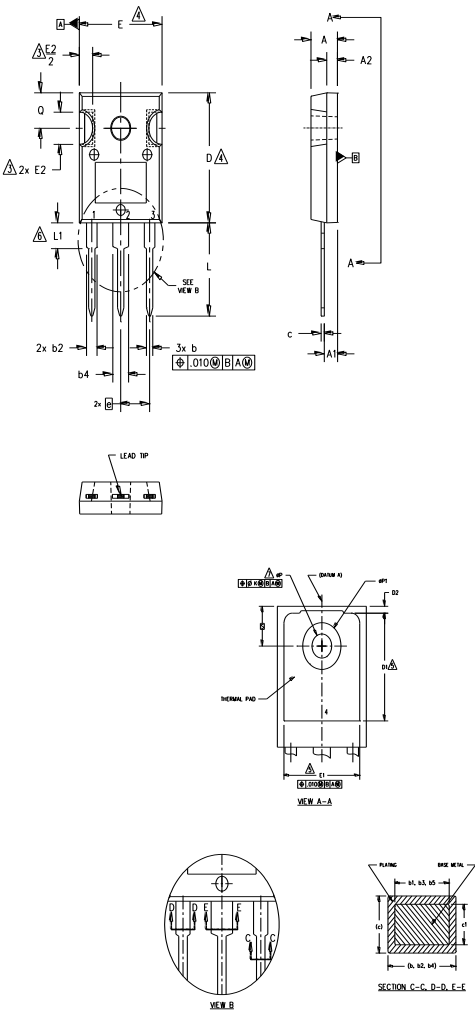


Fig 24b. Gate Charge Waveform

TO-247AC Package Outline (Dimensions are



- NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
 2. DIMENSIONS ARE SHOWN IN INCHES.
 3. CONTOUR OF SLOT OPTIONAL.
 4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
 6. LEAD FINISH UNCONTROLLED IN L1.
 7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	4 5 4
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	
D1	.515	-	13.08	-	
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

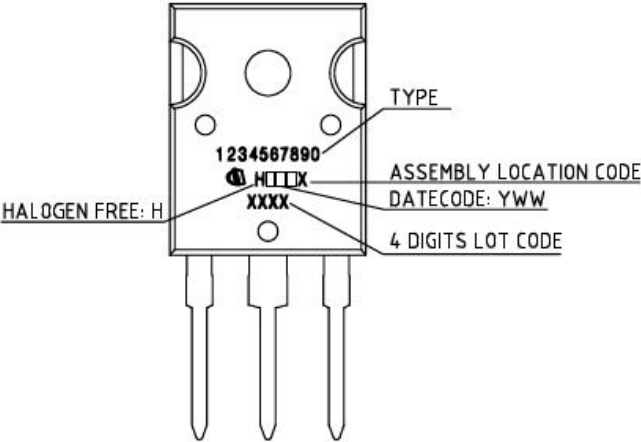
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information



TO-247AC package is not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
11/25/2024	2.1	• Update datasheet to Infineon format • Updated Part marking –page 8 • Added disclaimer on last page.

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