

# International **IR** Rectifier

## Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- Lead-Free

## Benefits

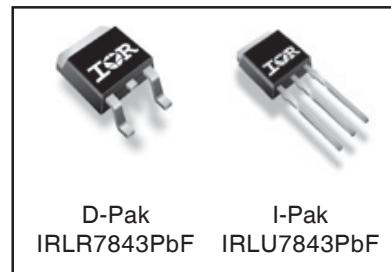
- Very Low RDS(on) at 4.5V V<sub>GS</sub>
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current

PD - 95440B

**IRLR7843PbF****IRLU7843PbF**

HEXFET® Power MOSFET

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>Q<sub>g</sub></b>
<b>30V</b>	<b>3.3mΩ</b>	<b>34nC</b>



## Absolute Maximum Ratings

	Parameter	Max.	Units
V <sub>DS</sub>	Drain-to-Source Voltage	30	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	161 <sup>④</sup>	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	113 <sup>④</sup>	
I <sub>DM</sub>	Pulsed Drain Current <sup>①</sup>	620	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation <sup>⑤</sup>	140	W
P <sub>D</sub> @ T <sub>C</sub> = 100°C	Maximum Power Dissipation <sup>⑤</sup>	71	
	Linear Derating Factor	0.95	W/°C
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
R <sub>0JC</sub>	Junction-to-Case	—	1.05	
R <sub>0JA</sub>	Junction-to-Ambient (PCB Mount) <sup>⑤</sup>	—	50	°C/W
R <sub>0JA</sub>	Junction-to-Ambient	—	110	

Notes ① through ⑤ are on page 11

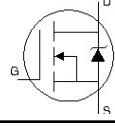
Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$\text{BV}_{\text{DSS}}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{\text{GS}} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	19	—	$\text{mV}/^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	2.6	3.3	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$ , $I_D = 15\text{A}$ ③
		—	3.2	4.0		$V_{\text{GS}} = 4.5\text{V}$ , $I_D = 12\text{A}$ ③
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	1.4	—	2.3	V	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250\mu\text{A}$
$\Delta V_{\text{GS}(\text{th})}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.4	—	$\text{mV}/^\circ\text{C}$	
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu\text{A}$	$V_{\text{DS}} = 24\text{V}$ , $V_{\text{GS}} = 0\text{V}$
		—	—	150		$V_{\text{DS}} = 24\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{\text{GS}} = -20\text{V}$
$g_{\text{fs}}$	Forward Transconductance	37	—	—	S	$V_{\text{DS}} = 15\text{V}$ , $I_D = 12\text{A}$
$Q_g$	Total Gate Charge	—	34	50	nC	$V_{\text{DS}} = 15\text{V}$ $V_{\text{GS}} = 4.5\text{V}$ $I_D = 12\text{A}$ See Fig. 16
$Q_{\text{gs}1}$	Pre-V <sub>th</sub> Gate-to-Source Charge	—	9.1	—		
$Q_{\text{gs}2}$	Post-V <sub>th</sub> Gate-to-Source Charge	—	2.5	—		
$Q_{\text{gd}}$	Gate-to-Drain Charge	—	12	—		
$Q_{\text{godr}}$	Gate Charge Overdrive	—	10	—		
$Q_{\text{sw}}$	Switch Charge ( $Q_{\text{gs}2} + Q_{\text{gd}}$ )	—	15	—		
$Q_{\text{oss}}$	Output Charge	—	21	—	nC	$V_{\text{DS}} = 15\text{V}$ , $V_{\text{GS}} = 0\text{V}$
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	25	—	ns	$V_{\text{DD}} = 15\text{V}$ , $V_{\text{GS}} = 4.5\text{V}$ ③ $I_D = 12\text{A}$ Clamped Inductive Load
$t_r$	Rise Time	—	42	—		
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	34	—		
$t_f$	Fall Time	—	19	—		
$C_{\text{iss}}$	Input Capacitance	—	4380	—	pF	$V_{\text{GS}} = 0\text{V}$ $V_{\text{DS}} = 15\text{V}$ $f = 1.0\text{MHz}$
$C_{\text{oss}}$	Output Capacitance	—	940	—		
$C_{\text{rss}}$	Reverse Transfer Capacitance	—	430	—		

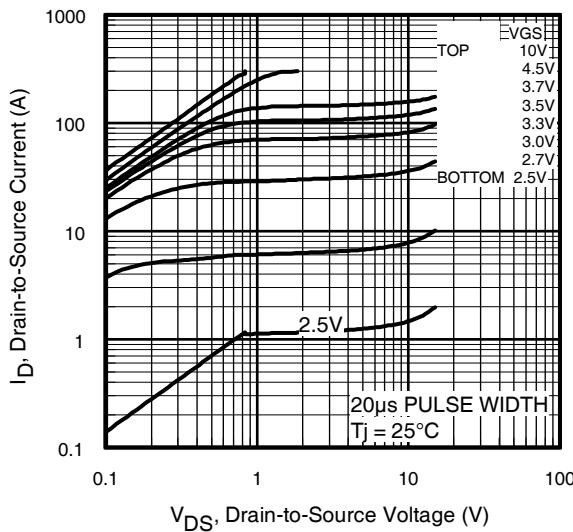
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{\text{AS}}$	Single Pulse Avalanche Energy ③	—	1440	mJ
$I_{\text{AR}}$	Avalanche Current ①	—	12	A
$E_{\text{AR}}$	Repetitive Avalanche Energy ①	—	14	mJ

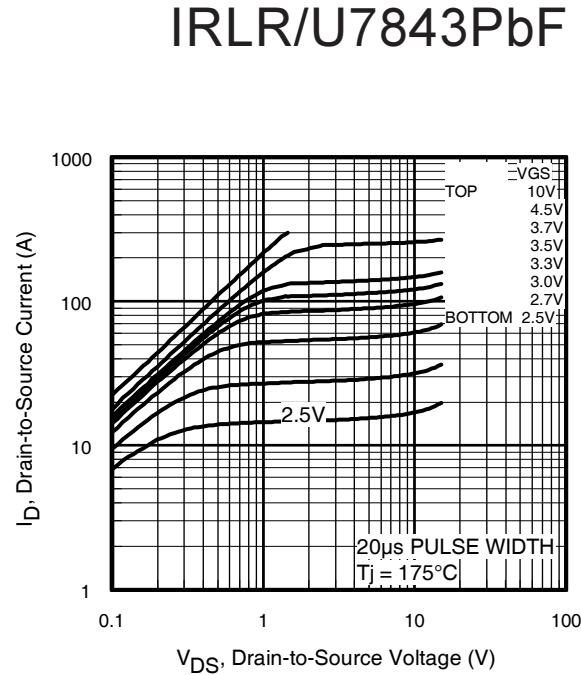
## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_s$	Continuous Source Current (Body Diode)	—	—	161④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
	Pulsed Source Current (Body Diode) ①	—	—	620		
$V_{\text{SD}}$	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}$ , $I_S = 12\text{A}$ , $V_{\text{GS}} = 0\text{V}$ ③
$t_{\text{rr}}$	Reverse Recovery Time	—	39	59	ns	$T_J = 25^\circ\text{C}$ , $I_F = 12\text{A}$ , $V_{\text{DD}} = 15\text{V}$
$Q_{\text{rr}}$	Reverse Recovery Charge	—	36	54	nc	$di/dt = 100\text{A}/\mu\text{s}$ ③
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

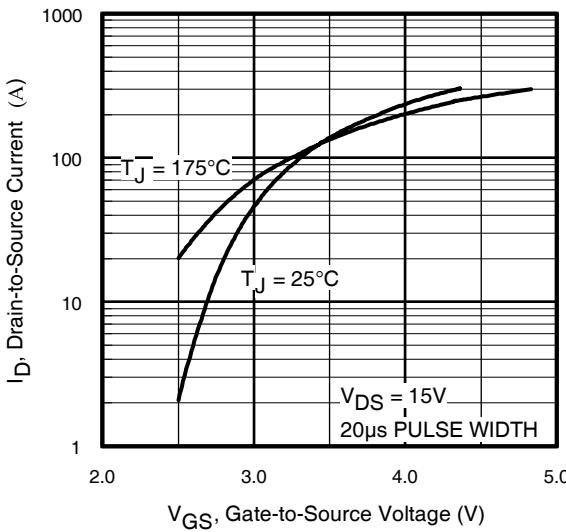
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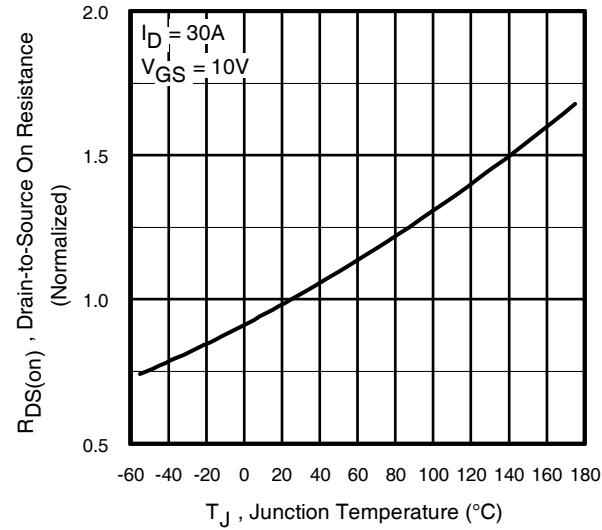
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



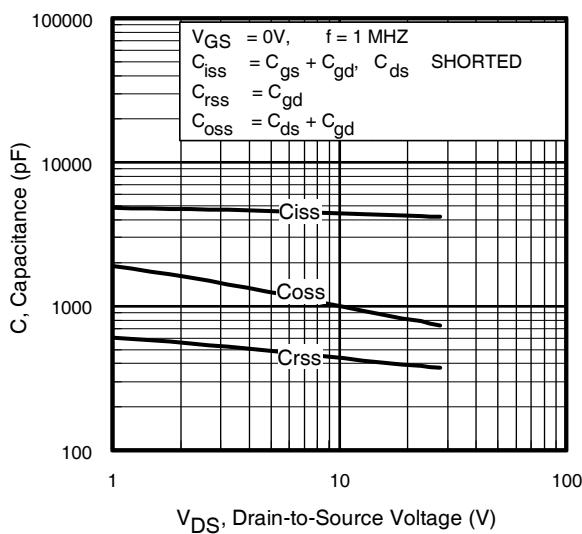
**Fig 3.** Typical Transfer Characteristics



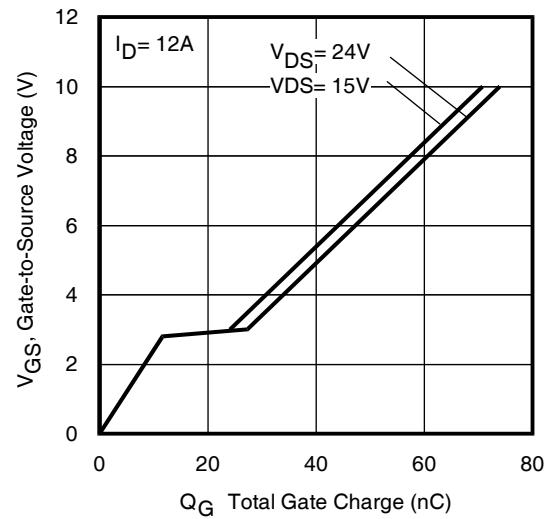
**Fig 4.** Normalized On-Resistance  
vs. Temperature

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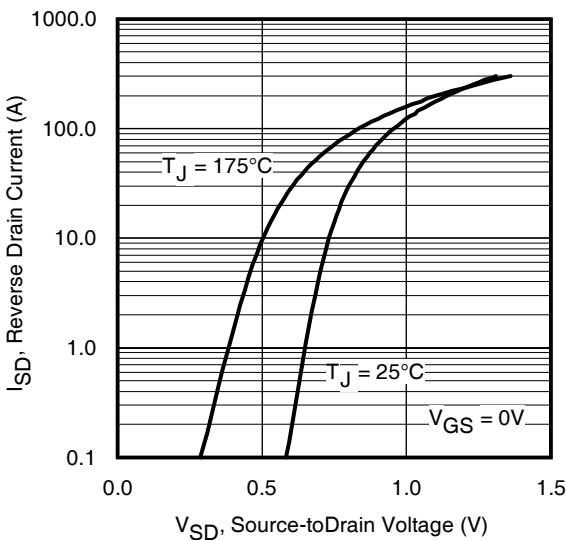
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Rectifier



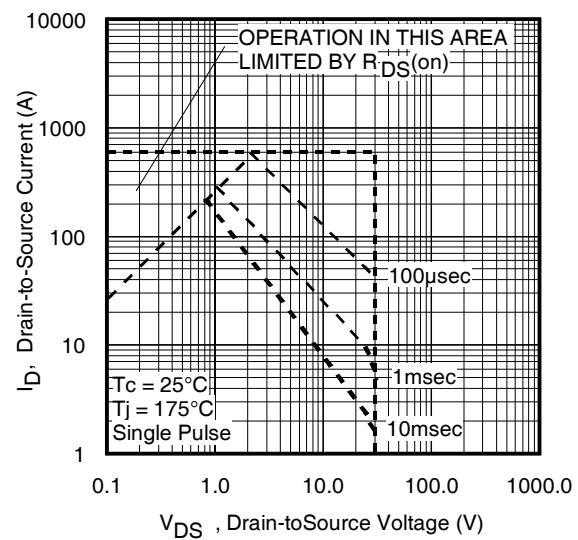
**Fig 5.** Typical Capacitance vs.  
Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge vs.  
Gate-to-Source Voltage



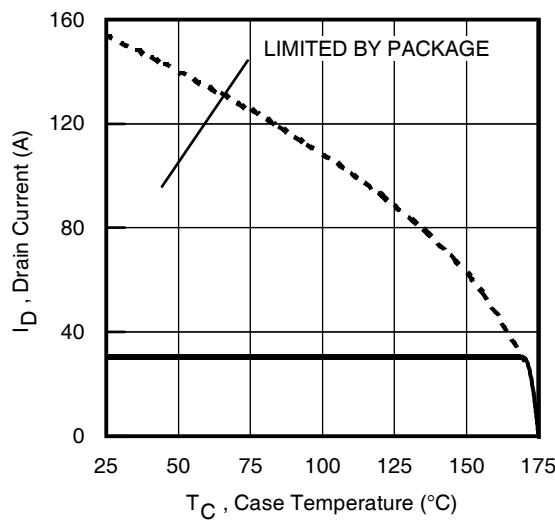
**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



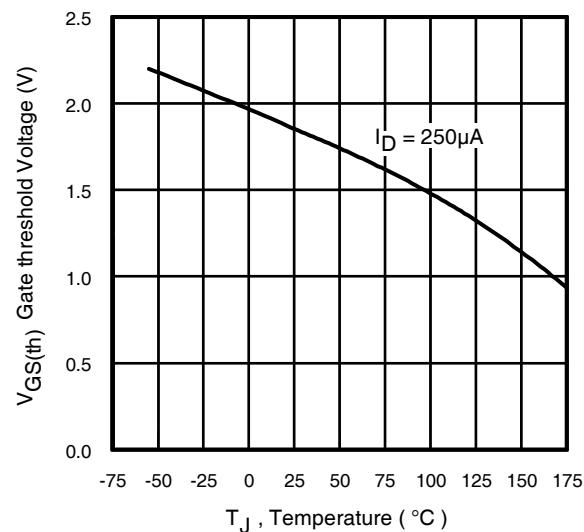
**Fig 8.** Maximum Safe Operating Area

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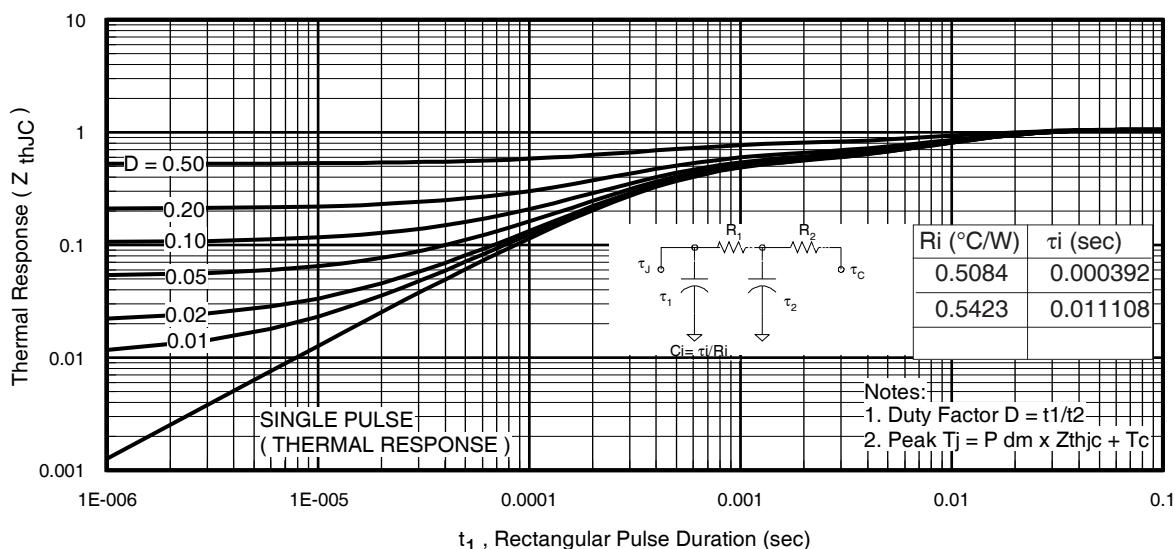
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**Fig 9.** Maximum Drain Current vs.  
Case Temperature



**Fig 10.** Threshold Voltage vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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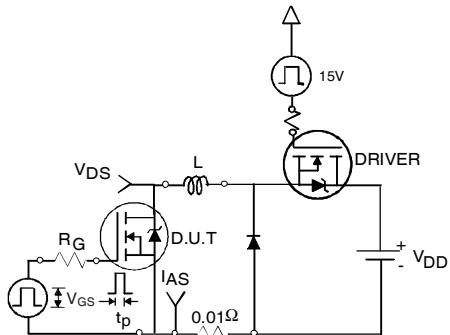


Fig 12a. Unclamped Inductive Test Circuit

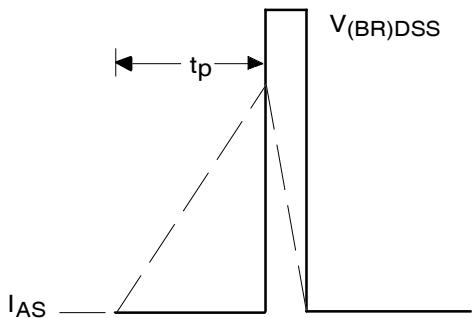


Fig 12b. Unclamped Inductive Waveforms

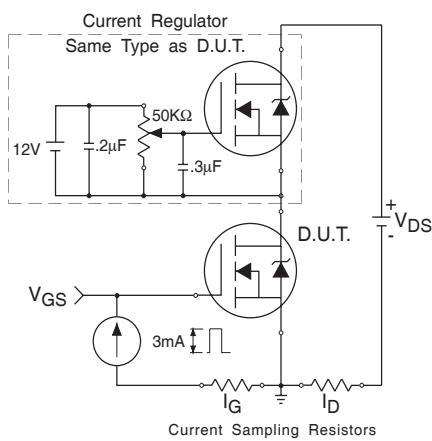


Fig 13. Gate Charge Test Circuit

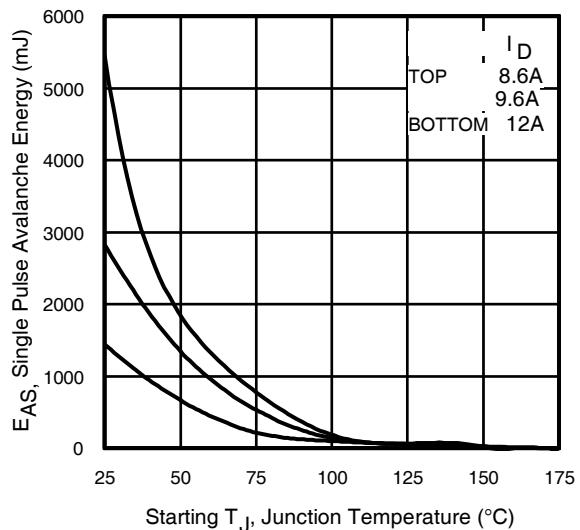


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

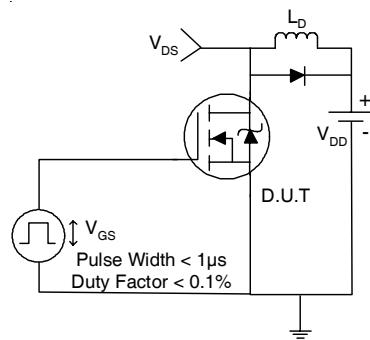


Fig 14a. Switching Time Test Circuit

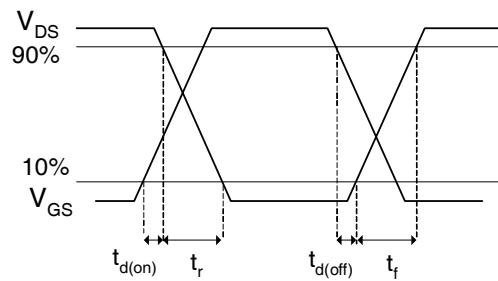
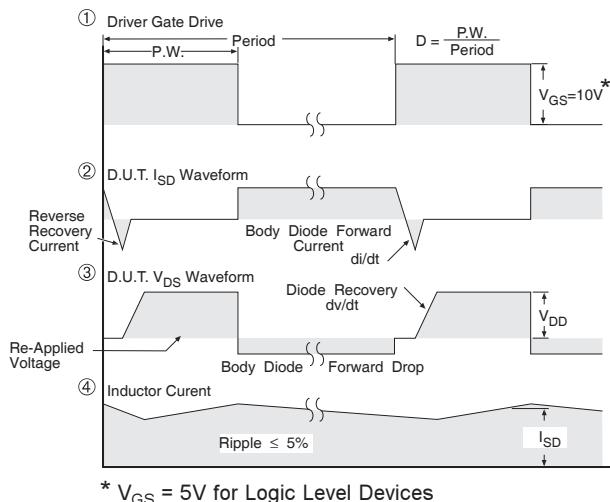
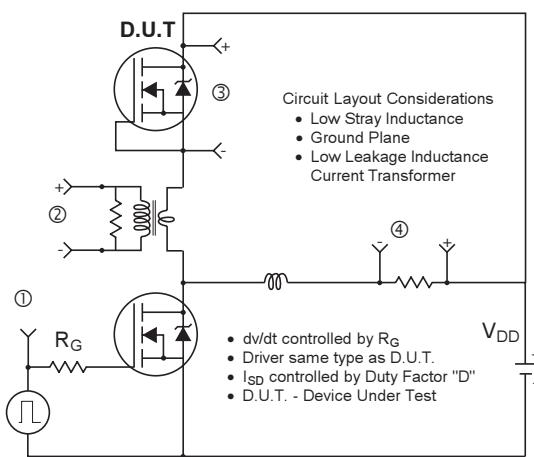


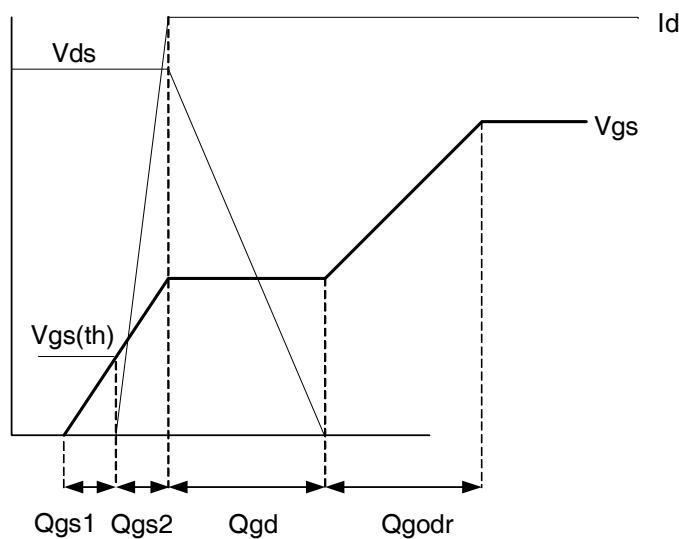
Fig 14b. Switching Time Waveforms

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**Fig 15.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



**Fig 16.** Gate Charge Waveform

## Power MOSFET Selection for Non-Isolated DC/DC Converters

### Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the  $R_{ds(on)}$  of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$\begin{aligned} P_{loss} = & \left( I_{rms}^2 \times R_{ds(on)} \right) \\ & + \left( I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left( I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) \\ & + \left( Q_g \times V_g \times f \right) \\ & + \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right) \end{aligned}$$

This simplified loss equation includes the terms  $Q_{gs2}$  and  $Q_{oss}$  which are new to Power MOSFET data sheets.

$Q_{gs2}$  is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements,  $Q_{gs1}$  and  $Q_{gs2}$ , can be seen from Fig 16.

$Q_{gs2}$  indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to  $I_{dmax}$  at which time the drain voltage begins to change. Minimizing  $Q_{gs2}$  is a critical factor in reducing switching losses in Q1.

$Q_{oss}$  is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how  $Q_{oss}$  is formed by the parallel combination of the voltage dependant (non-linear) capacitance's  $C_{ds}$  and  $C_{dg}$  when multiplied by the power supply input buss voltage.

### Synchronous FET

The power loss equation for Q2 is approximated by;

$$\begin{aligned} P_{loss} &= P_{conduction} + P_{drive} + P_{output}^* \\ P_{loss} &= \left( I_{rms}^2 \times R_{ds(on)} \right) \\ &+ \left( Q_g \times V_g \times f \right) \\ &+ \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right) + \left( Q_{rr} \times V_{in} \times f \right) \end{aligned}$$

\*dissipated primarily in Q1.

For the synchronous MOSFET Q2,  $R_{ds(on)}$  is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge  $Q_{oss}$  and reverse recovery charge  $Q_{rr}$  both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to  $Cdv/dt$  turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and  $V_{in}$ . As Q1 turns on and off there is a rate of change of drain voltage  $dV/dt$  which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of  $Q_{gd}/Q_{gs1}$  must be minimized to reduce the potential for  $Cdv/dt$  turn on.

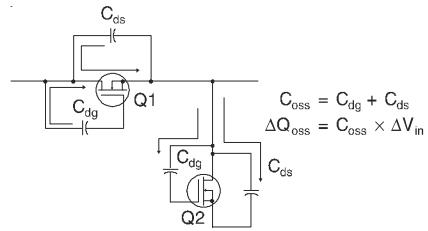
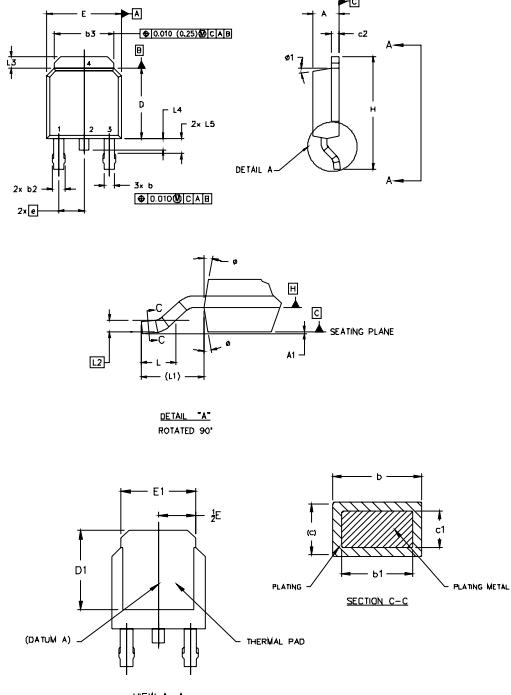


Figure A:  $Q_{oss}$  Characteristic

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## D-Pak (TO-252AA) Package Outline

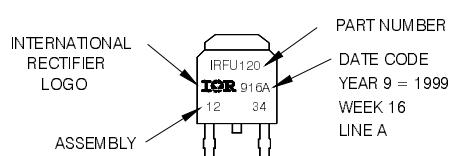


NOTES:						
1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.						
2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].						
3.0 LEAD DIMENSION UNCONTROLLED IN L5						
4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.						
5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.254] FROM THE LEAD TIP.						
6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.						
7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.						
SYMBOL	DIMENSIONS			NOTES	LEAD ASSIGNMENTS	
	MILLIMETERS		INCHES	HEXFET		
	MIN.	MAX.	MIN. MAX	IGBTs, CoPACK		
A	2.18	2.39	.086 .094		1.- GATE	
A1		0.13		.005	2.- DRAIN	
b	0.64	0.89	.025 .035	5	3.- SOURCE	
b1	0.64	0.79	.025 .031	5	4.- DRAIN	
b2	0.76	1.14	.030 .045		1.- GATE	
b3	4.95	5.46	.195 .215		2.- COLLECTOR	
c	0.46	0.81	.018 .024	5	3.- Emitter	
c1	0.41	0.56	.016 .022	5	4.- COLLECTOR	
c2	.046	0.89	.018 .035	5		
D	5.97	6.22	.235 .245	6		
D1	5.21		.205 -	4		
E	6.35	6.73	.250 .265	6		
E1	4.32		.170 -	4		
e	.229 .090 BSC					
H	9.40	10.41	.370 .410			
L	1.40	1.78	.055 .070			
LI	.274 REF .108 REF.					
L2	.0051 BSC .020 BSC					
L3	0.89	1.27	.035 .050			
L4		1.02		.040		
L5	1.14	1.52	.045 .060	3		
ø	0"	10"	0" 10"			
ø1	0"	15"	0" 15"			

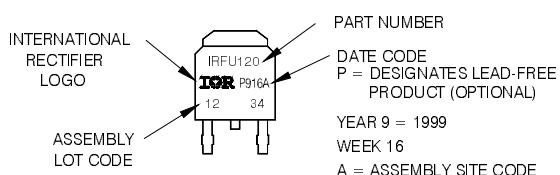
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 1999  
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position indicates 'Lead-Free'



QB



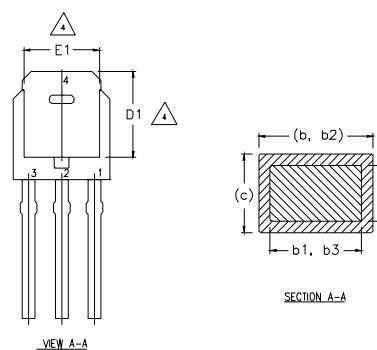
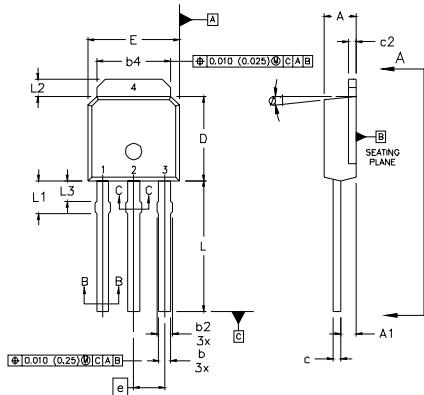
**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>  
[www.irf.com](http://www.irf.com)

# IRLR/U7843PbF

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## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



### NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	2.18	2.39	0.086	.094		
A1	0.89	1.14	0.035	0.045		
b	0.64	0.89	0.025	0.035		
b1	0.64	0.79	0.025	0.031	4	
b2	0.76	1.14	0.030	0.045		
b3	0.76	1.04	0.030	0.041		
b4	5.00	5.46	0.195	0.215	4	
c	0.46	0.61	0.018	0.024		
c1	0.41	0.56	0.016	0.022		
c2	.046	0.86	0.018	0.035		
D	5.97	6.22	0.235	0.245	3, 4	
D1	5.21	—	0.205	—	4	
E	6.35	6.73	0.250	0.265	3, 4	
E1	4.32	—	0.170	—	4	
e	2.29		0.090 BSC			
L	8.89	9.60	0.350	0.380		
L1	1.91	2.29	0.075	0.090		
L2	0.89	1.27	0.035	0.050	4	
L3	1.14	1.52	0.045	0.060	5	
ø1	0"	15"	0"	15"		

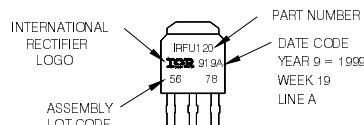
### LEAD ASSIGNMENTS

#### HEXFET

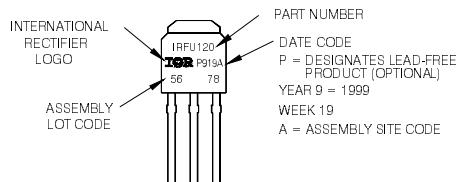
1. - GATE
2. - DRAIN
3. - SOURCE
4. - DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 1999  
IN THE ASSEMBLY LINE 'A'  
Note: 'P' in assembly line  
position indicates 'Lead-Free'



OR



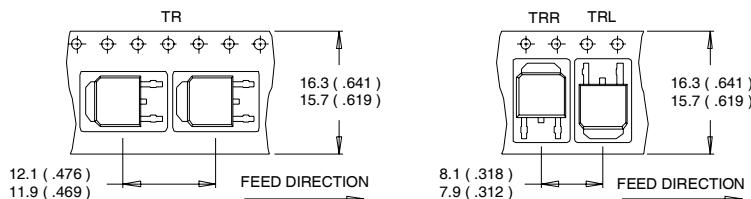
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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## IRLR/U7843PbF

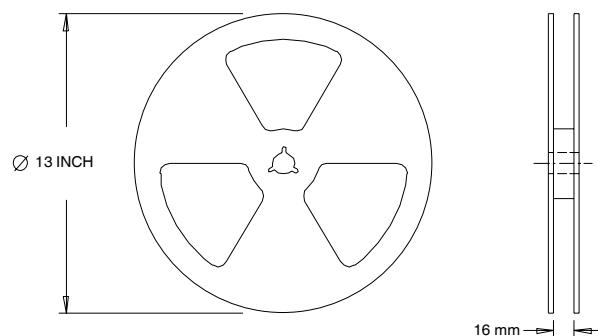
### D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 20\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 12\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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