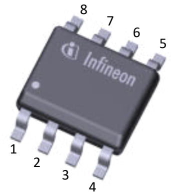
# MOSFET

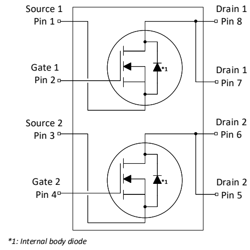
## OptiMOS™ 3 Power-Transistor, 40 V

PG-DSO-8




## Features

- Dual N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21




## Product validation

Qualified according to JEDEC Standard

**Table 1 Key Performance Parameters**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 40 | V |
| $R_{DS(on),max}$ | 25 | mΩ |
| $I_D$ | 7.9 | A |
| $Q_{oss}$ | 5.3 | nC |
| $Q_G$ | 3.8 | nC |

| Type/Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| ISA250250N04LMDS | PG-DSO-8 | 2525N04L | - |

## Table of Contents

# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

**Table 2 Maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current [1] | $I_D$ | - | - | 7.9<br>5.0<br>4.4<br>5.9 | A | $V_{GS}$=10 V, $T_C$=25 °C<br>$V_{GS}$=10 V, $T_C$=100 °C<br>$V_{GS}$=4.5 V, $T_C$=100 °C<br>$V_{GS}$=10 V, $T_A$=25 °C, $R_{thJA}$=90 °C/W [2] |
| Pulsed drain current [3] | $I_{D,pulse}$ | - | - | 32 | A | $T_C$=25 °C |
| Avalanche energy, single pulse [4] | $E_{AS}$ | - | - | 17.2 | mJ | $I_D$=7.9 A, $R_{GS}$=25 Ω |
| Gate source voltage | $V_{GS}$ | -20 | - | 20 | V | - |
| Power dissipation | $P_{tot}$ | - | - | 2.5<br>1.4 | W | $T_C$=25 °C<br>$T_A$=25 °C, $R_{thJA}$=90 °C/W [2] |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 150 | °C | - |

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 $cm^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

# 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - solder point | $R_{thJC}$ | - | - | 50 | °C/W | - |
| Thermal resistance, junction - ambient,<br>6 cm$^2$ cooling area [5)] | $R_{thJA}$ | - | - | 90 | °C/W | - |
| Thermal resistance, junction - ambient,<br>minimum footprint | $R_{thJA}$ | - | - | 150 | °C/W | - |

5) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm$^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

# 3 Electrical characteristics

at $T_j$=25 °C, unless otherwise specified

**Table 4 Static characteristics**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 40 | - | - | V | $V_{GS}$=0 V, $I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 1.1 | - | 2.7 | V | $V_{DS}$=$V_{GS}$, $I_D$=1000 µA |
| Zero gate voltage drain current | $I_{DSS}$ | - | 0.1<br>10 | 1<br>100 | µA | $V_{DS}$=40 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=40 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 10 | 100 | nA | $V_{GS}$=20 V, $V_{DS}$=0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 18<br>26 | 25<br>32 | mΩ | $V_{GS}$=10 V, $I_D$=7.9 A<br>$V_{GS}$=4.5 V, $I_D$=7.1 A |
| Gate resistance | $R_G$ | - | 1.5 | - | Ω | - |
| Transconductance [6] | $g_{fs}$ | 9 | 18 | - | S | $\|V_{DS}\|≥2\|I_D\|R_{DS(on)max}$, $I_D$=7.9 A |

6) Defined by design. Not subject to production test.

**Table 5 Dynamic characteristics**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance [7] | $C_{iss}$ | - | 550 | 720 | pF | $V_{GS}$=0 V, $V_{DS}$=20 V, $f$=1 MHz |
| Output capacitance [7] | $C_{oss}$ | - | 150 | 200 | pF | $V_{GS}$=0 V, $V_{DS}$=20 V, $f$=1 MHz |
| Reverse transfer capacitance [7] | $C_{rss}$ | - | 10 | 18 | pF | $V_{GS}$=0 V, $V_{DS}$=20 V, $f$=1 MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 5.8 | - | ns | $V_{DD}$=20 V, $V_{GS}$=4.5 V, $I_D$=7.9 A, $R_{G,ext}$=1.6 Ω |
| Rise time | $t_r$ | - | 5.3 | - | ns | $V_{DD}$=20 V, $V_{GS}$=4.5 V, $I_D$=7.9 A, $R_{G,ext}$=1.6 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 2.9 | - | ns | $V_{DD}$=20 V, $V_{GS}$=4.5 V, $I_D$=7.9 A, $R_{G,ext}$=1.6 Ω |
| Fall time | $t_f$ | - | 4.0 | - | ns | $V_{DD}$=20 V, $V_{GS}$=4.5 V, $I_D$=7.9 A, $R_{G,ext}$=1.6 Ω |

7) Defined by design. Not subject to production test.

## Table 6 Gate charge characteristics [8)]

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 1.8 | - | nC | $V_{DD}$=20 V, $I_D$=7.9 A, $V_{GS}$=0 to 4.5 V |
| Gate charge at threshold | $Q_{g(th)}$ | - | 0.9 | - | nC | $V_{DD}$=20 V, $I_D$=7.9 A, $V_{GS}$=0 to 4.5 V |
| Gate to drain charge | $Q_{gd}$ | - | 1.0 | - | nC | $V_{DD}$=20 V, $I_D$=7.9 A, $V_{GS}$=0 to 4.5 V |
| Switching charge | $Q_{sw}$ | - | 1.9 | - | nC | $V_{DD}$=20 V, $I_D$=7.9 A, $V_{GS}$=0 to 4.5 V |
| Gate charge total [9)] | $Q_g$ | - | 3.8 | 5.7 | nC | $V_{DD}$=20 V, $I_D$=7.9 A, $V_{GS}$=0 to 4.5 V |
| Gate plateau voltage | $V_{plateau}$ | - | 3.2 | - | V | $V_{DD}$=20 V, $I_D$=7.9 A, $V_{GS}$=0 to 4.5 V |
| Gate charge total [9)] | $Q_g$ | - | 7.9 | 11.9 | nC | $V_{DD}$=20 V, $I_D$=7.9 A, $V_{GS}$=0 to 10 V |
| Output charge | $Q_{oss}$ | - | 5.3 | - | nC | $V_{DS}$=20 V, $V_{GS}$=0 V |

8) See "Gate charge waveforms" for parameter definition

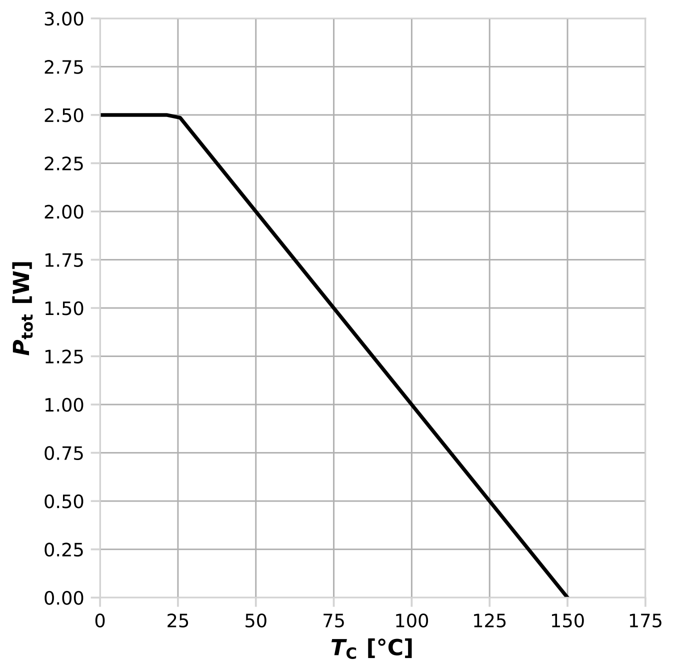
9) Defined by design. Not subject to production test.

## Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | $I_S$ | - | - | 3.1 | A | $T_C$=25 °C |
| Diode pulse current | $I_{S,pulse}$ | - | - | 32 | A | $T_C$=25 °C |
| Diode forward voltage | $V_{SD}$ | - | 0.87 | 1.0 | V | $V_{GS}$=0 V, $I_F$=7.9 A, $T_j$=25 °C |
| Reverse recovery time | $t_{rr}$ | - | 12 | - | ns | $V_R$=20 V, $I_F$=7.9 A, $di_F/dt$=100 A/µs |
| Reverse recovery charge | $Q_{rr}$ | - | 3.6 | - | nC | $V_R$=20 V, $I_F$=7.9 A, $di_F/dt$=100 A/µs |

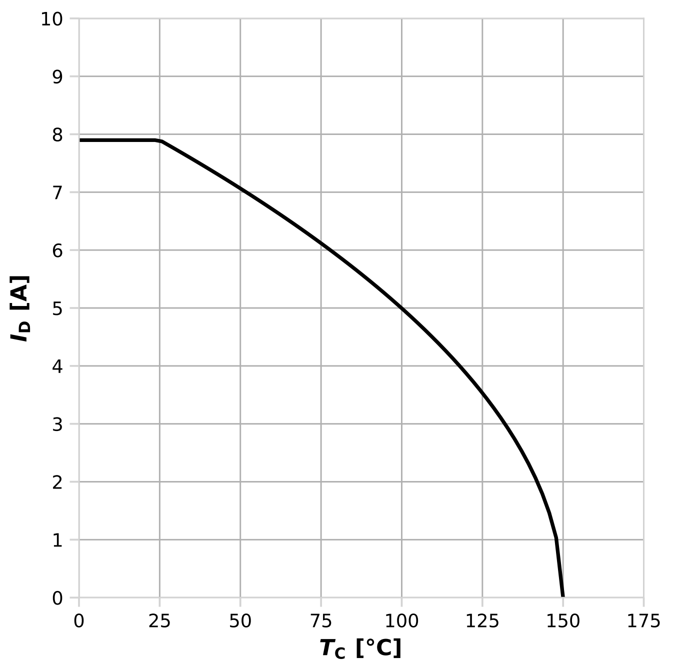
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



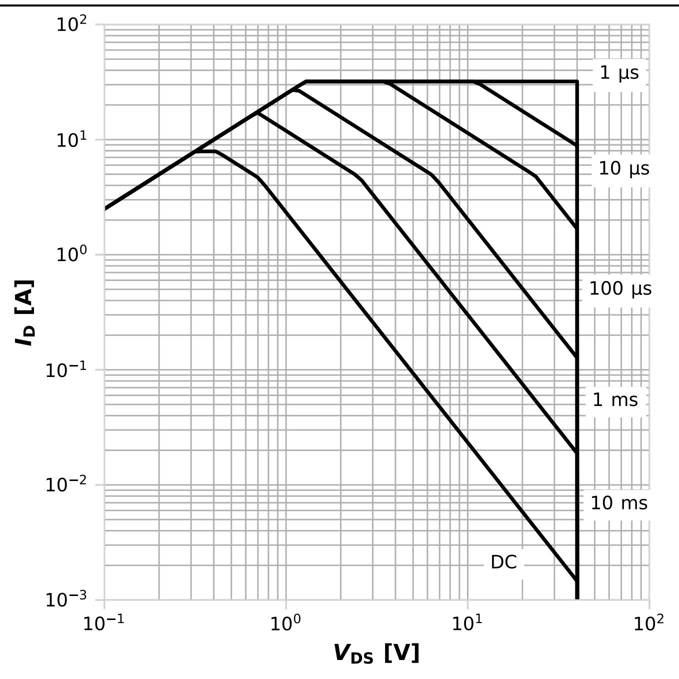

$P_{tot}$=f($T_C$)

**Diagram 2: Drain current**



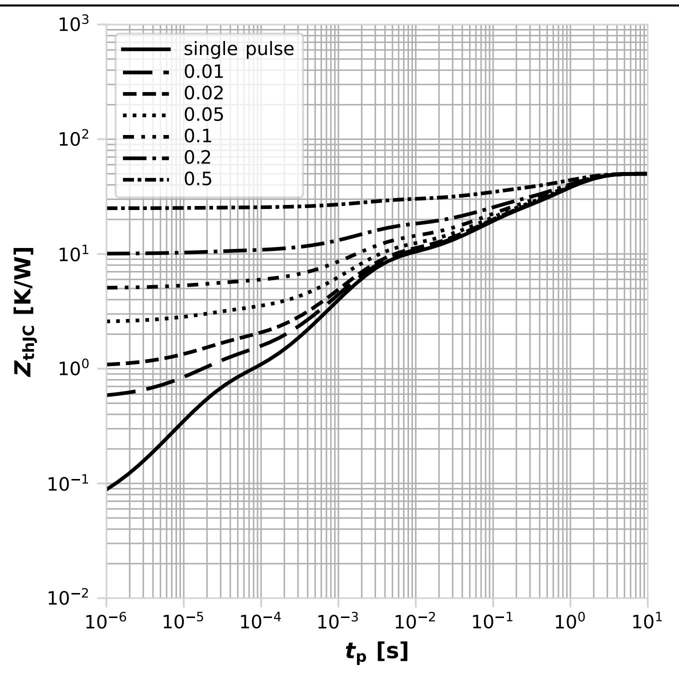

$I_D$=f($T_C$); $V_{GS}$≥10 V

**Diagram 3: Safe operating area**



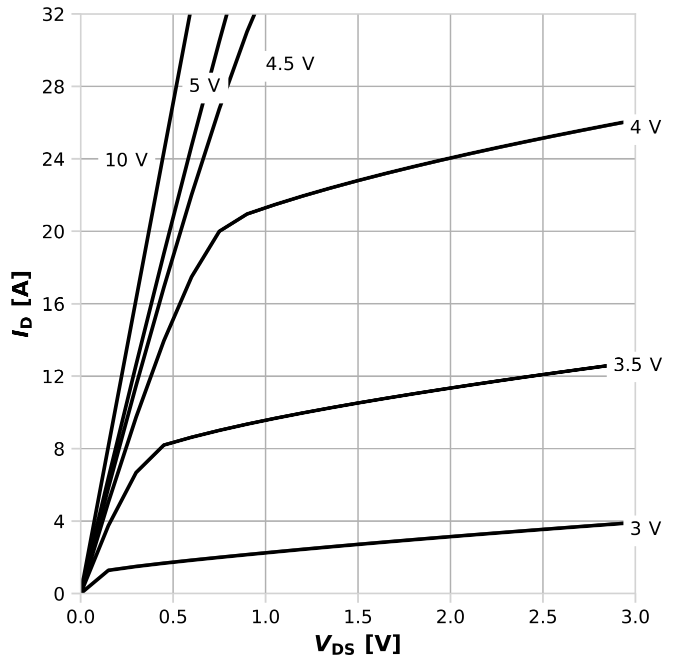

$I_D$=f($V_{DS}$); $T_C$=25 °C; $D$=0; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**



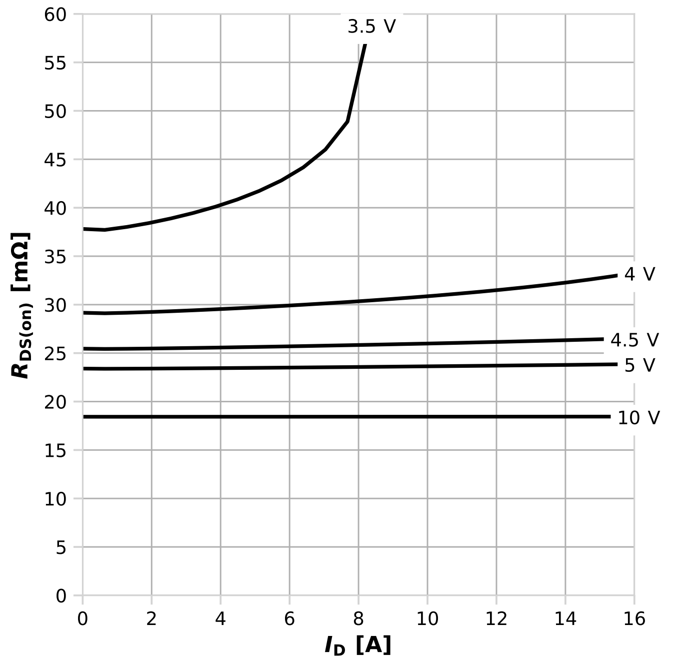

$Z_{thJC}$=f($t_p$); parameter: $D$=$t_p$/$T$

**Diagram 5: Typ. output characteristics**



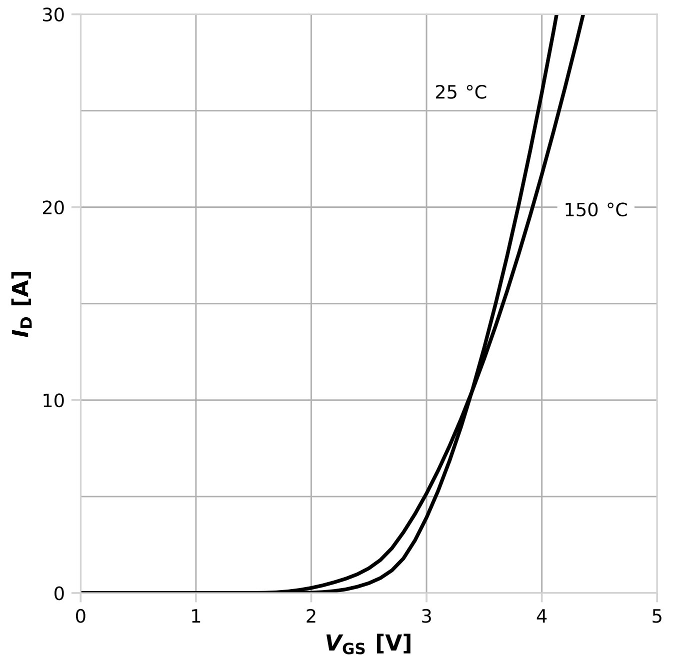

$I_D$=f($V_{DS}$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



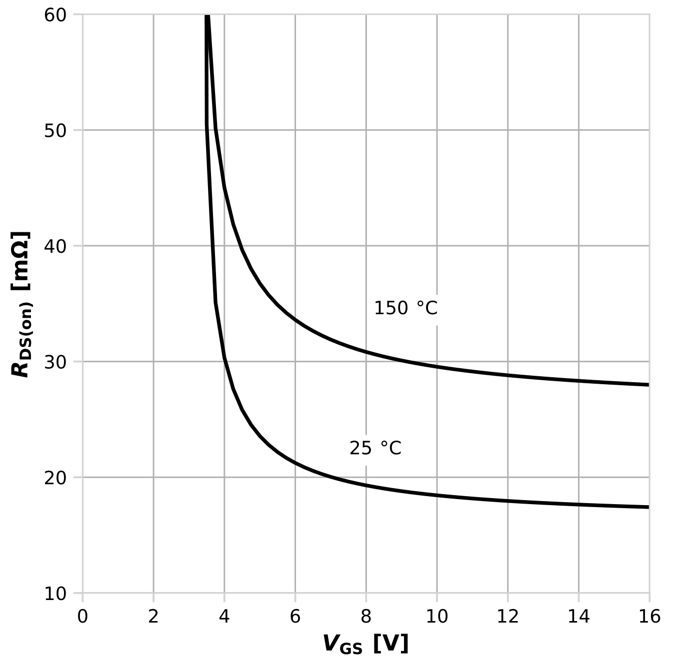

$R_{DS(on)}$=f($I_D$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**

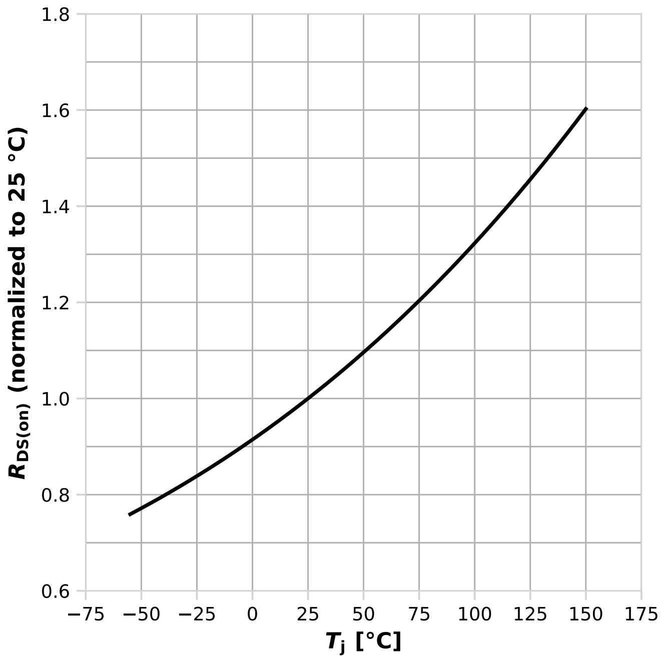
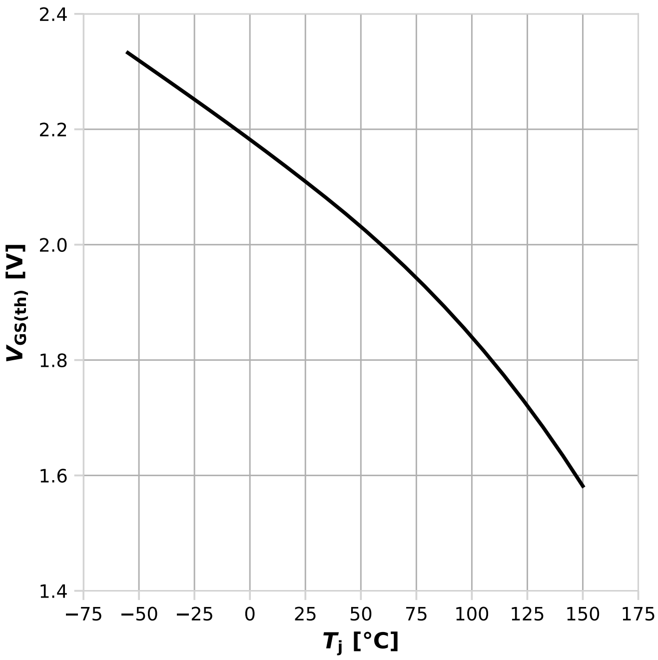



$I_D$=f($V_{GS}$), |$V_{DS}$|>2|$I_D$|$R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. drain-source on resistance**

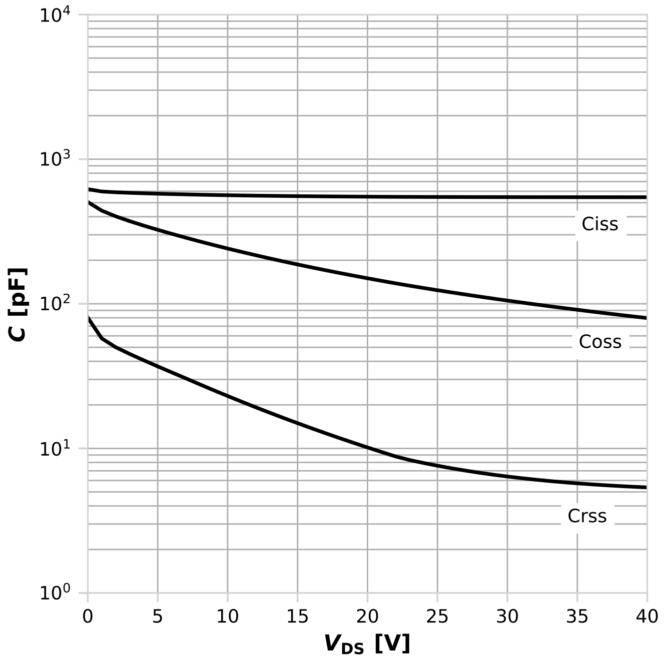
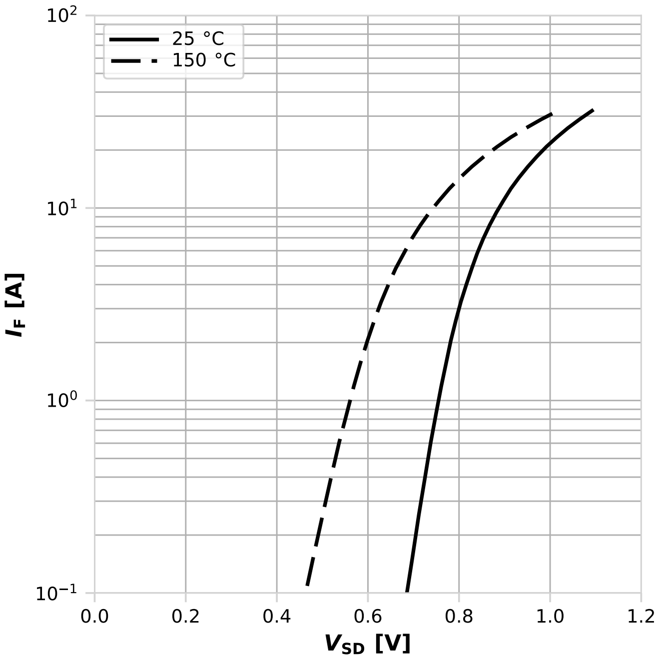


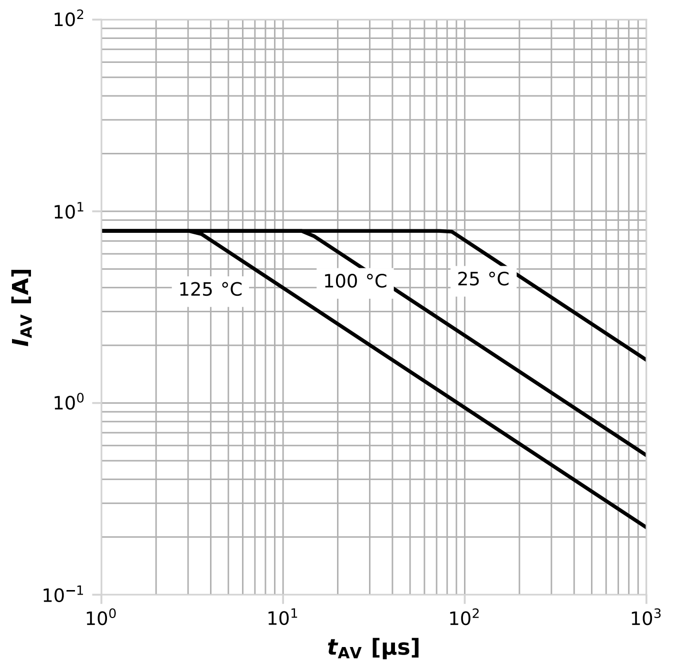
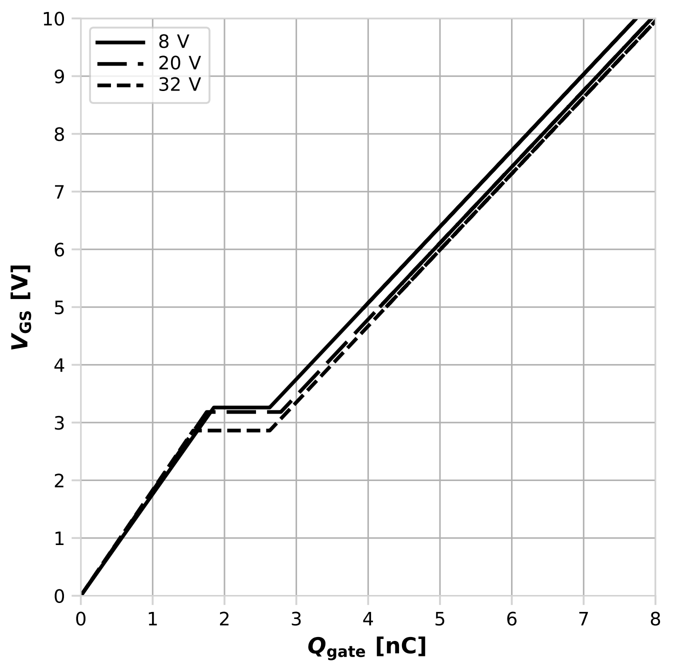

$R_{DS(on)}$=f($V_{GS}$), $I_D$=7.9 A; parameter: $T_j$

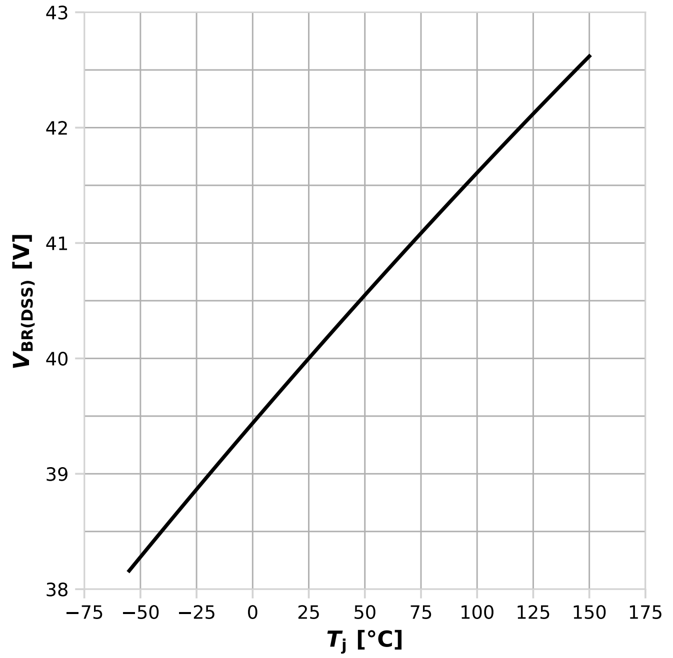
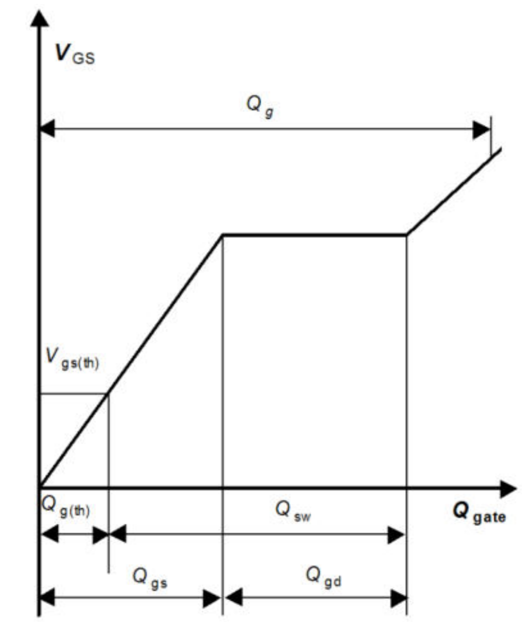
| Diagram 9: Normalized drain-source on resistance | Diagram 10: Typ. gate threshold voltage |
|---|---|
|  |  |
| $R_{DS(on)}$=f($T_j$), $I_D$=7.9 A, $V_{GS}$=10 V | $V_{GS(th)}$=f($T_j$), $V_{GS}$=$V_{DS}$; parameter: $I_D$=1000µA |



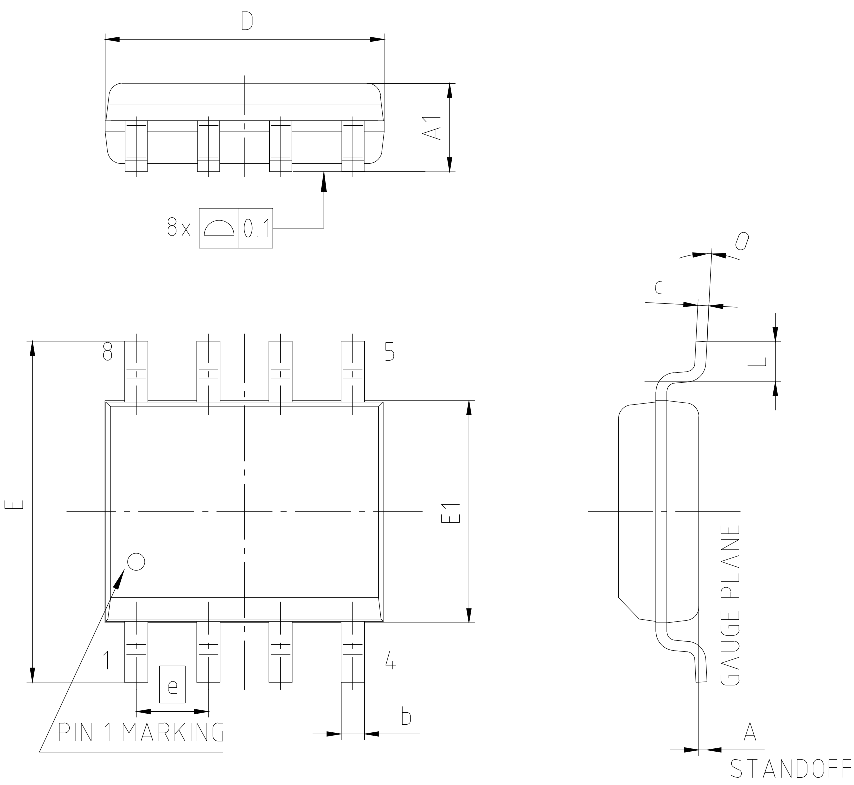


| Diagram 11: Typ. capacitances | Diagram 12: Forward characteristics of reverse diode |
|---|---|
|  |  |
| $C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz | $I_F$=f($V_{SD}$); parameter: $T_j$ |

| Diagram 13: Avalanche characteristics | Diagram 14: Typ. gate charge |
|---|---|
|   |   |
| $I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω; parameter: $T_{j,start}$ | $V_{GS}$=f($Q_{gate}$), $I_D$=7.9 A pulsed, $T_j$=25 °C; parameter: $V_{DD}$ |

| Diagram 15: Drain-source breakdown voltage | Gate charge waveforms |
|---|---|
|   |   |
| $V_{BR(DSS)}$=f($T_j$); $I_D$=1 mA | - |

# 5 Package Outlines




| PACKAGE - GROUP NUMBER: | PG-DSO-8-U02 | |
|---|---|---|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 0.18 | 0.25 |
| A1 | 1.35 | 1.75 |
| b | 0.38 | 0.51 |
| c | 0.254 | |
| D | 4.80 | 5.00 |
| E | 5.80 | 6.20 |
| E1 | 3.80 | 4.00 |
| e | 1.27 | |
| L | 0.48 | 0.91 |
| O | 4° | |
| N | 8 | |

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

**Figure 1 Outline PG-DSO-8, dimensions in mm**

## Revision History

ISA250250N04LMDS

### Revision 2024-10-02, Rev. 2.0

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 2.0 | 2024-10-02 | Release of final datasheet |

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**Published by**
**Infineon Technologies AG**
**81726 München, Germany**


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