

MOSFET
OptiMOS™ 6 Power-Transistor, 100 V

Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Optimized for high frequency switching and synchronous rectification
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

Product validation

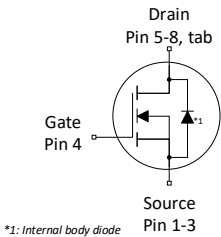
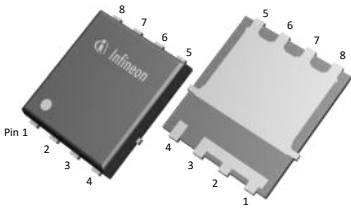
Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	8.05	mΩ
I_D	75	A
Q_{oss}	35	nC
$Q_G(0V...10V)$	19	nC
$Q_{rr}(100A/\mu s)$	31	nC

Type / Ordering code	Package	Marking	Related links
ISC080N10NM6	PG-TDSON-8	080N10N6	-

PG-TDSON-8



*1: Internal body diode

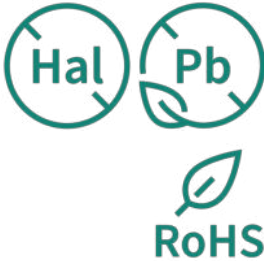




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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	75 53 48 13	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=8\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	300	A	$T_A=25\text{ °C}$
Avalanche current, single pulse ⁴⁾	I_{AS}	-	-	50	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	185	mJ	$I_D=11\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	100 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.77	1.5	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	
Thermal resistance, junction - ambient, 6 cm ² cooling area	R_{thJA}	-	-	50	°C/W	

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.3	2.8	3.3	V	$V_{DS}=V_{GS}$, $I_D=36\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1.0 100	μA	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$ ⁵⁾
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	7.1 8.7	8.05 10	m Ω	$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$ $V_{GS}=8\text{ V}$, $I_D=10\text{ A}$
Gate resistance	R_G	0.6	1.2	1.8	Ω	-
Transconductance	g_{fs}	15	30	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=20\text{ A}$

⁵⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1400	1800	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁶⁾	C_{oss}	-	310	390	pF	
Reverse transfer capacitance ⁶⁾	C_{rss}	-	9	13	pF	
Turn-on delay time	$t_{d(on)}$	-	6.4	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=10\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	1.5	-	ns	
Turn-off delay time	$t_{d(off)}$	-	10.7	-	ns	
Fall time	t_f	-	4.3	-	ns	

⁶⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge ⁸⁾	Q_{gs}	-	6.4	8.5	nC	$V_{DD}=50\text{ V}$, $I_D=10\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold ⁸⁾	$Q_{g(th)}$	-	3.9	4.9	nC	
Gate to drain charge ⁸⁾	Q_{gd}	-	3.4	5.1	nC	
Switching charge	Q_{sw}	-	5.9	-	nC	
Gate charge total ⁸⁾	Q_g	-	19	24	nC	
Gate plateau voltage	$V_{plateau}$	-	4.6	-	V	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	17	-	nC	
Output charge ⁸⁾	Q_{oss}	-	35	44	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	75	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	300	A	
Diode forward voltage	V_{SD}	-	0.82	1.0	V	$V_{GS}=0\text{ V}$, $I_F=20\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ⁹⁾	t_{rr}	-	31.5	47	ns	$V_R=50\text{ V}$, $I_F=10\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	31	46.5	nC	
Reverse recovery time ⁹⁾	t_{rr}	-	18	27	ns	$V_R=50\text{ V}$, $I_F=10\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	140	210	nC	

⁹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

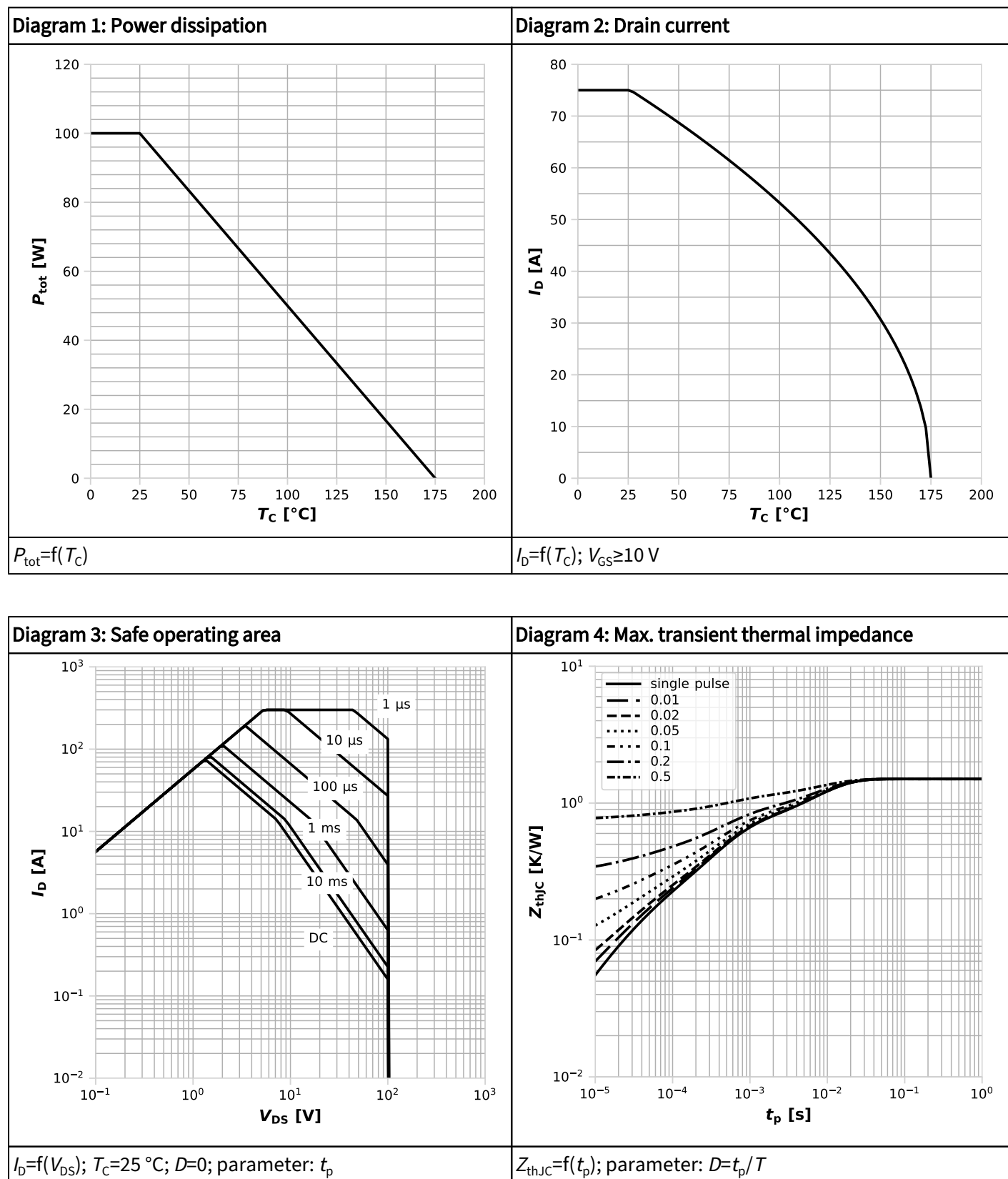
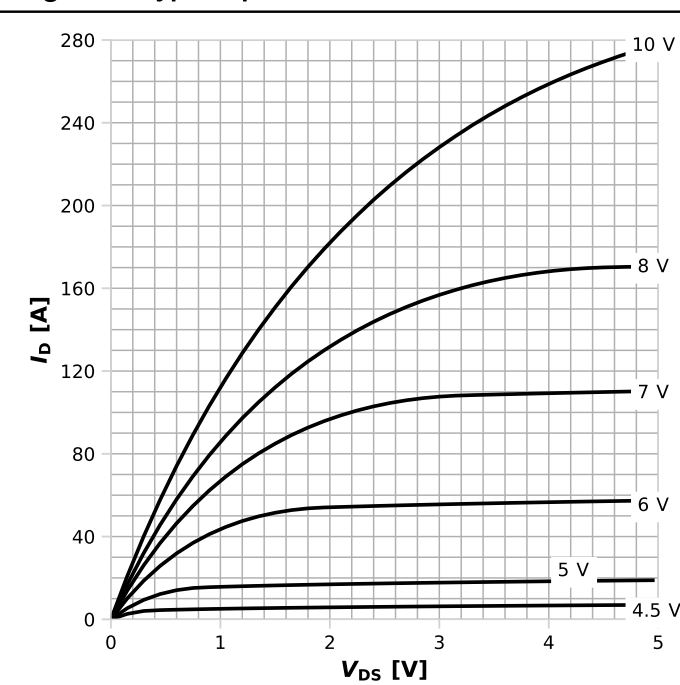
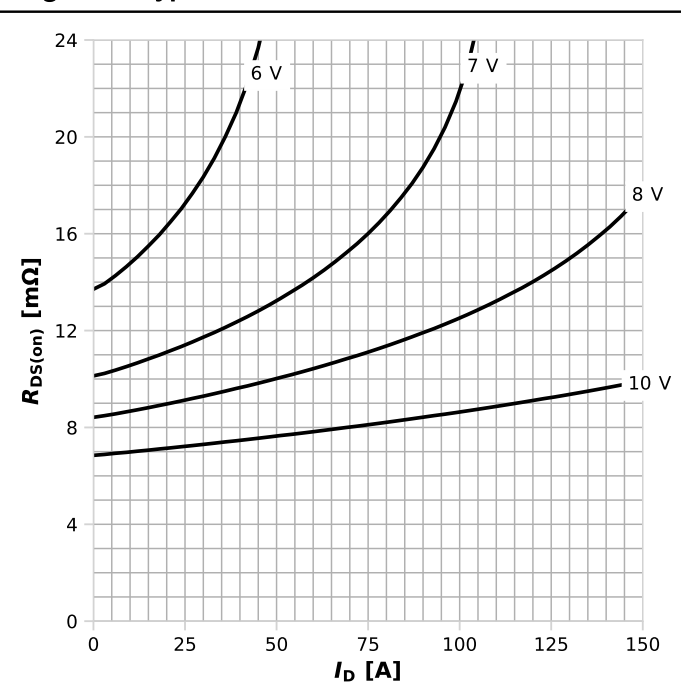


Diagram 5: Typ. output characteristics



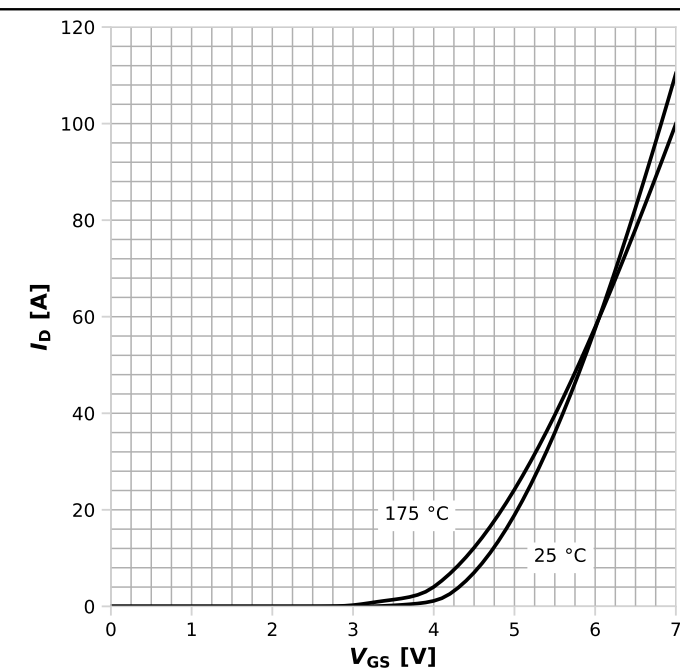
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



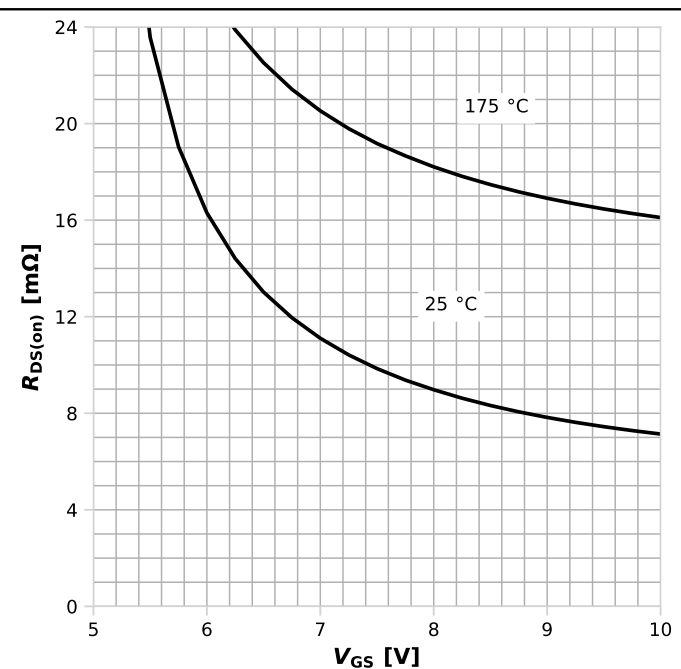
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



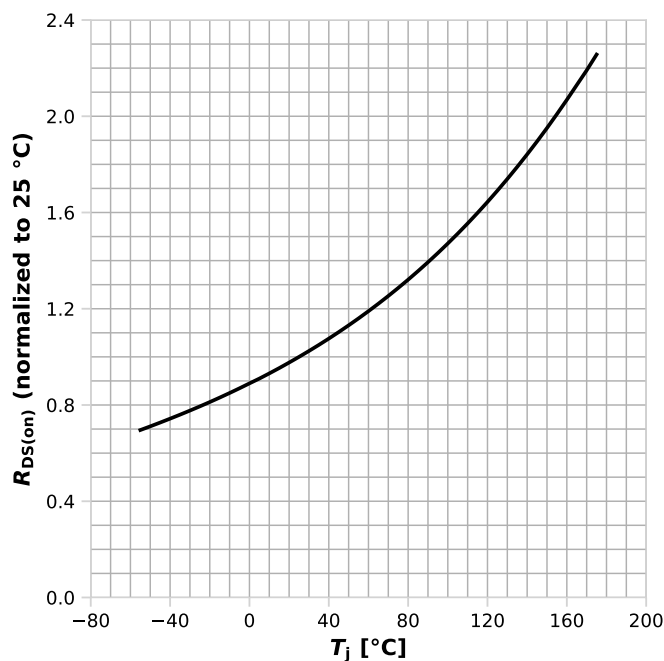
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)\max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



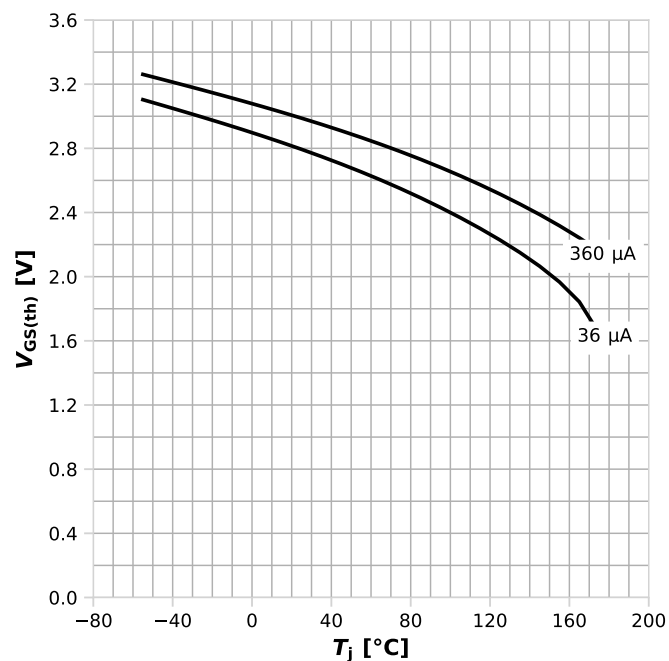
$R_{DS(on)} = f(V_{GS})$, $I_D = 20\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



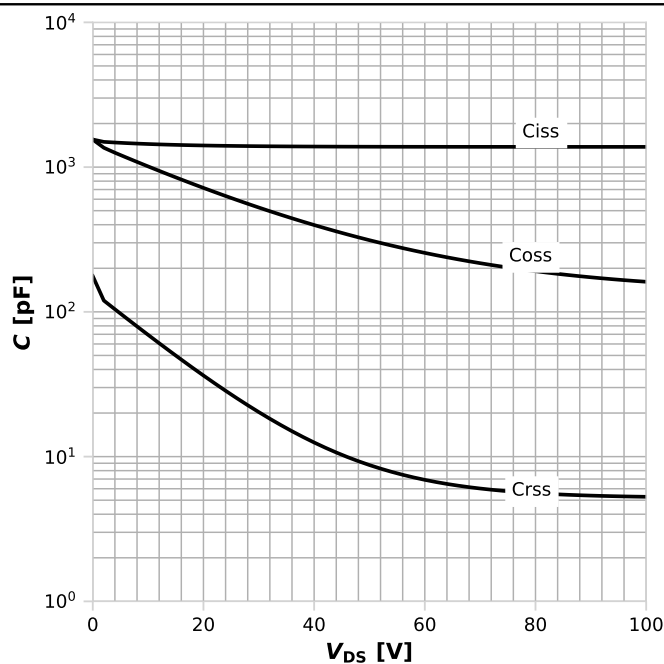
$$R_{DS(on)} = f(T_j), I_D = 20 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



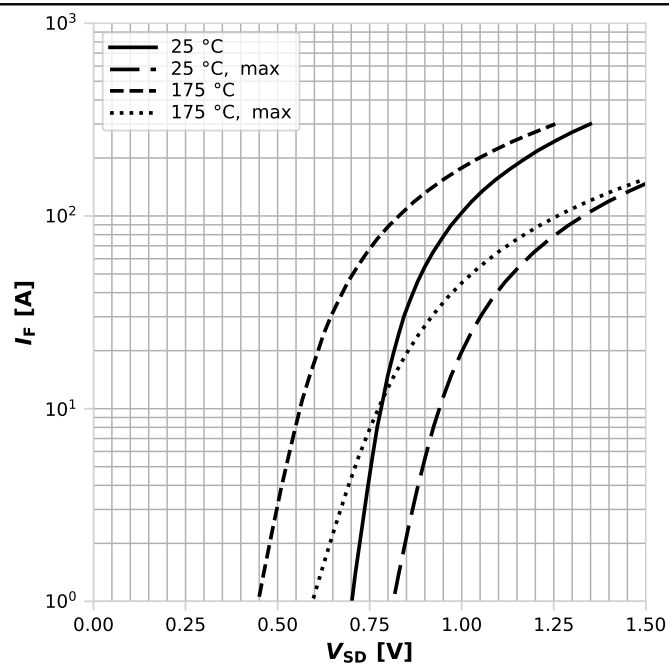
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances

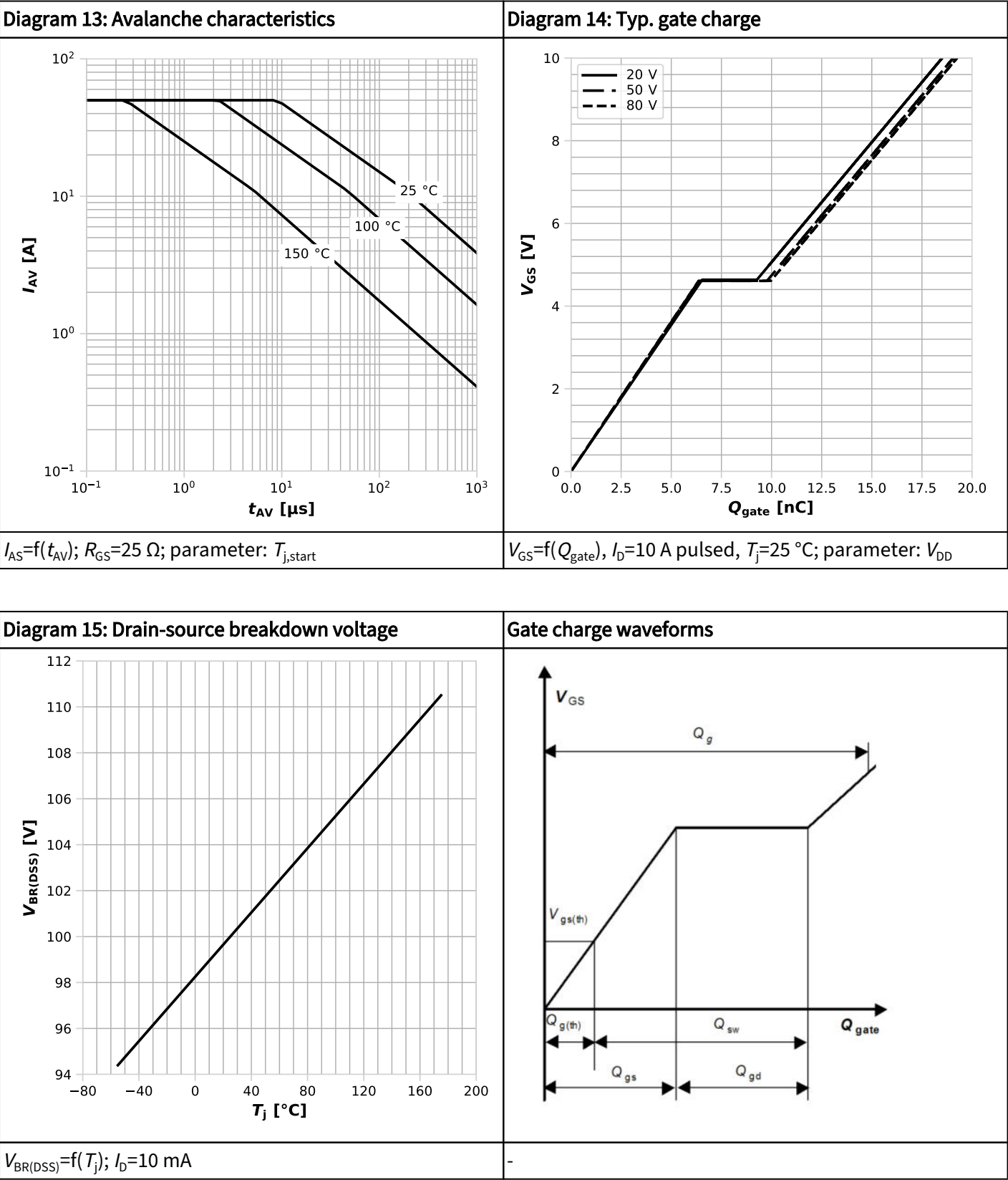


$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



$$I_F = f(V_{SD}); \text{ parameter: } T_j$$



5 Package outlines

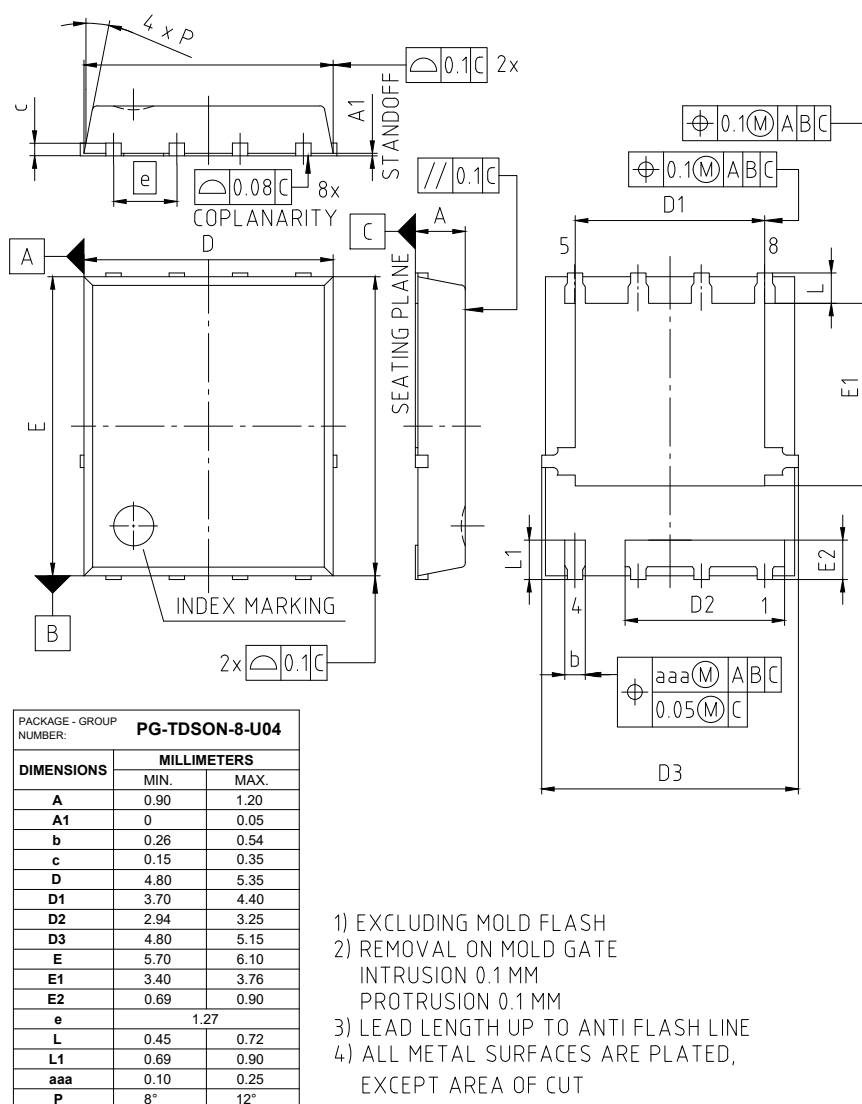


Figure 1 Outline PG-TDSON-8, dimensions in mm

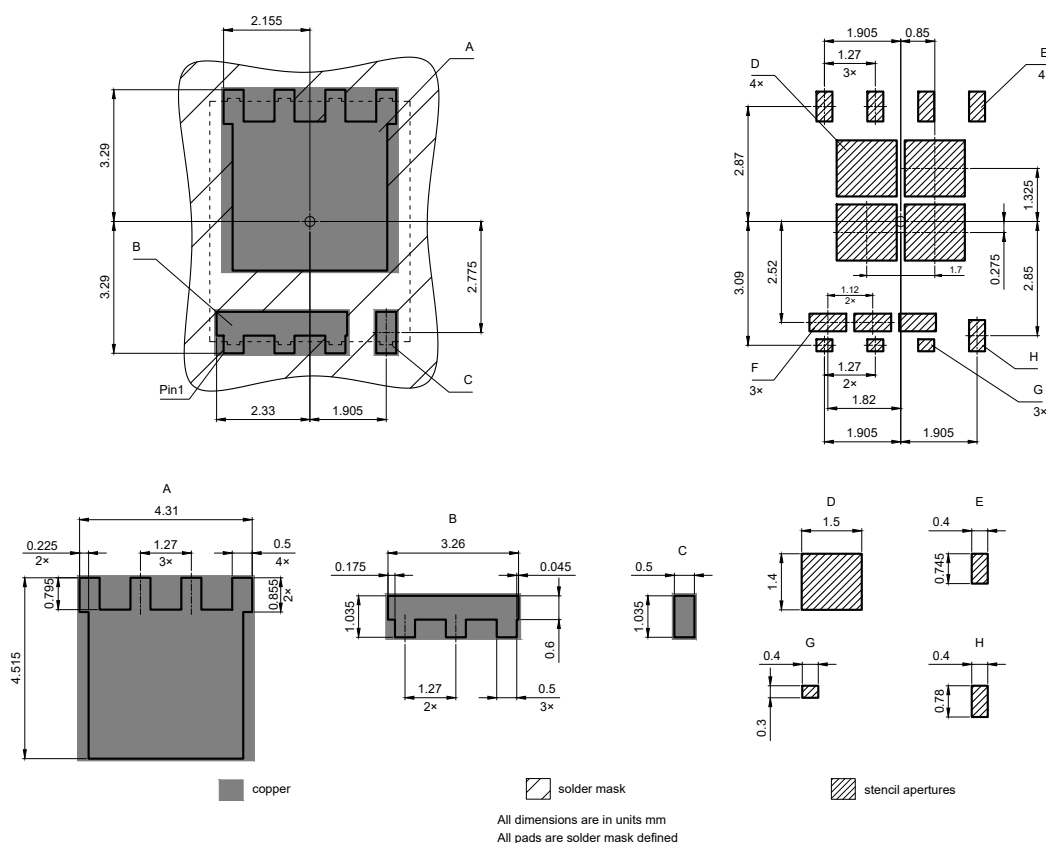


Figure 2 Footprint drawing PG-TDSON-8, dimensions in mm

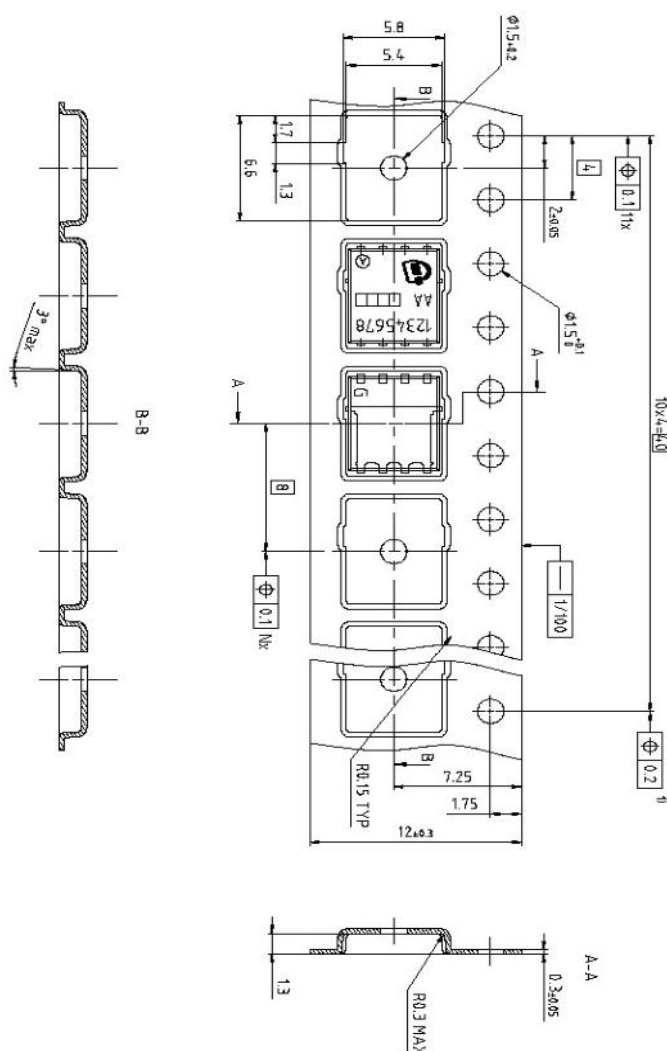


Figure 3 Packaging variant PG-TDSON-8, dimensions in mm

Revision history

ISC080N10NM6

Revision 2024-12-16, Rev. 2.3

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2021-07-05	Release of final version
2.1	2021-07-20	Update IAS
2.2	2023-02-07	Update SOA Diagram
2.3	2024-12-16	Update IAS

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