

MOSFET

OptiMOS™ 7 Power-Transistor, 15 V

Features

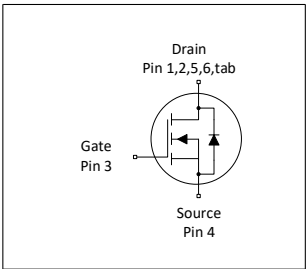
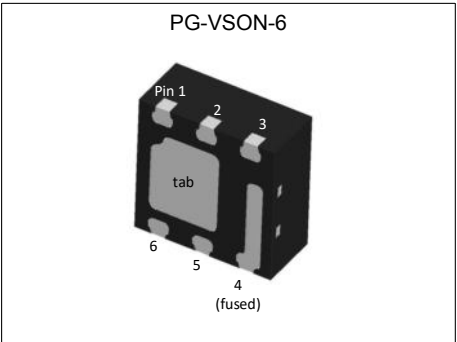
- N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Optimized for high performance SMPS, e.g. synchronous rectification

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	15	V
$R_{DS(on),max}$	1.8	$m\Omega$
I_D	129	A
Q_{oss}	6.7	nC
$Q_G (0V...4.5V)$	7.5	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
ISK018NE1LM7	PG-VSON-6	18E1	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	129 82 30	A	$V_{GS}=7\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=7\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=7\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	516	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	53	mJ	$I_D=20\text{ A}$, $R_{GS}=25\text{ }\Omega$
Recommended gate source voltage	V_{GS}	-7	-	7	V	-
Gate source voltage, transient	$V_{GS, AC}$	-8	-	8	V	$t_{pulse}<20\text{ ns}$
Power dissipation	P_{tot}	-	-	39 2.1	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}^{2)}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	1.6	3.2	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	60	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	15	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.0	V	$V_{DS}=V_{GS}$, $I_D=106\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1.0 100	μA	$V_{DS}=12\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=12\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=7\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.5 1.9	1.8 2.15	m Ω	$V_{GS}=7\text{ V}$, $I_D=20\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=20\text{ A}$
Gate resistance	R_G	-	0.5	-	Ω	-
Transconductance	g_{fs}	46	92	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=20\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	1200	1600	pF	$V_{GS}=0\text{ V}$, $V_{DS}=7.5\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	620	810	pF	$V_{GS}=0\text{ V}$, $V_{DS}=7.5\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	68	120	pF	$V_{GS}=0\text{ V}$, $V_{DS}=7.5\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	5	-	ns	$V_{DD}=7.5\text{ V}$, $V_{GS}=7\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	1	-	ns	$V_{DD}=7.5\text{ V}$, $V_{GS}=7\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	10	-	ns	$V_{DD}=7.5\text{ V}$, $V_{GS}=7\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	2	-	ns	$V_{DD}=7.5\text{ V}$, $V_{GS}=7\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3.6	5.2	nC	$V_{DD}=7.5\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	1.9	2.8	nC	$V_{DD}=7.5\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	1.5	2.2	nC	$V_{DD}=7.5\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	3.1	-	nC	$V_{DD}=7.5\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	7.5	9.0	nC	$V_{DD}=7.5\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.9	-	V	$V_{DD}=7.5\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	11.3	13.6	nC	$V_{DD}=7.5\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }7\text{ V}$
Output charge ¹⁾	Q_{oss}	-	6.7	8.9	nC	$V_{DS}=7.5\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

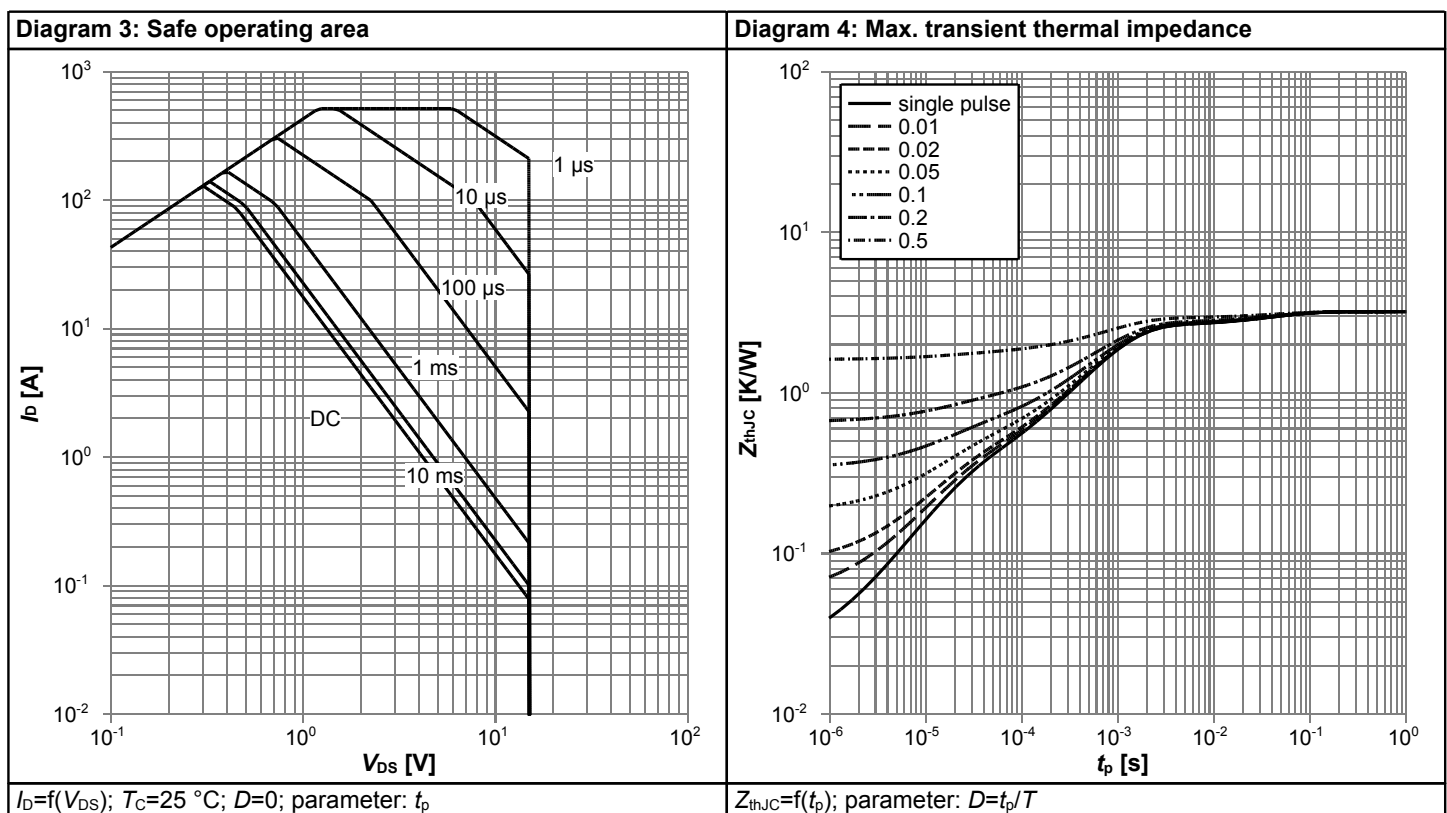
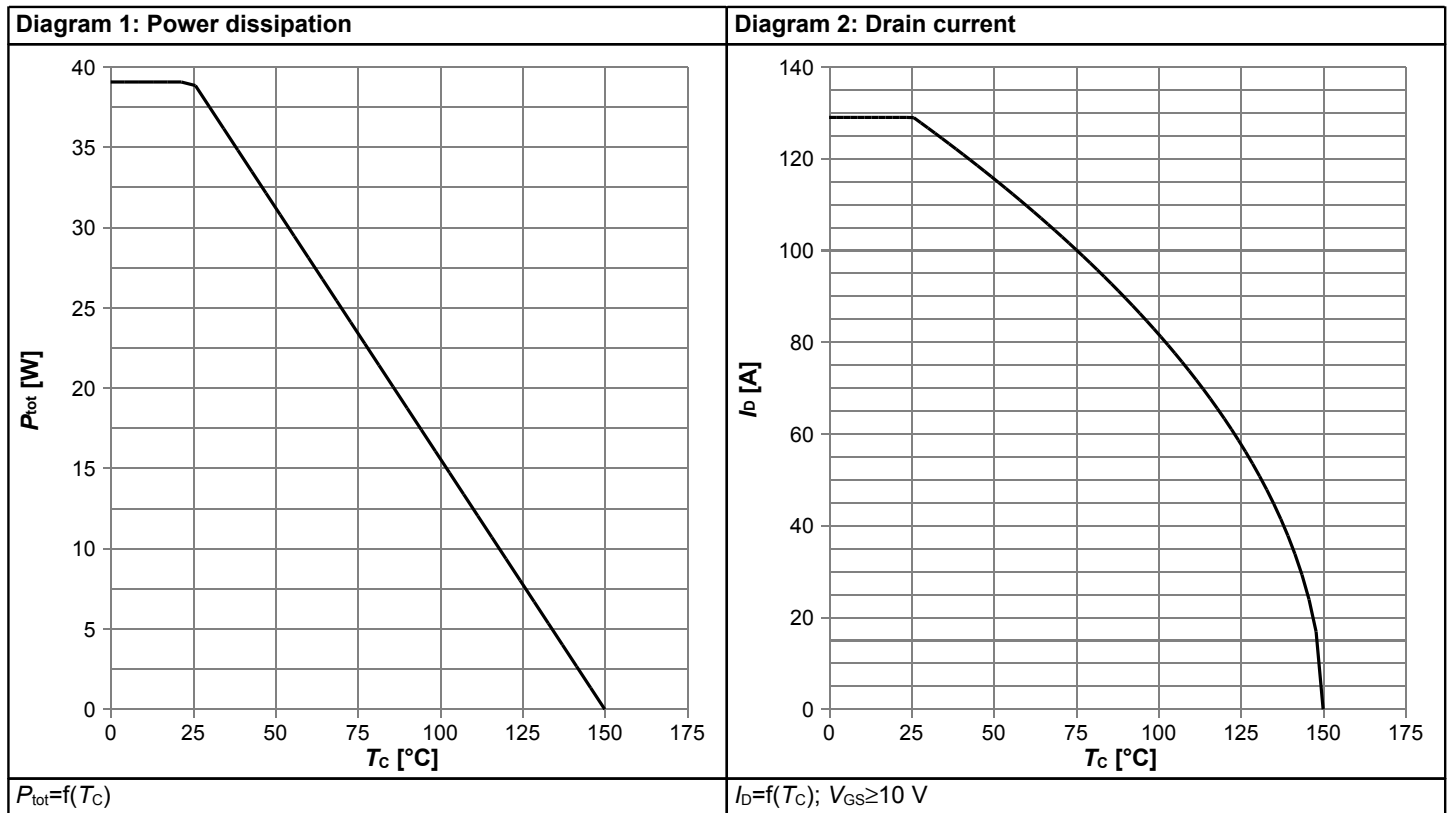
²⁾ See figure 16 for gate charge parameter definition.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	40	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	516	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.79	1.0	V	$V_{GS}=0\text{ V}$, $I_F=20\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	16	32	ns	$V_R=7.5\text{ V}$, $I_F=20\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	8	16	nC	$V_R=7.5\text{ V}$, $I_F=20\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery time ¹⁾	t_{rr}	-	14	28	ns	$V_R=7.5\text{ V}$, $I_F=20\text{ A}$, $di_F/dt=300\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	15	30	nC	$V_R=7.5\text{ V}$, $I_F=20\text{ A}$, $di_F/dt=300\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

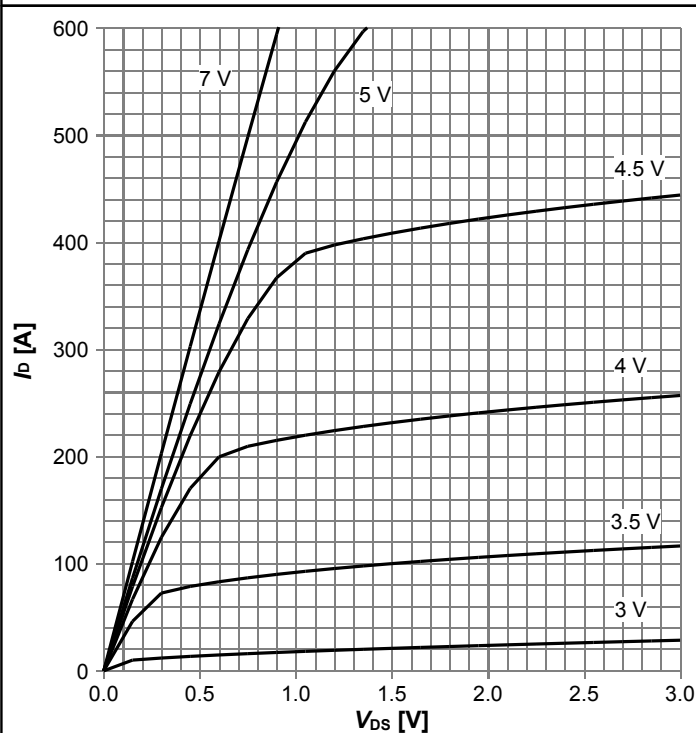
4 Electrical characteristics diagrams



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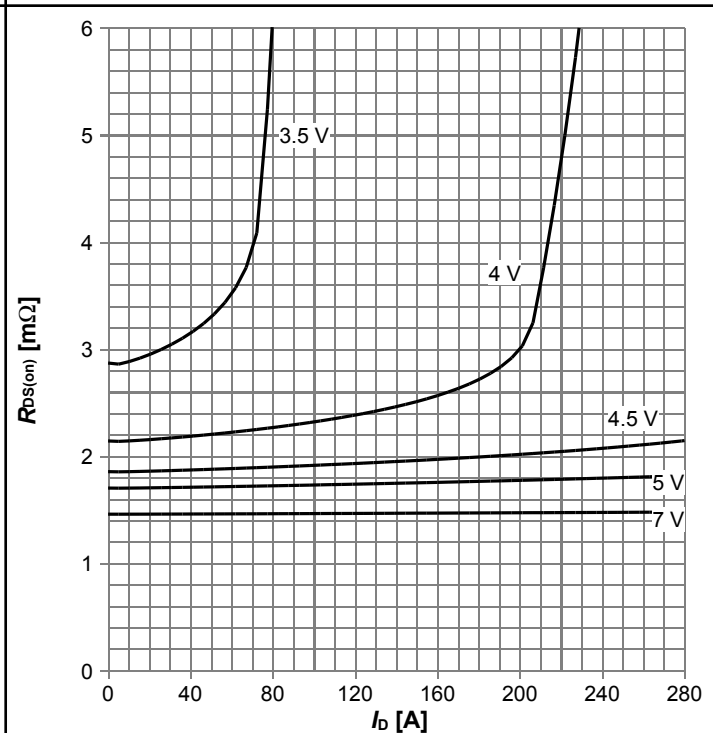
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Diagram 5: Typ. output characteristics



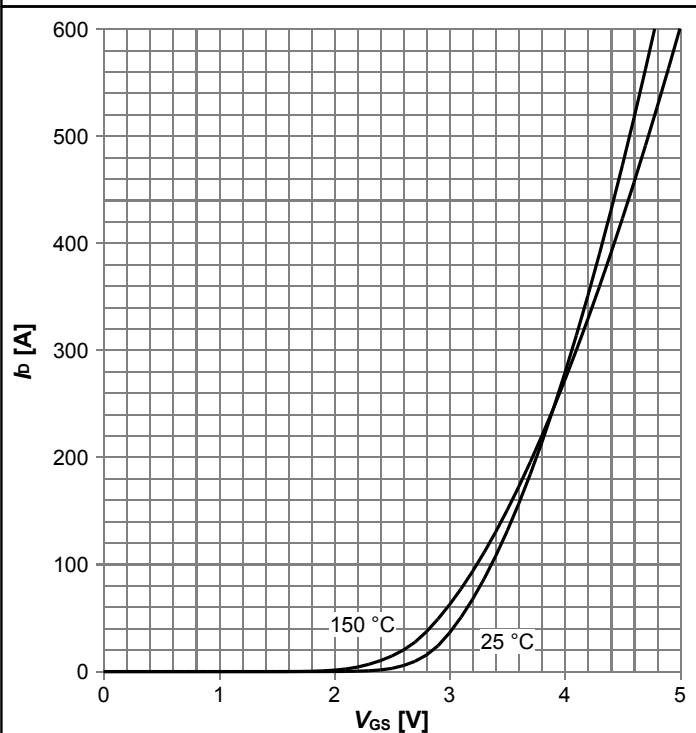
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



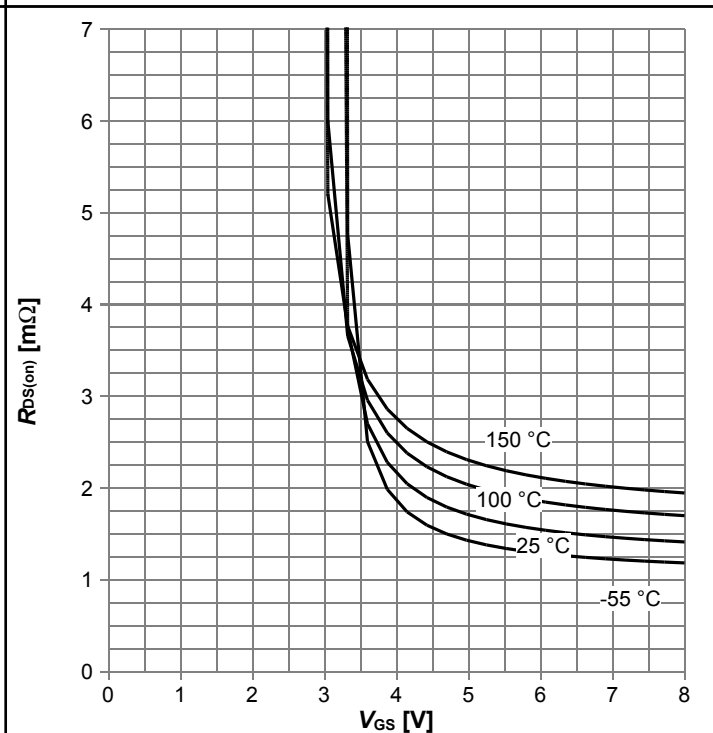
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



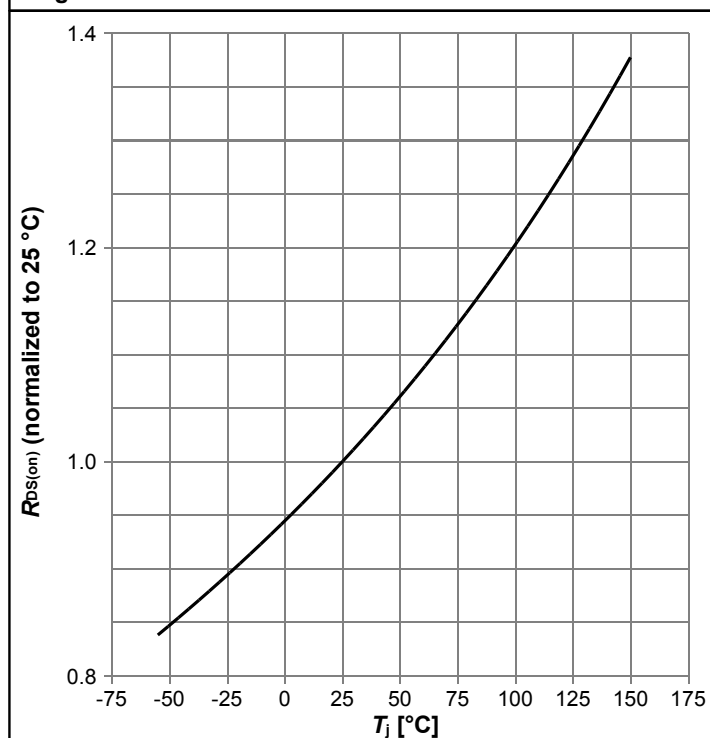
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



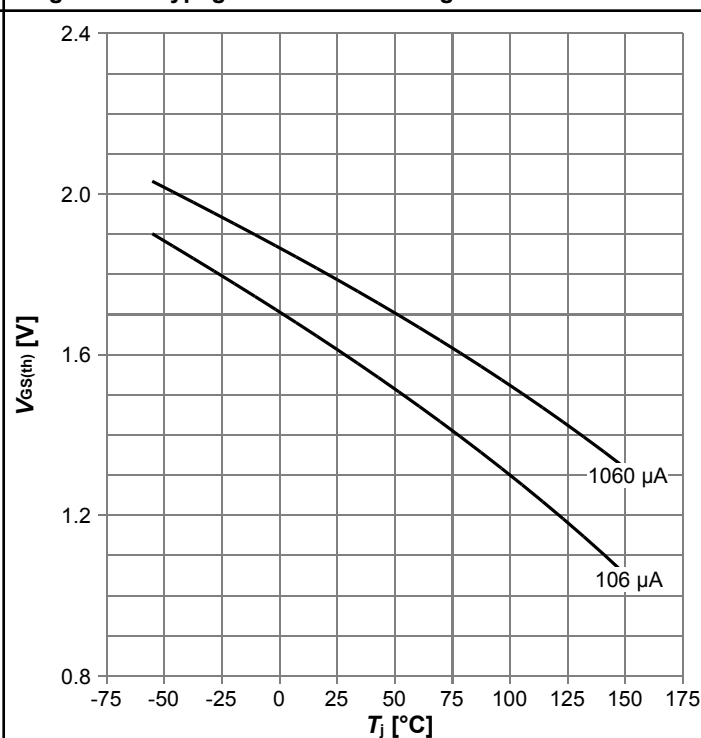
$R_{DS(on)} = f(V_{GS})$, $I_D = 20\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



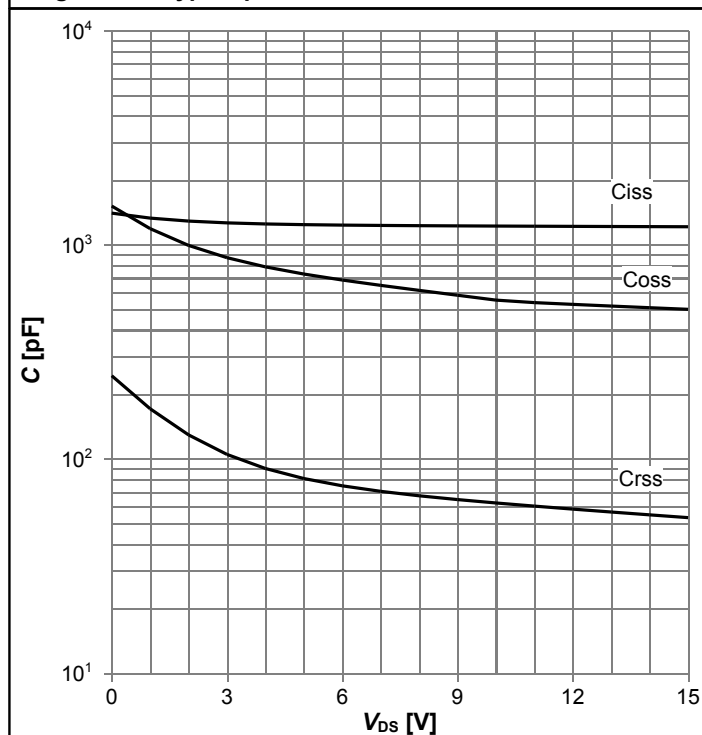
$R_{DS(on)} = f(T_j)$, $I_D = 20$ A, $V_{GS} = 8$ V

Diagram 10: Typ. gate threshold voltage



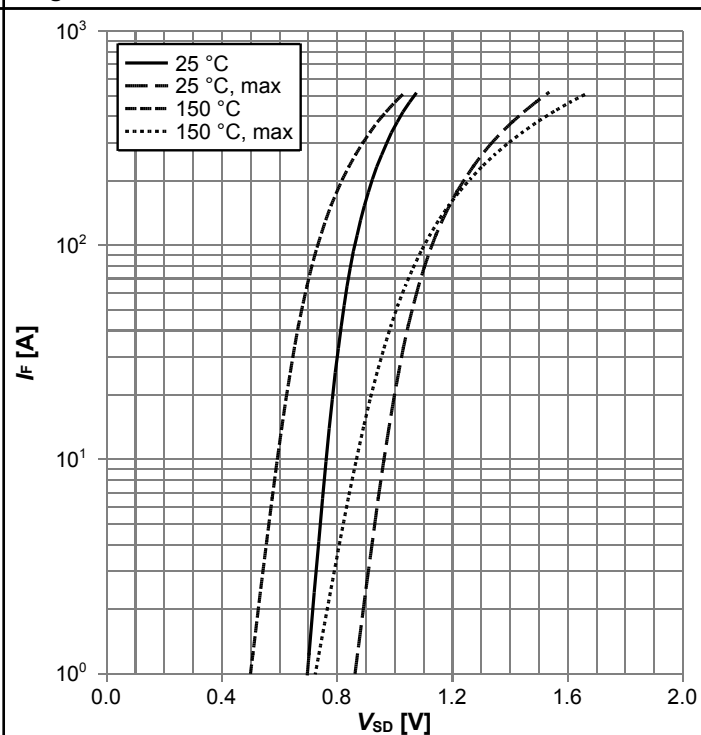
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



$I_F = f(V_{SD})$; parameter: T_j

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Diagram 13: Avalanche characteristics

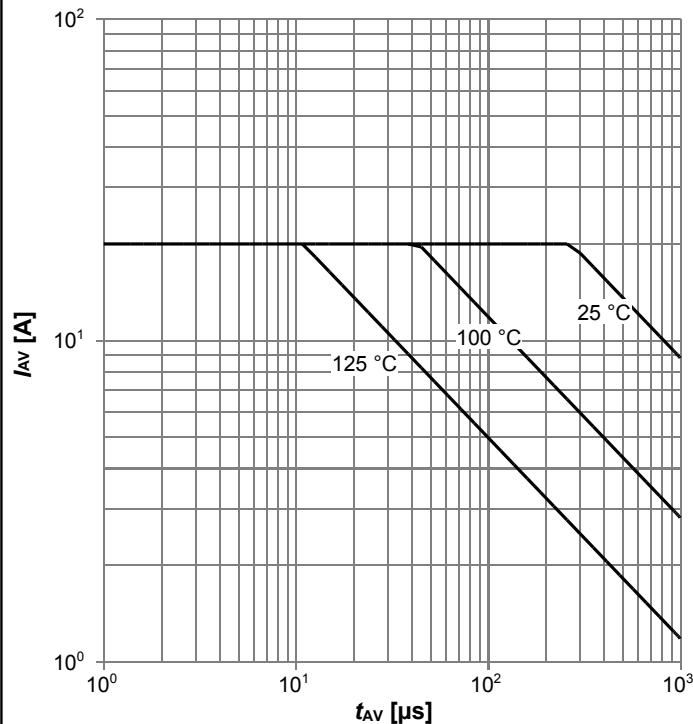


Diagram 14: Typ. gate charge

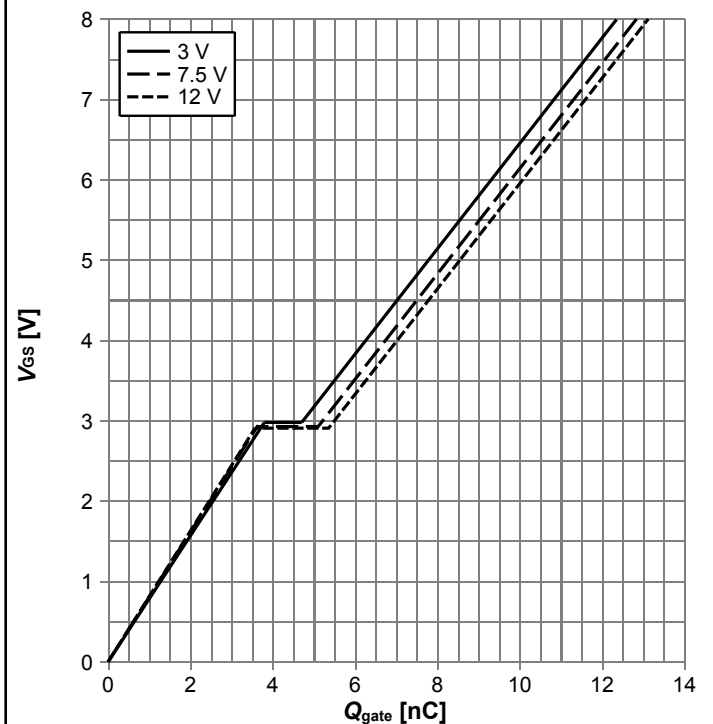


Diagram 15: Min. drain-source breakdown voltage

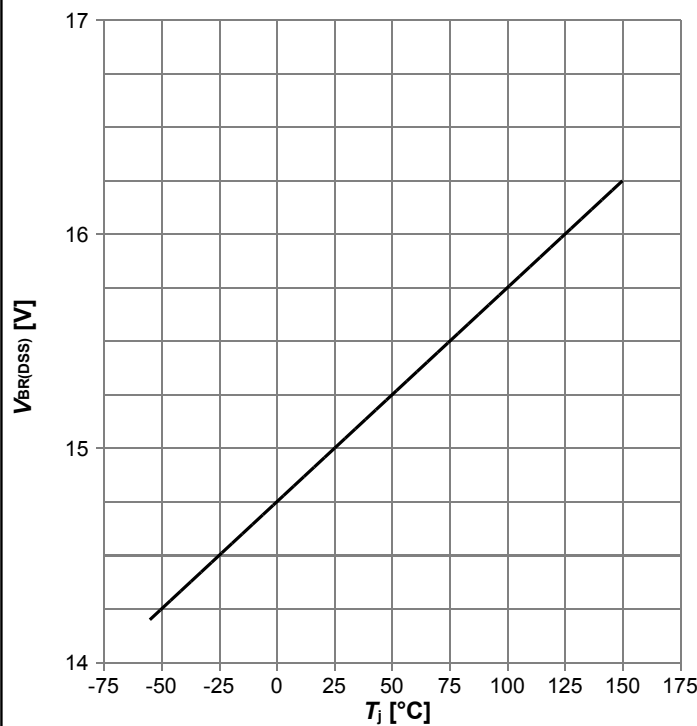
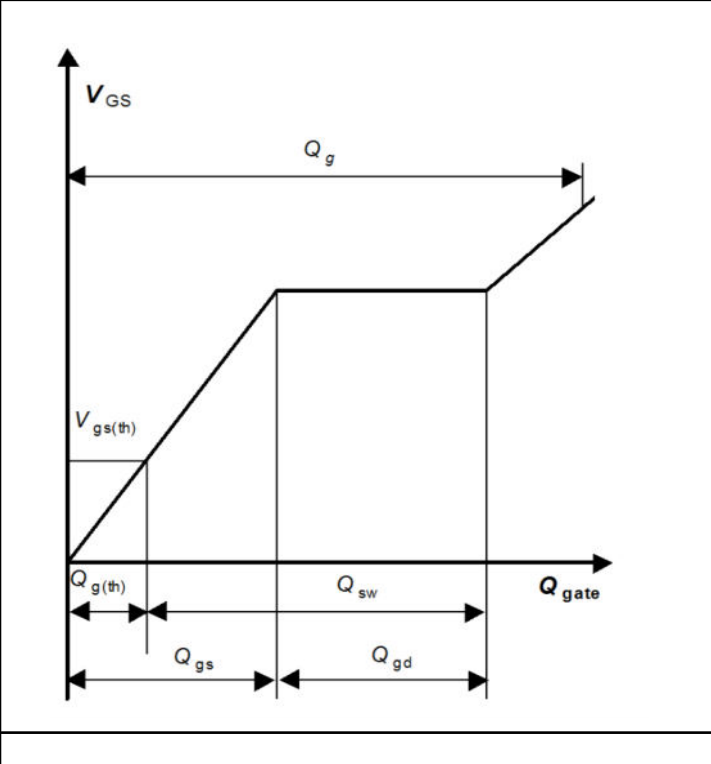
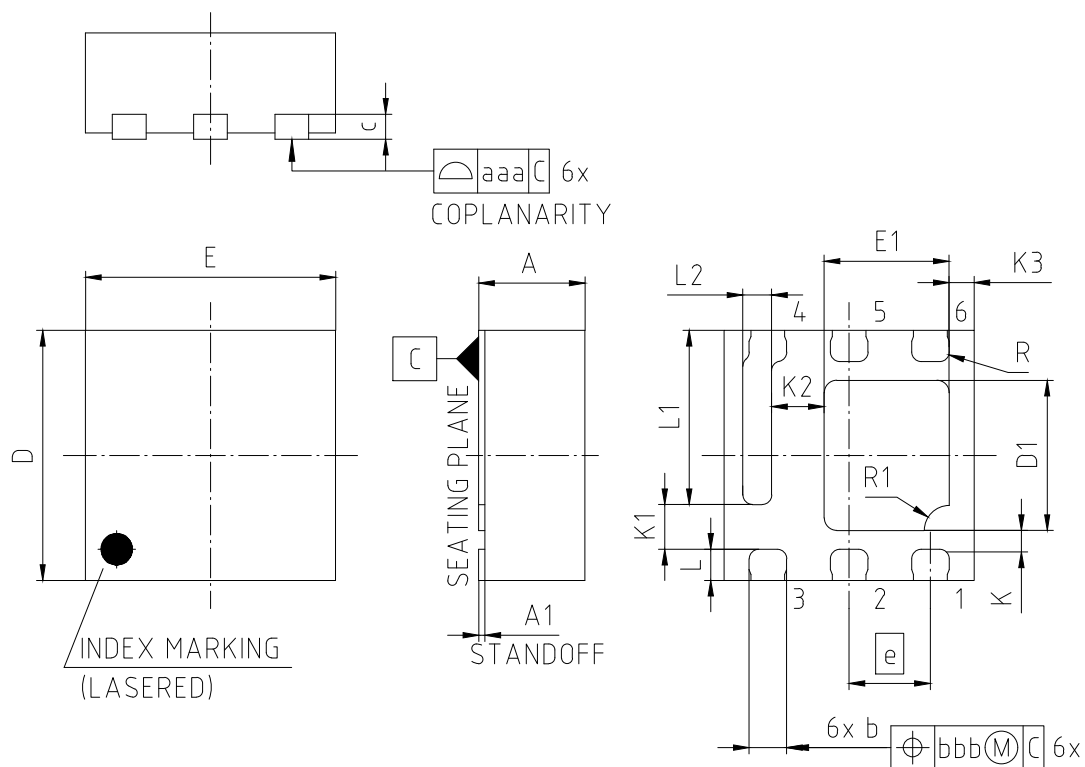


Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER: PG-VSON-6-U02					
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	---	0.90	L	0.20	0.30
A1	---	0.05	L1	1.29	1.49
b	0.20	0.40	L2	0.13	0.33
c	(0.20)		R	(0.08)	
D	1.90	2.10	R1	(0.20)	
D1	1.10	1.30	N	6	
E	1.90	2.10	aaa	0.08	
E1	0.90	1.10	bbb	0.10	
e	0.65				
K	0.05	---			
K1	0.26	---			
K2	0.42	---			
K3	0.10	0.30			

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-VSON-6, dimensions in mm

Revision History

ISK018NE1LM7

Revision: 2023-09-25, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2023-06-21	Release of final version
2.1	2023-09-25	Update Id for Vgs(th)

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