IGBT

TRENCHSTOP^{TM} IGBT3 Chip

SIGC109T120R3E

Data Sheet

Industrial Power Control

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SIGC109T120R3E

TRENCHSTOP™ IGBT3 Chip

Features:

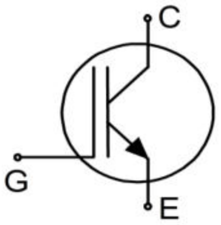
- 1200V trench & field stop technology
- Low turn-off losses
- Short tail current
- Positive temperature coefficient
- Easy paralleling

Recommended for:

- Power modules

Applications:

- Drives



Chip Type	V_{CE}	I_{Cn} [1]	Die Size	Package
SIGC109T120R3E	1200V	100A	10.47mm x 10.44mm	Sawn on foil

Mechanical Parameters

Die size		10.47 x 10.44	mm^2
Emitter pad size		See chip drawing	
Gate pad size		1.319 x 0.820	
Area total		109.31	
Thickness		140	µm
Wafer size		200	mm
Maximum possible chips per wafer		222	
Passivation frontside		Photoimide	
Pad metal		3200nm AlSiCu	
Backside metal		Ni Ag – system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process	
Die bond		Electrically conductive epoxy glue and soft solder	
Wire bond		Al, ≤500µm	
Reject ink dot size		∅ 0.65mm; max. 1.2mm	
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C, <6 months	
	for open MBB bags	Acc. to IEC62258-3: atmosphere >99% Nitrogen or inert gas, humidity <25%RH, temperature 17°C – 25°C, <6 months	

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[1] Nominal collector current at T_C=100°C for chip packaged in power modules, see application example cited on page 5.

Maximum Ratings

Parameter	**Symbol**	**Value**	**Unit**
Collector-emitter voltage, T_{vj}=25°C	V_{CE}	1200	V
DC collector current, limited by $T_{vj\ max}$ [2]	I_C	-	A
Pulsed collector current, t_p limited by $T_{vj\ max}$ [3]	$I_{C,puls}$	300	A
Gate-emitter voltage	V_{GE}	±20	V
Junction temperature range	T_{vj}	-55 ... +175	°C
Operating junction temperature	T_{vj}	-55 ... +150	°C
Short circuit data [3 / 4] V_{GE}=15V, V_{CC}=900V, T_{vj}=125°C	t_{sc}	10	µs
Reverse bias safe operating area [3] (RBSOA)	$I_{C,max}$=200A, $V_{CE,max}$=1200V, T_{vj}≤125°C		

Static Characteristics (tested on wafer), T_{vj}=25°C

Parameter	**Symbol**	**Conditions**	**Value**			**Unit**
			min.	**typ.**	**max.**	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V, I_C=4mA	1200	-	-	V
Collector-emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=100A	1.4	1.7	2.1	
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C=4mA, V_{GE}=V_{CE}	5.0	5.8	6.5	
Zero gate voltage collector current	I_{CES}	V_{CE}=1200V, V_{GE}=0V	-	-	13.4	µA
Gate-emitter leakage current	I_{GES}	V_{CE}=0V, V_{GE}=20V	-	-	600	nA
Integrated gate resistor	r_G			7.5		Ω

Electrical Characteristics [3]

Parameter	**Symbol**	**Conditions**	**Value**			**Unit**
			min.	**typ.**	**max.**	
Collector-emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=100A, T_{vj}=125°C	-	2.0	-	V
Input capacitance	C_{ies}	V_{CE}=25V, V_{GE}=0V, f=1MHz T_{vj}=25°C	-	7210	-	pF
Reverse transfer capacitance	C_{res}		-	327	-	

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[2] Depending on thermal properties of assembly.

[3] Not subject to production test - verified by design/characterization.

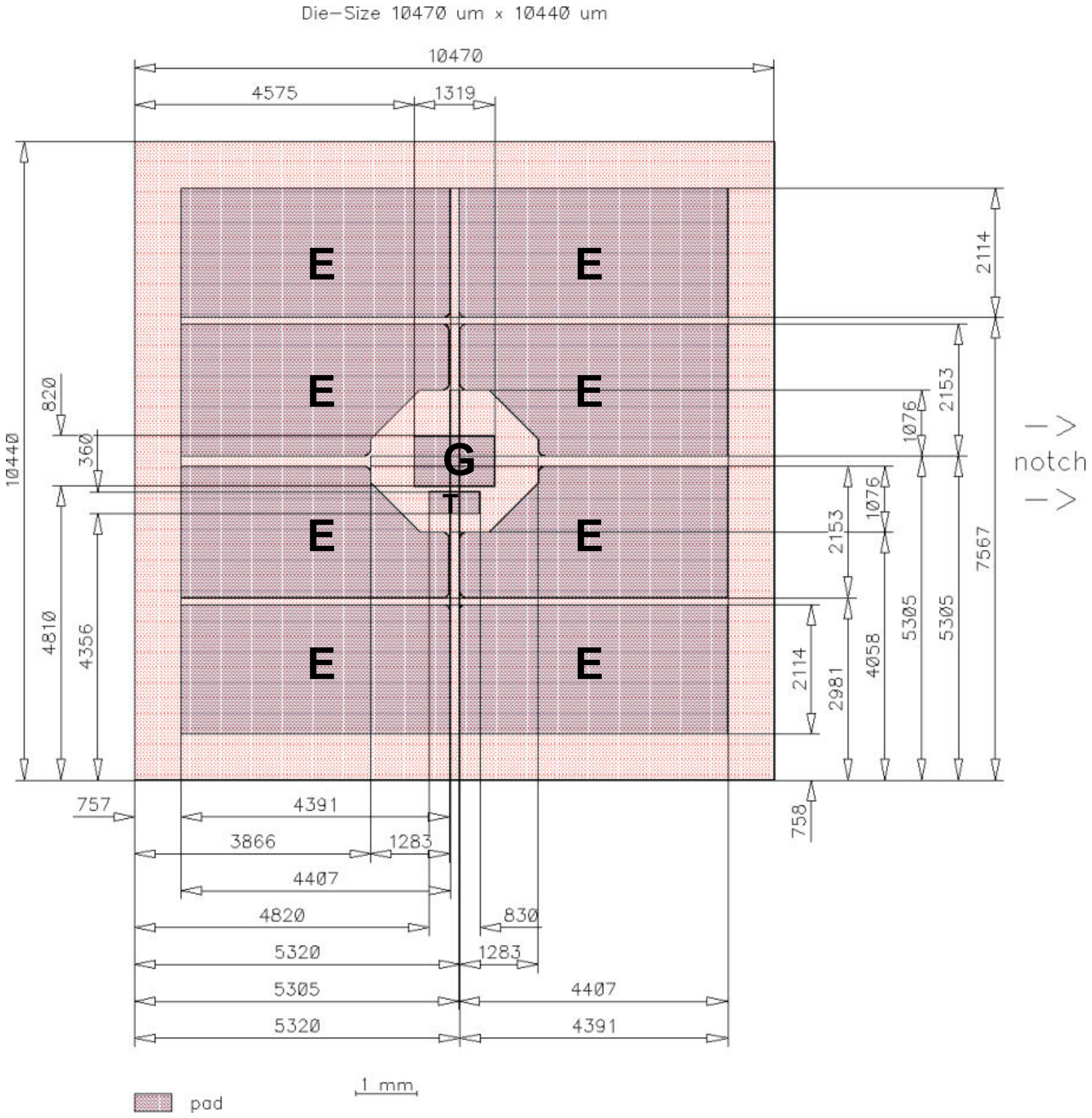
[4] Allowed number of short circuits: <1000; time between short circuits: >1s.

Further Electrical Characteristics

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

Application example	FS100R12KE3	Rev. 3.1

Chip Drawing



E = Emitter
G = Gate
T = Test pad do not contact

Bare Die Product Specifics
Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

Description

AQL 0.65 for visual inspection according to failure catalogue
Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision History

Revision	Subjects (major changes since last revision)	Date
2.0	Release of final datasheet, change wafer size to 200mm	30.04.2010
2.1	Additional basic types L7688M, L7688T, L7688E; new gate pad design	01.07.2014
2.2	Minor changes, chip drawing	06.02.2015
2.3	Update disclaimer	19.08.2015

Relevant Application Notes

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