

A large, stylized white arc graphic that starts from the left, curves upwards and to the right, and then curves back down towards the left, resembling a partial circle or a stylized 'C' shape.

IGBT

TRENCHSTOP™ IGBT3 Chip  
SIGC41T120R3LE

Data Sheet

Industrial Power Control

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# SIGC41T120R3LE

## TRENCHSTOP™ IGBT3 Chip

### Features:

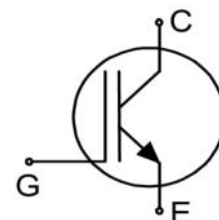
- 1200V trench & field stop technology
- Low turn-off losses
- Short tail current
- Positive temperature coefficient
- Easy paralleling

### Recommended for:

- Power modules

### Applications:

- Drives



Chip Type	$V_{CE}$	$I_{Cn}^1$	Die Size	Package
SIGC41T120R3LE	1200V	40A	6.5mm x 6.37mm	Sawn on foil

### Mechanical Parameters

Die size		6.5 x 6.37	mm <sup>2</sup>
Emitter pad size		See chip drawing	
Gate pad size		1.139 x 1.139	
Area total		41.405	
Thickness		120	µm
Wafer size		200	mm
Maximum possible chips per wafer		640	
Passivation frontside		Photoimide	
Pad metal		3200nm AlSiCu	
Backside metal		Ni Ag – system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process	
Die bond		Electrically conductive epoxy glue and soft solder	
Wire bond		Al, ≤500µm	
Reject ink dot size		Ø 0.65mm; max. 1.2mm	
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C, <6 months	
	for open MBB bags	Acc. to IEC62258-3: atmosphere >99% Nitrogen or inert gas, humidity <25%RH, temperature 17°C – 25°C, <6 months	

<sup>1</sup> Nominal collector current at  $T_C=100^\circ\text{C}$  for chip packaged in TO packages, see application example cited on page 5.

## Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj}=25^{\circ}\text{C}$	$V_{CE}$	1200	V
DC collector current, limited by $T_{vj\text{ max}}^2$	$I_C$	-	A
Pulsed collector current, $t_p$ limited by $T_{vj\text{ max}}^3$	$I_{C,puls}$	105	A
Gate-emitter voltage	$V_{GE}$	$\pm 20$	V
Junction temperature range	$T_{vj}$	$-55 \dots +175$	$^{\circ}\text{C}$
Operating junction temperature	$T_{vj}$	$-55 \dots +150$	$^{\circ}\text{C}$
Short circuit data <sup>3/4</sup> $V_{GE}=15\text{V}$ , $V_{CC}=900\text{V}$ , $T_{vj}=125^{\circ}\text{C}$	$t_{sc}$	10	$\mu\text{s}$
Reverse bias safe operating area <sup>3</sup> (RBSOA)	$I_{C,max}=80\text{A}$ , $V_{CE,max}=1200\text{V}$ , $T_{vj}\leq 125^{\circ}\text{C}$		

## Static Characteristics (tested on wafer), $T_{vj}=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$ , $I_C=1.5\text{mA}$	1200	-	-	V
Collector-emitter saturation voltage	$V_{CEsat}$	$V_{GE}=15\text{V}$ , $I_C=40\text{A}$	1.4	1.7	2.1	
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_C=1.5\text{mA}$ , $V_{GE}=V_{CE}$	5.0	5.8	6.5	
Zero gate voltage collector current	$I_{CES}$	$V_{CE}=1200\text{V}$ , $V_{GE}=0\text{V}$	-	-	4.8	$\mu\text{A}$
Gate-emitter leakage current	$I_{GES}$	$V_{CE}=0\text{V}$ , $V_{GE}=20\text{V}$	-	-	600	nA
Integrated gate resistor	$r_G$		6			$\Omega$

## Electrical Characteristics <sup>3</sup>

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter saturation voltage	$V_{CEsat}$	$V_{GE}=15\text{V}$ , $I_C=40\text{A}$ , $T_{vj}=150^{\circ}\text{C}$	-	2.3	-	V
Input capacitance	$C_{ies}$	$V_{CE}=25\text{V}$ , $V_{GE}=0\text{V}$ , $f=1\text{MHz}$ , $T_{vj}=25^{\circ}\text{C}$	-	2500	-	pF
Reverse transfer capacitance	$C_{res}$		-	110	-	

<sup>2</sup> Depending on thermal properties of assembly.

<sup>3</sup> Not subject to production test - verified by design/characterization.

<sup>4</sup> Allowed number of short circuits: <1000; time between short circuits: >1s.



# SIGC41T120R3LE

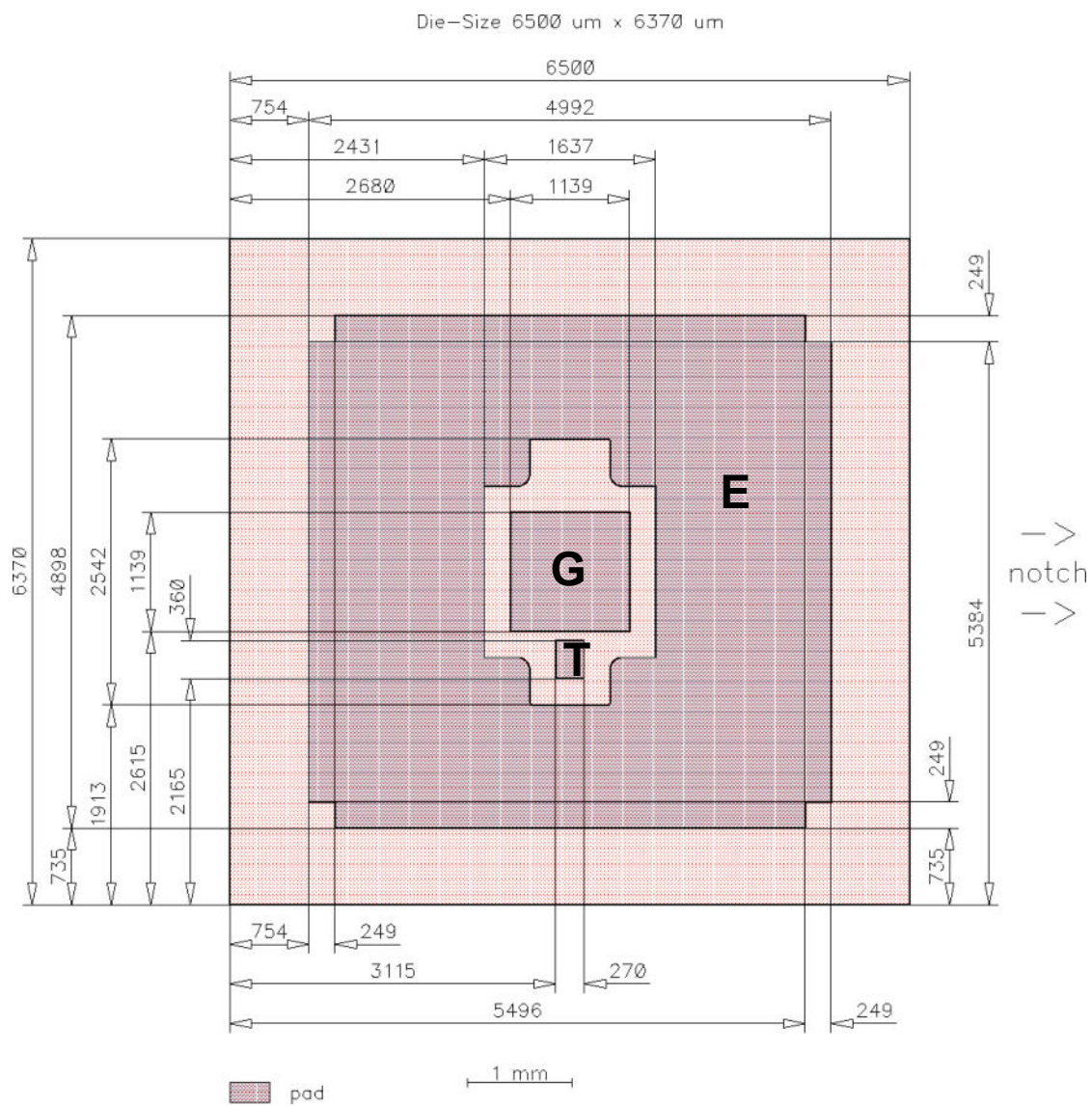
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**Further Electrical Characteristics**

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

Application example	IGW40T120	Rev. 2.4
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## Chip Drawing



**E** = Emitter

**G** = Gate

**T** = Test pad do not contact



# SIGC41T120R3LE

## Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

## Description

AQL 0.65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

## Revision History

Revision	Subjects (major changes since last revision)	Date
2.0	Release of final datasheet, change wafer size to 200mm	30.04.2010
2.1	Additional basic types L7651N, L7651U, L7651F	27.06.2014
2.2	Minor changes, chip drawing	06.02.2015
2.3	Update disclaimer	19.08.2015

## Relevant Application Notes

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**Infineon Technologies AG**  
**81726 München, Germany**  
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