

# SIGC42T120C

## IGBT Chip in NPT-technology

### Features:

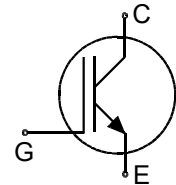
- 1200V NPT technology
- low turn-off losses
- positive temperature coefficient
- easy paralleling

### This chip is used for:

- power module  
BUP 314

### Applications:

- drives



Chip Type	V <sub>CE</sub>	I <sub>C</sub>	Die Size	Package
SIGC42T120C	1200V	25A	6.59 x 6.49 mm <sup>2</sup>	sawn on foil

### Mechanical Parameter

Raster size	6.59 x 6.49	mm <sup>2</sup>
Emitter pad size	2 x ( 1.58 x 2.18 )	
Gate pad size	1.06 x 0.65	
Area total	42.8	
Thickness	200	µm
Wafer size	150	mm
Max.possible chips per wafer	334	
Passivation frontside	Photoimide	
Pad metal	3200 nm AlSiCu	
Backside metal	Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	Electrically conductive glue or solder	
Wire bond	Al, <500µm	
Reject ink dot size	Ø 0.65mm ; max 1.2mm	
Recommended storage environment	Store in original container, in dry nitrogen, in dark environment, < 6 month at an ambient temperature of 23°C	



# SIGC42T120C

## Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, $T_{vj} = 25^\circ\text{C}$	$V_{CE}$	1200	V
DC collector current, limited by $T_{vj\text{ max}}$	$I_C$	<sup>1)</sup>	A
Pulsed collector current, $t_p$ limited by $T_{vj\text{ max}}$	$I_{C,puls}$	75	A
Gate emitter voltage	$V_{GE}$	$\pm 20$	V
Junction temperature range	$T_{vj}$	$-55 \dots +175$	$^\circ\text{C}$
Operating junction temperature	$T_{vj}$	$-55 \dots +150$	$^\circ\text{C}$
Short circuit data <sup>2)</sup> $V_{GE} = 15\text{V}$ , $V_{CC} = 900\text{V}$ , $T_{vj} = 150^\circ\text{C}$	$t_{SC}$	10	$\mu\text{s}$
Reverse bias safe operating area <sup>2)</sup> (RBSOA)	$I_{C,max} = 50\text{A}$ , $V_{CE,max} = 1200\text{V}$ $T_{vj} \leq 150^\circ\text{C}$		

<sup>1)</sup> depending on thermal properties of assembly

<sup>2)</sup> not subject to production test - verified by design/characterization

## Static Characteristic (tested on wafer), $T_{vj} = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$ , $I_C = 1.5\text{mA}$	1200			V
Collector-Emitter saturation voltage	$V_{CEsat}$	$V_{GE}=15\text{V}$ , $I_C=25\text{A}$	2.0	2.5	3.0	
Gate-Emitter threshold voltage	$V_{GE(th)}$	$I_C=1\text{mA}$ , $V_{GE}=V_{CE}$	4.5	5.5	6.5	
Zero gate voltage collector current	$I_{CES}$	$V_{CE}=1200\text{V}$ , $V_{GE}=0\text{V}$			3.1	$\mu\text{A}$
Gate-Emitter leakage current	$I_{GES}$	$V_{CE}=0\text{V}$ , $V_{GE}=20\text{V}$			120	nA
Integrated gate resistor	$r_G$			none		$\Omega$

## Dynamic Characteristic (not subject to production test - verified by design / characterization),

$T_{vj} = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	$C_{ies}$	$V_{CE}=25\text{V}$ , $V_{GE}=0\text{V}$ , $f=1\text{MHz}$		1650		pF
Output capacitance	$C_{oes}$			250		
Reverse transfer capacitance	$C_{res}$			110		



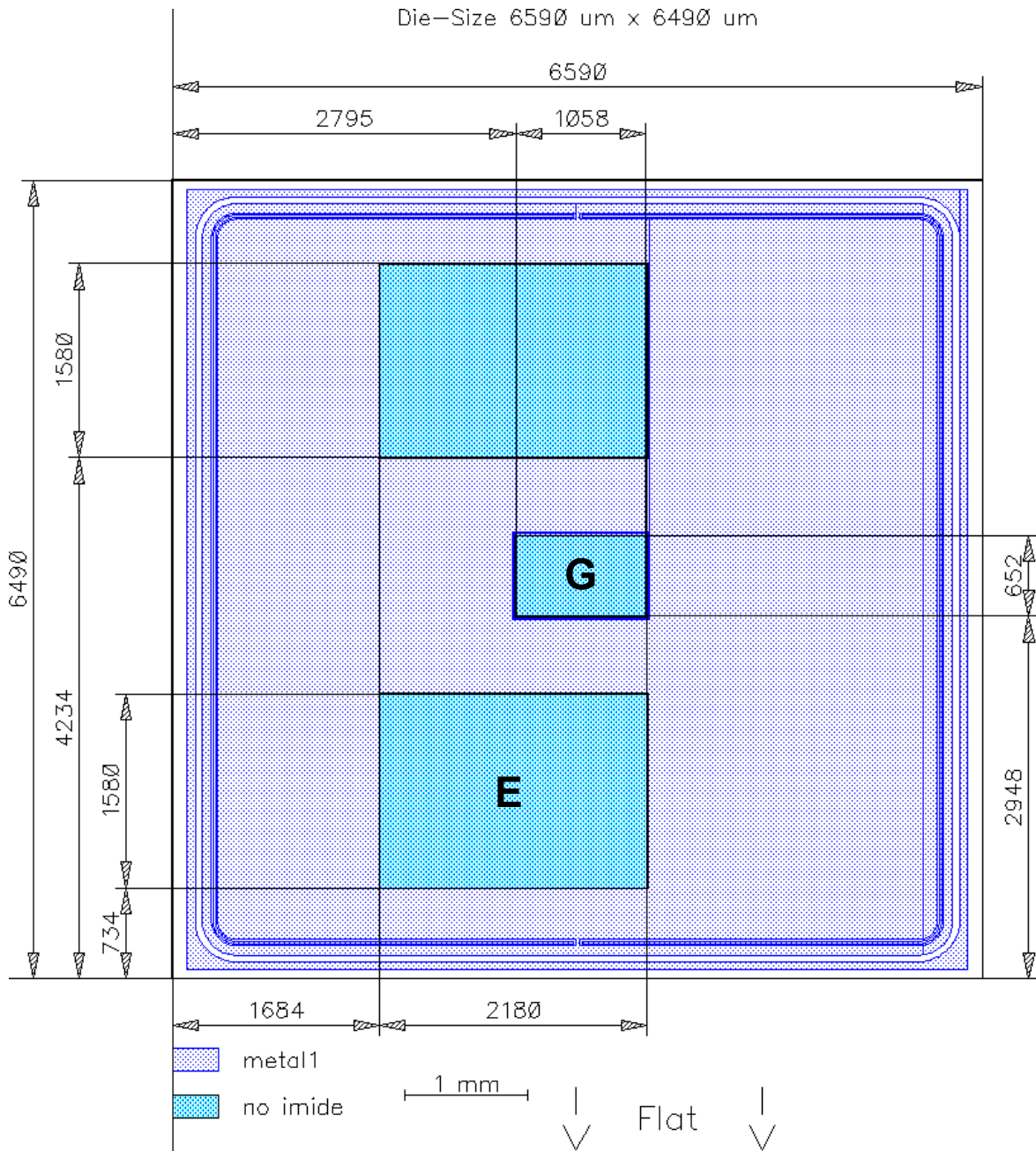
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### **Further Electrical Characteristic**

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

## Chip Drawing



**E** = Emitter pad

**G** = Gate pad



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## Description

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AQL 0,65 for visual inspection according to failure catalogue

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Electrostatic Discharge Sensitive Device according to MIL-STD 883

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